

TUPP+622



PM5363 TUPP+622

DATASHEET

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ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S  
INTERFACES

# PM5363

## TUPP+622

SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR  
FOR 622 MBIT/S INTERFACES

# DATASHEET

RELEASED  
ISSUE 4: JULY 2000

**REVISION HISTORY**

| <b>Issue No.</b> | <b>Issue Date</b> | <b>Details of Change</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Issue 4          | July 2000         | Update for revision B device. De-document TU3 Inband Error feature. Added changes to timing and operating conditions. All Input Hold Times for SCLK (19.44MHz) are changed from 1ns to 1.5ns. All Output Max Prop Delays for HSCLK (77.76MHz) changed from 8ns to 9ns. All Output Min Prop Delay for SCLK (19.44MHz) changed from 2ns to 3.5ns. Operating Condition for V <sub>DD3.3</sub> changed from 3.3V ± 10% to 3.3V ± 0.3V and operating condition for V <sub>DD2.5</sub> changed from 2.5V ± 10% to 2.5V ± 0.2V. TUGEN Bit and TUGBYP Bit description changed. Device ID Revision Number, SOS Bit description and Boundary Scan ID changed. |
| Issue 3          | Nov 1999          | Update Data-sheet portion to preliminary.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Issue 2          | May 1999          | Update pin and register description.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Issue 1          | December 1998     | Document created.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

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## **1 FEATURES**

- Configurable, multi-channel, payload processor for aligning SONET virtual tributaries (VTs) (SDH tributary units, TUs) in an STS-12 or four STS-3 (an STM-4 or four STM-1) byte serial data streams.
- Four TUPP+622 may be used in parallel to support STS-48 (STM-16) applications.
- Transfers all incoming tributaries in the twelve STS-1 synchronous payload envelopes of an STS-12 or four STS-3 byte serial streams to the corresponding twelve STS-1 synchronous payload envelopes of an outgoing STS-12 or four outgoing STS-3 byte serial streams.
- Transfers all incoming tributaries in the four AU4 or twelve AU3 administrative units of an STM-4 or four STM-1 byte serial streams to the corresponding four AU4 or twelve AU3 administrative units of an outgoing STM-4 or four outgoing STM-1 byte serial streams.
- Compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) payload frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, or TU11) tributary pointers.
- Provides software configurable offset between the payload frame boundaries and the transport frame boundary on a per STS-3 or STM-1 basis.
- Optionally bypasses the tributary pointer interpretation function. Tributary payload frame boundaries and payload bytes are identified by signals coincident with the incoming data stream.
- Configurable to process any legal mix of VT1.5, VT2, VT3, VT6, TU11, TU12, TU2, or TU3 tributaries. Each VT group or TUG2 can be configured to carry one of four tributary types. TUG2s can be multiplexed into VC3s or TUG3s. Each TUG3 can also be configured to carry a single TU3.
- Independently configurable for AU3 or AU4 frame format on incoming and outgoing interfaces.



- Configurable to process 16-byte or 64-byte format tributary path trace messages (tributary trail trace identifiers).
- Optionally frames to the H4 byte in the path overhead to determine tributary multiframe boundaries. Inserts internally generated H4 bytes with leading logic 1 bits into the outgoing administrative units.
- Extracts and serializes the entire tributary path overhead of each tributary into lower speed serial streams.
- Extracts tributary size (SS) bits of each tributary into internal registers.
- Detects loss of pointer (LOP) and re-acquisition for each tributary and optionally generates interrupts.
- Detects tributary path alarm indication signal (AIS) and return to normal state for each tributary and optionally generates interrupts.
- Detects tributary elastic store underflow and overflow errors and optionally generates interrupts.
- Extracts tributary path trace message (trail trace identifier) of each tributary into internal buffers.
- Provides individual tributary path trace message buffer that holds the expected message and detects tributary path trace mismatch (trail trace identifier mismatch) alarms (TIM) and return to matched state for each tributary and optionally generates interrupts.
- Detects tributary path trace unstable (trail trace identifier unstable) alarms (TIU) and return to stable state for each tributary and optionally generates interrupts.
- Extracts tributary path signal label for each tributary into internal registers and detects change of tributary path signal label events (COPSL) of each tributary and optionally generates interrupts.
- Provides individual tributary path signal label register that hold the expected label and detects tributary path signal label mismatch alarms (PSLM) and return to matched state for each tributary and optionally generates interrupts.

- Detects tributary path signal label unstable alarms (PSLU) and return to stable state for each tributary and optionally generates interrupts.
- Detects tributary unequipped defect (UNEQ) and tributary path defect indication (PDI-V).
- Detects assertion and removal of tributary extended remote defect indications (RDI) for each tributary and optionally generates interrupts.
- Calculates and compares the tributary path BIP-2 error detection code for each tributary and configurable to accumulate the BIP-2 errors, on block or bit basis, in internal registers.
- Calculates and compares the TU3 path BIP-8 error detection code for each TU3 stream and accumulates the BIP-8 errors, on block or bit basis, in internal registers.
- Accumulates TU3 tributary remote error indications (REI) on a bit or a block basis, in internal registers.
- Allows insertion of all-zeros or all-ones tributary idle code with unequipped indication and valid pointer into any tributary under software control. Idle tributaries are identified by an output signal.
- Identifies outgoing tributaries that are in AIS state by an output signal. Allows software to force the AIS insertion on a per tributary basis.
- Inserts valid H4 byte and all-zeros fixed stuff bytes on the outgoing stream. Remaining path overhead bytes (J1, B3, C2, G1, F2, Z3, Z4, and Z5) can be configured to be set to all-zeros or to reflect the value of the corresponding POH bytes in the incoming stream.
- Inserts valid pointers (H1, H2), framing bytes (A1, A2), and all-zeros transport overhead bytes on the outgoing stream with valid "TeleCombus" control signals.
- Supports in-band error reporting by updating the REI, RDI and auxiliary RDI bits in the V5 byte (G1 in TU3) with the status of the incoming stream.

- Provides low maximum tributary processing delay of 33  $\mu$ s for VT1.5, 25  $\mu$ s for VT2, 17  $\mu$ s for VT3, and 9  $\mu$ s for VT6 streams.
- Verifies parity on the IC1J1 and IPL signals and on the incoming data stream and generates parity on the outgoing data stream.
- May be used for multiframe synchronization or ring closure at the head-end node of a SONET/SDH ring.
- Operates in conjunction with the PM5313 SPECTRA-622 SONET/SDH Payload Extractor/Aligner For 622 Mbit/s or the PM5342 SPECTRA-155 SONET/SDH Payload Extractor/Aligner to align tributaries such that they can be switched by the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect. Provides backwards compatibility with the PM5362 TUPP SONET/SDH Tributary Unit Payload Processor / Performance Monitor.
- Independently configurable incoming and outgoing interfaces that operate in the 19.44 MHz STM-1 (STS-3) or the 77.76 MHz STM-4 (STS-12) byte interface modes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a standard 5 signal IEEE P1149.1 JTAG test port for boundary scan test purposes.
- Low power, +2.5 Volt, CMOS technology, +3.3 Volt TTL compatible inputs and outputs (5V tolerant).
- 304 pin Super BGA package.

## **2 APPLICATIONS**

- SONET/SDH Digital Cross-Connect
- SONET/SDH Add-Drop Multiplexer

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## **4 DEFINITIONS**

The following table defines the abbreviations for the TUPP+622.

|      |                                   |
|------|-----------------------------------|
| VTPP | Tributary Payload Processor       |
| RTOP | Tributary Overhead Processor      |
| RTTB | Tributary Trace Buffer            |
| STP  | STM-1 (STS-3) Tributary Processor |

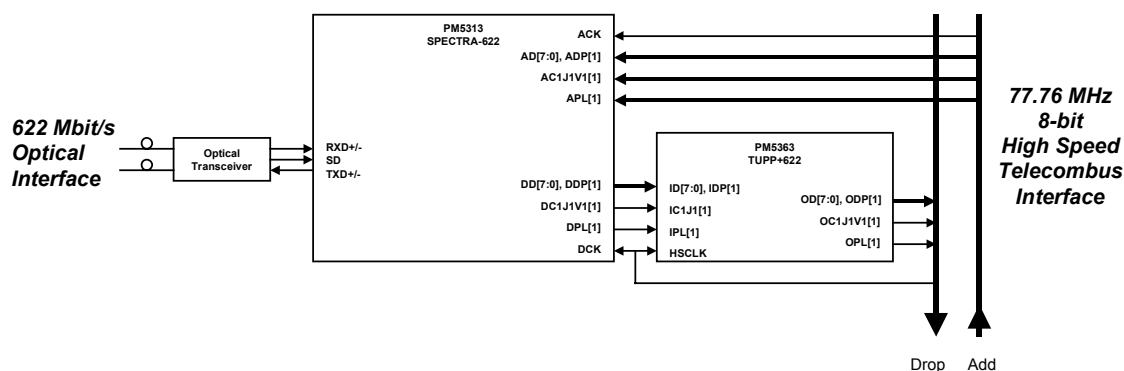
## 5 APPLICATION EXAMPLES

The TUPP+622 can be used in SONET/SDH network elements including switches, terminal multiplexers, and add-drop multiplexers. In such applications, the TUPP+622 performs VT (TU) pointer processing to align the virtual tributaries to facilitate cross-connecting and SONET ring closure. The TUPP+622 also performs performance monitoring of any legal mix of tributaries to implement intermediate performance monitoring. The TUPP+622 is well suited to process data from one STS-12 (STM-4), four STS-3's (STM-1's) or one quarter of an STS-48 (STM-16).

### 5.1 STS-12 (STM-4) AGGREGATE INTERFACE

Figure 1 shows how the TUPP+622 is used to implement a single 77.76 MHz STS-12 (STM-4) aggregate interface. In this application, the PM5313 SPECTRA-622 performs SONET/SDH section, line and path termination and the PM5363 TUPP+622 performs tributary pointer processing and performance monitoring.

**Figure 1 - STS-12 (STM-4) Aggregate Interface with Tributary Processing and Performance Monitoring**

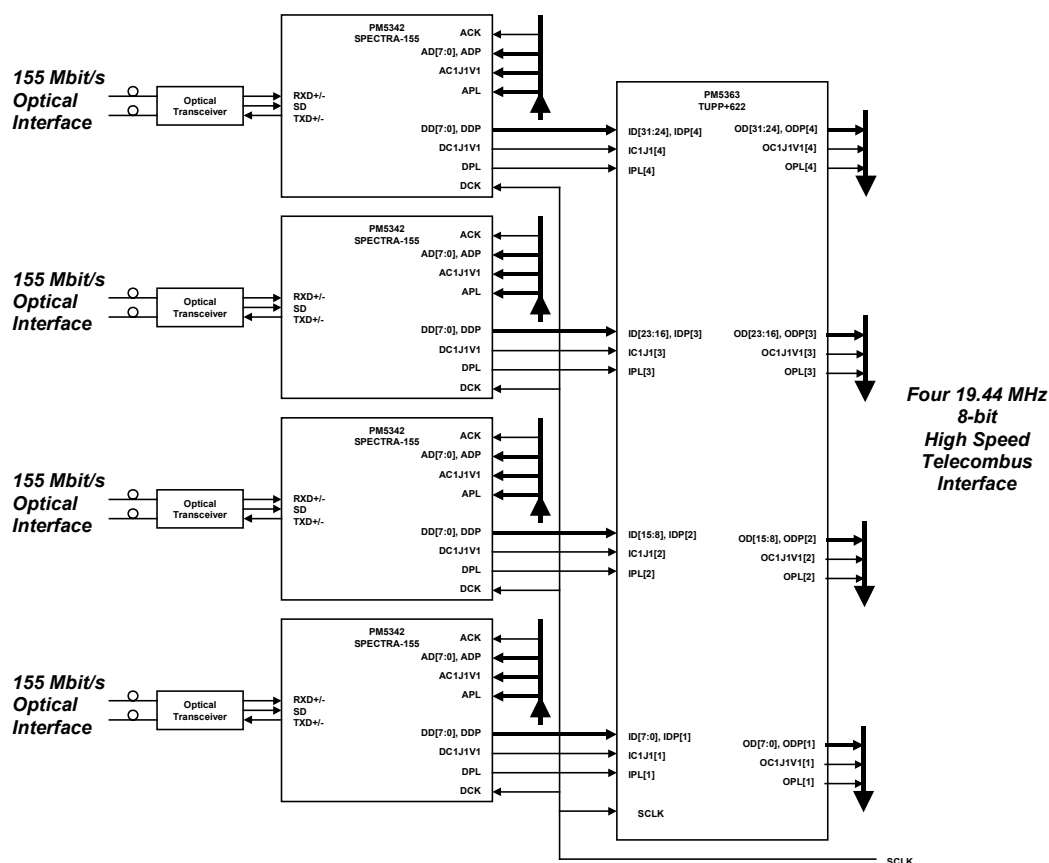




## 5.2 QUAD STS-3 (STM-1) AGGREGATE INTERFACE

The system side interface of the TUPP+622 can be configured to interface to four SPECTRA-155's Telecombuss interface. Figure 2 shows how the TUPP+622 is connected to quad STS-3 (STM-1) aggregate interface using four 19.44 MHz Telecom buses on the system side interface. In this application, the PM5342 SPECTRA-155's perform SONET/SDH section, line and path termination and the PM5363 TUPP+622 performs tributary pointer processing and performance monitoring.

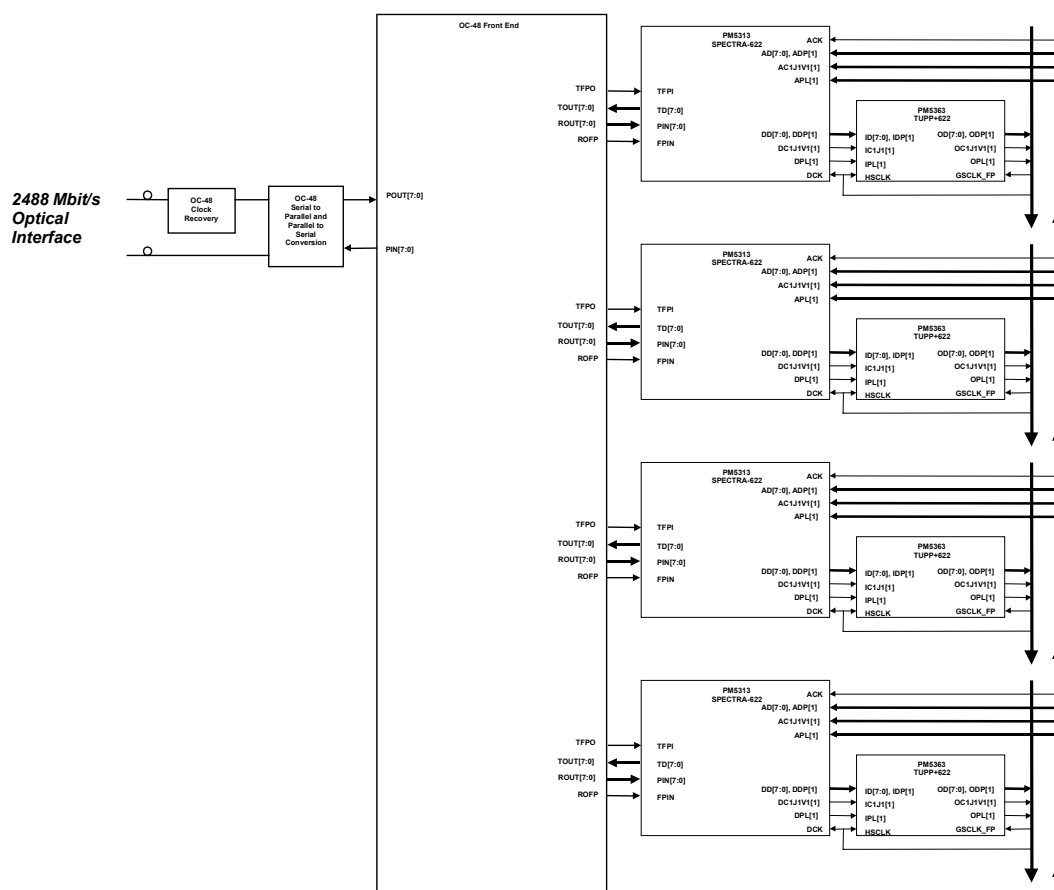
**Figure 2 - Quad STS-3 (STM-1) Aggregate Interface with Tributary Processing and Performance Monitoring**



## 5.3 STS-48 (STM-16) AGGREGATE INTERFACE

Four PM5363 TUPP+622 devices can be connected to four PM5313 SPECTRA-622 devices and an OC-48 front end transceiver device to implement an STS-48 (STM-16) aggregate interface. Figure 3 shows a block diagram for the STS-48 (STM-16) application. In this application, the OC-48 transceiver performs SONET/SDH section and line processing, the SPECTRA-622 devices perform SONET/SDH path processing, line rate decoupling, and pointer processing, and the TUPP+622 devices perform VT (TU) pointer processing and performance monitoring.

**Figure 3 - STS-48 (STM-16) Aggregate Interface with Tributary Processing and Performance Monitoring**



## **5.4 TUPP-PLUS Compatibility and TUPP+622 Feature Enhancements**

The TUPP+622 (PM5363) supports software configuration of the payload frame alignment in the outgoing data stream. The high order path active offset may be set to any alignment on a per-STM-1 (STS-3) basis. For example, by setting the outgoing stream active offset contained in the STP Outgoing Pointer MSB and LSB registers in STM-1 (STS-3) Tributary Processor #1 (STP #1) to zero, the J1 byte(s) of the outgoing AU3/AU4 in STM-1 (STS-3) #1 will be aligned to the first payload byte(s) immediately following the H3 bytes. Similarly, the J1 byte(s) can be aligned to the payload byte(s) immediately after the J0/Z0 bytes of the section overhead by setting the outgoing stream active offset to 522. In the TUPP-PLUS (PM5362), arbitrary placement of payload frame boundaries, is supported by placing the device in floating mode and supplying the device with an outgoing payload active signal (OPL) and a payload frame alignment signal (J1 portion of OC1J1). Since the TUPP+622 supports this feature in software, floating mode is no longer required. Consequently, the OC1J1 and OPL signals are deleted. The transport frame alignment of the outgoing data stream corresponds to a delayed version of the incoming data stream. To improve signal naming consistency in the TUPP+622, the TUPP-PLUS equivalent LC1J1V1 and LPL signals are renamed to OC1J1V1 and OPL, respectively. An input generated system clock frame position (GSCLK\_FP) signal is added to the TUPP+622 to enable externally alignment of the GSCLK generation and related internal operation of the device when the 77.76 MHz STM-4 interface mode is selected for the incoming or outgoing interface. This feature allows a deterministic transport frame delay through the TUPP+622 to be set. This is essential when multiple TUPP+622 devices have to be aligned in processing data streams with aggregate bandwidth greater than an STM-4.

## **6 DESCRIPTION**

The PM5363 TUPP+622 SONET/SDH Tributary Unit Payload Processor For 622 Mbit/s Interfaces is a monolithic integrated circuit that implements a configurable, multi-channel, payload processor that aligns and monitors performance of SONET virtual tributaries (VTs) or SDH tributary units (TUs.).

When configured for SONET compatible operation, the TUPP+622 transfers all incoming tributaries in the twelve STS-1 synchronous payload envelopes of an STS-12 or four STS-3 byte serial streams to the corresponding twelve STS-1 synchronous payload envelopes of an outgoing STS-12 or four outgoing STS-3 byte serial streams. Similarly, when configured for SDH compatible operation, the TUPP+622 transfers all incoming tributaries in the four AU4 or twelve AU3 administrative units of an STM-4 or four STM-1 byte serial streams to the corresponding four AU4 or twelve AU3 administrative units of an outgoing STM-4 or four outgoing STM-1 byte serial streams. The TUPP+622 compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) synchronous payload envelope frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, TU11) tributary pointers. The incoming and outgoing data streams are configurable independently.

The TUPP+622 is configurable to process any legal mix of tributaries. Each VT group can be configured to carry any one of the four tributary types (VT1.5, VT2, VT3, or VT6) and each TUG2 can be configured to carry any one of three tributary types (TU11, TU12, or TU2). TUG2s can be multiplexed into a VC3 or a TUG3. Alternatively, each TUG3 can be configured to carry a TU3.

The TUPP+622 operates in conjunction with the PM5313 SPECTRA-622 SONET/SDH Payload Extractor/Aligner For 622 Mbit/s or the PM5342 SPECTRA-155 SONET/SDH Payload Extractor/Aligner to align tributaries such that they can be switched by the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect.

The TUPP+622 provides useful maintenance functions. They include, for each tributary, detection of loss of pointer, detection of AIS alarm, detection of tributary path signal label mismatch and unstable alarms, detection of tributary path trace mismatch and unstable alarms. Optionally, interrupts can be generated due to the assertion and removal of any of the above alarm conditions. The TUPP+622 counts received tributary path BIP-2 (BIP-8 for TU3) errors on a block or bit basis

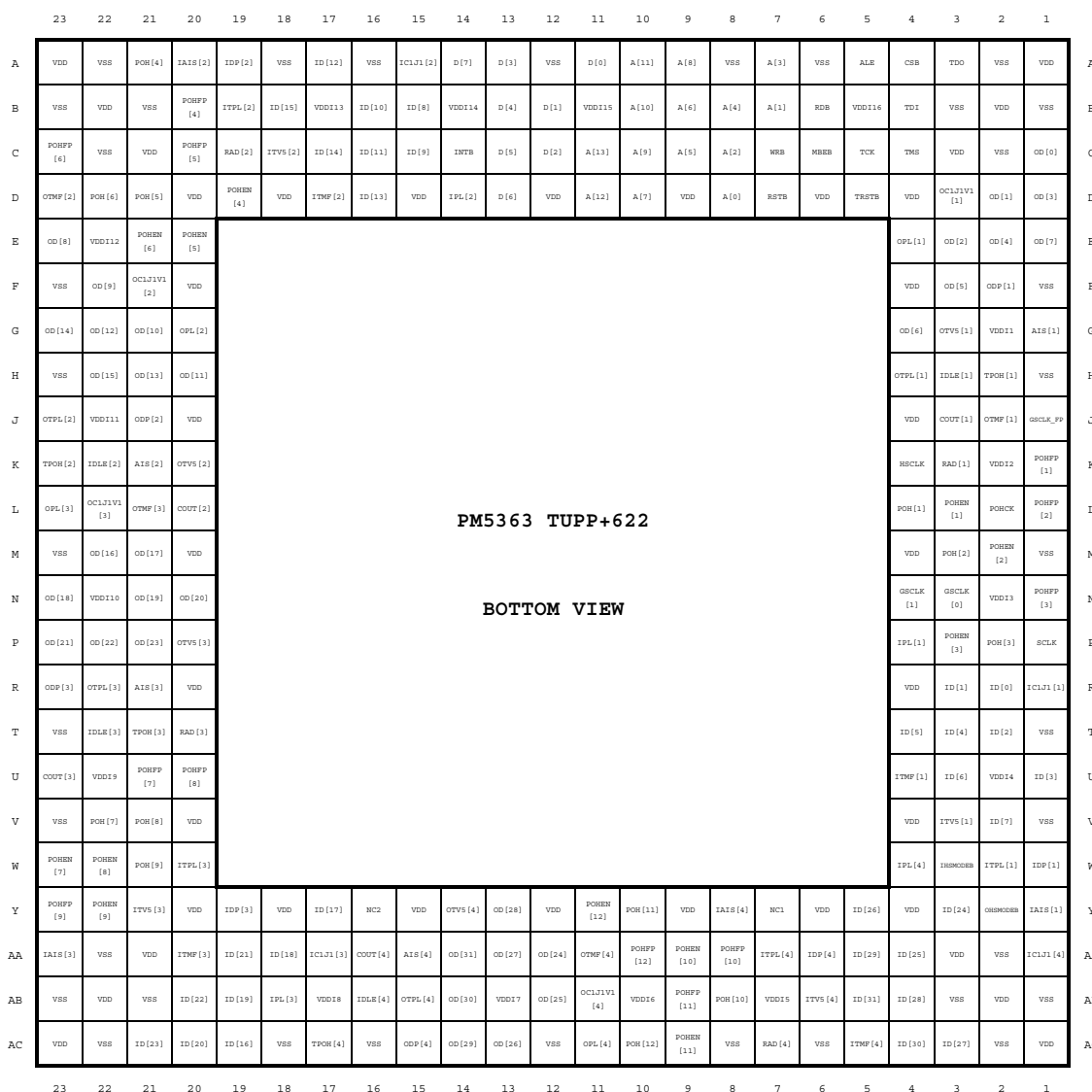
and counts REI indications. The TUPP+622 also allows insertion of tributary path AIS as a consequence of any of the above alarm conditions. In addition, the TUPP+622 may insert tributary idle (unequipped) into any tributary. Incoming tributary path trace messages and path signal labels are stored in a set of microprocessor accessible registers. The TUPP+622 can also insert inverted new data flag fields that can be used to diagnose downstream pointer processing elements.

No auxiliary high speed clocks are required as the TUPP+622 operates from either a single 19.44 MHz or a single 77.76 MHz line rate clock. The TUPP+622 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

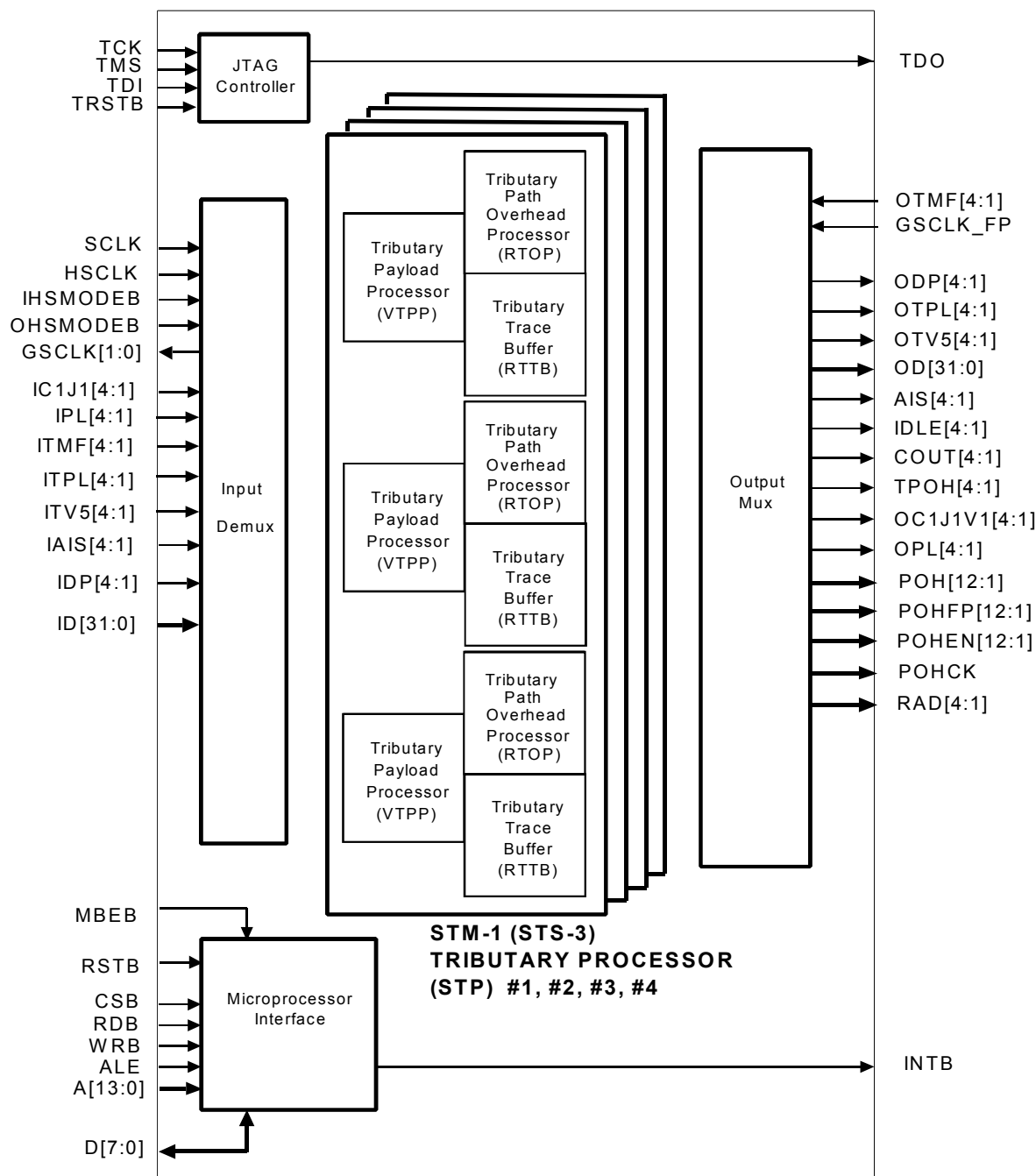
The TUPP+622 is implemented in low power, +2.5 Volt Core and +3.3 Volt I/O, CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 304 pin SBGA package.

## 7 PIN DIAGRAM

The TUPP+622 is packaged in a 304 pin SBGA package having a body size of 31 mm by 31 mm and a pin pitch of 1.27 mm.



## 8 BLOCK DIAGRAM



## 9 PIN DESCRIPTION (304)

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|-------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SCLK/    | Input | P1      | <p>The system clock (SCLK) provides timing for TUPP+622 internal operations. SCLK is a 19.44 MHz, nominally 50% duty cycle, clock. When either incoming interface is in STM-4 mode (IHSMODEB set low) or the outgoing interface is in STM-4 mode (OHSMODEB set low), SCLK must be connected to GSCLK[0] externally.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IC1J1[4:1], IPL[4:1], ITMF[4:1], IDP[4:1], ID[31:0], ITV5[4:1], ITPL[4:1], IAIS[4:1] and OTMF[4:1] are sampled on the rising edge of SCLK. In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), ODP[4:1], OTPL[4:1], OTV5[4:1], OD[31:0], AIS[4:1], IDLE[4:1], TPOH[4:1], OC1J1V1[4:1] and OPL[4:1] are updated on the rising edge of SCLK.</p> |
| VCLK     |       |         | The test vector clock (VCLK) signal is used during TUPP+622 production testing to verify manufacture.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |



| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|-------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HSCLK    | Input | K4      | <p>The High-Speed STM-4 (STS-12) interface mode system clock (HSCLK) provides timing for TUPP+622 internal operations in incoming or outgoing STM-4 (STS-12) interface mode (IHSMODEB or OHSMODEB set low). HSCLK is a 77.76 MHz, nominally 50% duty cycle, clock.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IC1J1[1], IPL[1], ITMF[1], IDP[1], ID[7:0], ITV5[1], ITPL[1] and LAIS[1] are sampled on the rising edge of HSCLK. In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTMF[1] and GSCLK_FP are sampled on the rising edge of HSCLK, and ODP[1], OTPL[1], OTV5[1], OD[7:0], AIS[1], IDLE[1], TPOH[1], OC1J1V1[1] and OPL[1] are updated on the rising edge of HSCLK. When the incoming and the outgoing interfaces are in STM-1 mode (IHSMODEB and OHSMODEB both set high), HSCLK may be left unconnected. HSCLK has an integral pull-up resistor.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IHSMODEB | Input | W3      | The active low incoming High-Speed interface mode signal (IHSMODEB) configures the incoming interface mode of the TUPP+622. When IHSMODEB is set low, the 77.76 MHz STM-4 (STS-12) interface mode is selected. SCLK must be connected to GSCLK[0]. IC1J1[1], IPL[1], ITMF[1], IDP[1], ID[7:0], ITV5[1], ITPL[1], IAIS[1] are sampled on the rising edge of HSCLK. When IHSMODEB is set high, the 19.44 MHz STM-1 (STS-3) interface mode is selected. IC1J1[4:1], IPL[4:1], ITMF[4:1], IDP[4:1], ID[31:0], ITV5[4:1], ITPL[4:1], IAIS[4:1] are sampled on the rising edge of SCLK. IHSMODEB has an integral pull-up resistor.                                                                                                              |
| OHSMODEB | Input | Y2      | The outgoing High-Speed interface mode signal (OHSMODEB) configures the outgoing interface mode of the TUPP+622. When OHSMODEB is set low, the 77.76 MHz STM-4 (STS-12) interface mode is selected. SCLK must be connected to GSCLK[0]. OTMF[1] and GSCLK_FP are sampled on the rising edge of HSCLK. ODP[1], OTPL[1], OTV5[1], OD[7:0], AIS[1], IDLE[1], OC1J1V1[1] and OPL[1] are updated on the rising edge of HSCLK. When OHSMODEB is set high, the 19.44 MHz STM-1 (STS-3) interface mode is selected. OTMF[4:1] are sampled on the rising edge of SCLK. ODP[4:1], OTPL[4:1], OTV5[4:1], OD[31:0], AIS[4:1], IDLE[4:1], OC1J1V1[4:1] and OPL[4:1] are updated on the rising edge of SCLK. OHSMODEB has an integral pull-up resistor. |

| Pin Name             | Type   | Pin No.  | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GSCLK[1]<br>GSCLK[0] | Output | N4<br>N3 | The generated system clock (GSCLK[1:0]) signals provide timing for the TUPP+622 when STM-4 (STS-12) interface mode is selected at the incoming or outgoing interface (IHSMODEB or OHSMODEB set low). GSCLK[1:0] are a divide by four of HSCLK. GSCLK[0] must only be connected to SCLK externally when IHSMODEB or OHSMODEB is set low. GSCLK[1] is a exact replica of GSCLK[0] and can be used to supply timing to external devices that are operating in the 19.44 MHz STM-1 (STS-3) interface timing domain. GSCLK[1:0] are updated on the rising edge of HSCLK. |

## DATASHEET

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**ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S  
INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IC1J1[1] | Input | R1      | <p>The input C1/J1 frame pulse #1 (IC1J1[1]) identifies the transport envelope and synchronous payload envelope frame boundaries on the incoming STM-4 or STM-1 #1 stream (ID[7:0]).</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IC1J1[1] is set high while IPL[1] is low to mark the first C1 byte of the STM-1 #1 transport envelope frame on the ID[7:0] bus. The C1 byte position must be coincident to the C1 byte positions of the STM-1 streams on ID[15:8], ID[23:16] and ID[31:24]. IC1J1[1] is set high while IPL[1] is high to mark each J1 byte of the synchronous payload envelope(s) on the ID[7:0] bus. IC1J1[1] must be present at every occurrence of the first C1 and all J1 bytes. The TUPP+622 will ignore a pulse on IC1J1[1] at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IC1J1[1] is set high while IPL[1] is low to mark the first C1 byte of the STM-4 transport envelope frame on the ID[7:0] bus. IC1J1[1] is set high while IPL[1] is high to mark each J1 byte of the synchronous payload envelopes on the ID[7:0] bus. IC1J1[1] must be present at every occurrence of the first C1 and all J1 bytes. The TUPP+622 will ignore a pulse on IC1J1[1] at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1[1] is sampled on the rising edge of HCLK.</p> |

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**ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S  
INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------|-------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IC1J1[2] | Input | A15     | <p>The input C1/J1 frame pulse #2 (IC1J1[2]) identifies the transport envelope and synchronous payload envelope frame boundaries on the incoming STM-1 #2 stream (ID[15:8]).</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IC1J1[2] is set high while IPL[2] is low to mark the first C1 byte of the STM-1 #2 transport envelope frame on the ID[15:8] bus. The C1 byte position must be coincident to the C1 byte positions of the STM-1 streams on ID[7:0], ID[23:16] and ID[31:24]. IC1J1[2] is set high while IPL[2] is high to mark each J1 byte of the synchronous payload envelope(s) on the ID[15:8] bus. IC1J1[2] must be present at every occurrence of the first C1 and all J1 bytes. The TUPP+622 will ignore a pulse on IC1J1[2] at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IC1J1[2] is unused and must be strapped low.</p> |

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**ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S  
INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IC1J1[3] | Input | AA17    | <p>The input C1/J1 frame pulse #3 (IC1J1[3]) identifies the transport envelope and synchronous payload envelope frame boundaries on the incoming STM-1 #3 stream (ID[23:16]).</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IC1J1[3] is set high while IPL[3] is low to mark the first C1 byte of the STM-1 #3 transport envelope frame on the ID[23:16] bus. The C1 byte position must be coincident to the C1 byte positions of the STM-1 streams on ID[7:0], ID[15:8] and ID[31:24]. IC1J1[3] is set high while IPL[3] is high to mark each J1 byte of the synchronous payload envelope(s) on the ID[23:16] bus. IC1J1[3] must be present at every occurrence of the first C1 and all J1 bytes. The TUPP+622 will ignore a pulse on IC1J1[3] at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IC1J1[3] is unused and must be strapped low.</p> |

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**ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S  
INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IC1J1[4] | Input | AA1     | <p>The input C1/J1 frame pulse #4 (IC1J1[4]) identifies the transport envelope and synchronous payload envelope frame boundaries on the incoming STM-1 #4 stream (ID[31:24]).</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IC1J1[4] is set high while IPL[4] is low to mark the first C1 byte of the STM-1 #4 transport envelope frame on the ID[31:24] bus. The C1 byte position must be coincident to the C1 byte positions of the STM-1 streams on ID[7:0], ID[15:8] and ID[23:16]. IC1J1[4] is set high while IPL[4] is high to mark each J1 byte of the synchronous payload envelope(s) on the ID[31:24] bus. IC1J1[4] must be present at every occurrence of the first C1 and all J1 bytes. The TUPP+622 will ignore a pulse on IC1J1[4] at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IC1J1[4] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|-------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IPL[1]   | Input | P4      | <p>The active high incoming payload active #1 (IPL[1]) signal identifies the bytes within the transport envelope frame on the incoming STM-4 or STM-1 #1 stream that carry VC3 or VC4 virtual containers, or STS-1 synchronous payload envelopes.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IPL[1] must be brought high to mark each payload byte on ID[7:0]. IPL[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IPL[1] must be brought high to mark each payload byte on ID[7:0]. IPL[1] is sampled on the rising edge of HSCLK.</p> |
| IPL[2]   | Input | D14     | <p>The active high incoming payload active #2 (IPL[2]) signal identifies the bytes within the transport envelope frame on the incoming STM-1 #2 stream that carry VC3 or VC4 virtual containers, or STS-1 synchronous payload envelopes.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IPL[2] must be brought high to mark each payload byte on ID[15:8]. IPL[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IPL[2] is unused and must be strapped low.</p>                                                                               |



| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IPL[3]   | Input | AB18    | <p>The active high incoming payload active #3 (IPL[3]) signal identifies the bytes within the transport envelope frame on the incoming STM-1 #3 stream that carry VC3 or VC4 virtual containers, or STS-1 synchronous payload envelopes.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IPL[3] must be brought high to mark each payload byte on ID[23:16]. IPL[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IPL[3] is unused and must be strapped low.</p> |
| IPL[4]   | Input | W4      | <p>The active high incoming payload active #4 (IPL[4]) signal identifies the bytes within the transport envelope frame on the incoming STM-1 #4 stream that carry VC3 or VC4 virtual containers, or STS-1 synchronous payload envelopes.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IPL[4] must be brought high to mark each payload byte on ID[31:24]. IPL[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IPL[4] is unused and must be strapped low.</p> |

## DATASHEET

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INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|-------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITMF[1]  | Input | U4      | <p>The active high incoming tributary multiframe #1 (ITMF[1]) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit in the STM-4 or STM-1 #1 stream (ID[7:0]). ITMF[1] is enabled by setting the corresponding ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF[1] is selectable to pulse high during the third byte after J1 of the first frame of the tributary multiframe or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking each H4 or the third byte after each J1 is controlled by the corresponding ITMFH4 register bit. Pulses on ITMF[1] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. When ITMFH4 is low, ITMF[1] can be set high for the entire first frame of the tributary multiframe. ITMF[1] must be low for the 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> frame of the tributary multiframe. When ITMFH4 is high, ITMF[1] can be set high for the entire fourth frame of the tributary multiframe. ITMF[1] must be low for the 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> frame of the tributary multiframe.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITMF[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITMF[1] is sampled on the rising edge of HSCLK.</p> |

## DATASHEET

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**ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S  
INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITMF[2]  | Input | D17     | <p>The active high incoming tributary multiframe #2 (ITMF[2]) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit in the STM-1 #2 stream (ID[15:8]). ITMF[2] is enabled by setting the corresponding ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF[2] is selectable to pulse high during the third byte after J1 of the first frame of the tributary multiframe or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking each H4 or the third byte after each J1 is controlled by the corresponding ITMFH4 register bit. Pulses on ITMF[2] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. When ITMFH4 is low, ITMF[2] can be set high for the entire first frame of the tributary multiframe. ITMF[2] must be low for the 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> frame of the tributary multiframe. When ITMFH4 is high, ITMF[2] can be set high for the entire fourth frame of the tributary multiframe. ITMF[2] must be low for the 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> frame of the tributary multiframe.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITMF[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITMF[2] is unused and must be strapped low.</p> |

## DATASHEET

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**ISSUE 4 SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S INTERFACES**

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITMF[3]  | Input | AA20    | <p>The active high incoming tributary multiframe #3 (ITMF[3]) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit in the STM-1 #3 stream (ID[23:16]). ITMF[3] is enabled by setting the corresponding ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF[3] is selectable to pulse high during the third byte after J1 of the first frame of the tributary multiframe or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking each H4 or the third byte after each J1 is controlled by the corresponding ITMFH4 register bit. Pulses on ITMF[3] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. When ITMFH4 is low, ITMF[3] can be set high for the entire first frame of the tributary multiframe. ITMF[3] must be low for the 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> frame of the tributary multiframe. When ITMFH4 is high, ITMF[3] can be set high for the entire fourth frame of the tributary multiframe. ITMF[3] must be low for the 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> frame of the tributary multiframe.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITMF[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITMF[3] is unused and must be strapped low.</p> |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITMF[4]  | Input | AC5     | <p>The active high incoming tributary multiframe #4 (ITMF[4]) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit in the STM-1 #4 stream (ID[31:24]). ITMF[4] is enabled by setting the corresponding ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF[4] is selectable to pulse high during the third byte after J1 of the first frame of the tributary multiframe or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking each H4 or the third byte after each J1 is controlled by the corresponding ITMFH4 register bit. Pulses on ITMF[4] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. When ITMFH4 is low, ITMF[4] can be set high for the entire first frame of the tributary multiframe. ITMF[4] must be low for the 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> frame of the tributary multiframe. When ITMFH4 is high, ITMF[4] can be set high for the entire fourth frame of the tributary multiframe. ITMF[4] must be low for the 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> frame of the tributary multiframe.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITMF[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITMF[4] is unused and must be strapped low.</p> |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITPL[1]  | Input | W2      | <p>The incoming tributary payload active #1 (ITPL[1]) signal marks the bytes carrying the tributary payload for the STM-4 or STM-1 #1 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITPL[1] is ignored. Also, ITPL[1] is ignored when IPL[1] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITPL[1] is set high to mark each tributary payload byte of the STM-1 #1 stream on the ID[7:0] bus. ITPL[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITPL[1] is set high to mark each tributary payload byte of the STM-4 stream on the ID[7:0] bus. ITPL[1] is sampled on the rising edge of HSCLK.</p> |
| ITPL[2]  | Input | B19     | <p>The incoming tributary payload active #2 (ITPL[2]) signal marks the bytes carrying the tributary payload for the STM-1 #2 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITPL[2] is ignored. Also, ITPL[2] is ignored when IPL[2] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITPL[2] is set high to mark each tributary payload byte on the ID[15:8] bus. ITPL[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITPL[2] is unused and must be strapped low.</p>                                                                                                                                    |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|-------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITPL[3]  | Input | W20     | <p>The incoming tributary payload active #3 (ITPL[3]) signal marks the bytes carrying the tributary payload for the STM-1 #3 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITPL[3] is ignored. Also, ITPL[3] is ignored when IPL[3] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITPL[3] is set high to mark each tributary payload byte on the ID[23:16] bus. ITPL[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITPL[3] is unused and must be strapped low.</p> |
| ITPL[4]  | Input | AA7     | <p>The incoming tributary payload active #4 (ITPL[4]) signal marks the bytes carrying the tributary payload for the STM-1 #4 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITPL[4] is ignored. Also, ITPL[4] is ignored when IPL[4] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITPL[4] is set high to mark each tributary payload byte on the ID[31:24] bus. ITPL[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITPL[4] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|-------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITV5[1]  | Input | V3      | <p>The incoming tributary V5 byte #1 (ITV5[1]) signal marks the tributary V5 bytes of the STM-4 or STM-1 #1 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITV5[1] is ignored. Also, ITV5[1] is ignored when IPL[1] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITV5[1] is set high to mark each tributary V5 byte of the STM-1 #1 stream on the ID[7:0] bus. When the incoming tributary is a TU3, ITV5[1] marks the J1 byte of the TU3. ITV5[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITV5[1] is set high to mark each tributary V5 byte of the STM-4 stream on the ID[7:0] bus. When the incoming tributary is a TU3, ITV5[1] marks the J1 byte of the TU3. ITV5[1] is sampled on the rising edge of HSCLK.</p> |



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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------|-------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITV5[2]  | Input | C18     | <p>The incoming tributary V5 byte #2 (ITV5[2]) signal marks the tributary V5 bytes of the STM-1 #2 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITV5[2] is ignored. Also, ITV5[2] is ignored when IPL[2] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITV5[2] is set high to mark each tributary V5 byte on the ID[15:8] bus. When the incoming tributary is a TU3, ITV5[2] marks the J1 byte of the TU3. ITV5[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITV5[2] is unused and must be strapped low.</p>  |
| ITV5[3]  | Input | Y21     | <p>The incoming tributary V5 byte #3 (ITV5[3]) signal marks the tributary V5 bytes of the STM-1 #3 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITV5[3] is ignored. Also, ITV5[3] is ignored when IPL[3] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITV5[3] is set high to mark each tributary V5 byte on the ID[23:16] bus. When the incoming tributary is a TU3, ITV5[3] marks the J1 byte of the TU3. ITV5[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITV5[3] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------|-------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ITV5[4]  | Input | AB6     | <p>The incoming tributary V5 byte #4 (ITV5[4]) signal marks the tributary V5 bytes of the STM-1 #4 stream when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), ITV5[4] is ignored. Also, ITV5[4] is ignored when IPL[4] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ITV5[4] is set high to mark each tributary V5 byte on the ID[31:24] bus. When the incoming tributary is a TU3, ITV5[4] marks the J1 byte of the TU3. ITV5[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), ITV5[4] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|-------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IAIS[1]  | Input | Y1      | <p>The incoming tributary alarm indication signal #1 (IAIS[1]) marks tributaries on the incoming STM-4 or STM-1 #1 stream that are in AIS state when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), IAIS[1] is ignored. Also, IAIS[1] is ignored when IPL[1] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IAIS[1] is set high when the associated tributary of the STM-1 #1 stream on the ID[7:0] is in AIS state and is set low when the associated tributary is operating normally. IAIS[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IAIS[1] is set high when the associated tributary of the STM-4 stream on the ID[7:0] is in AIS state and is set low when the associated tributary is operating normally. IAIS[1] is sampled on the rising edge of HSCLK.</p> |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IAIS[2]  | Input | A20     | <p>The incoming tributary alarm indication signal #2 (IAIS[2]) marks tributaries on the incoming STM-STM-1 #2 stream that are in AIS state when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), IAIS[2] is ignored. Also, IAIS[2] is ignored when IPL[2] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IAIS[2] is set high when the associated tributary on the ID[15:8] is in AIS state and is set low when the associated tributary is operating normally. IAIS[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IAIS[2] is unused and must be strapped low.</p>  |
| IAIS[3]  | Input | AA23    | <p>The incoming tributary alarm indication signal #3 (IAIS[3]) marks tributaries on the incoming STM-STM-1 #3 stream that are in AIS state when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), IAIS[3] is ignored. Also, IAIS[3] is ignored when IPL[3] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IAIS[3] is set high when the associated tributary on the ID[23:16] is in AIS state and is set low when the associated tributary is operating normally. IAIS[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IAIS[3] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IAIS[4]  | Input | Y8      | <p>The incoming tributary alarm indication signal #4 (IAIS[4]) marks tributaries on the incoming STM-STM-1 #4 stream that are in AIS state when pointer interpreter bypass is enabled (PIBYP bit set high). When pointer interpreter bypass is disabled (PIBYP bit set low), IAIS[4] is ignored. Also, IAIS[4] is ignored when IPL[4] is low.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), IAIS[4] is set high when the associated tributary on the ID[31:24] is in AIS state and is set low when the associated tributary is operating normally. IAIS[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IAIS[4] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDP[1]   | Input | W1      | <p>The incoming data parity #1 (IDP[1]) signal carries the parity of the incoming signals for the STM-4 or STM-1 #1 stream.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), the parity calculation encompasses the ID[7:0] bus and optionally the IC1J1[1] and the IPL[1] signals. IC1J1[1] and IPL[1] can be included in the parity calculation by setting the corresponding INCIC1J1 and INCIPL register bits high, respectively. Odd parity is selected by setting the corresponding IOP register bit high, and even parity is selected by setting the IOP bit low. IDP[1] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), the parity calculation encompasses the ID[7:0] bus and optionally the IC1J1[1] and the IPL[1] signals. IC1J1[1] and IPL[1] can be included in the parity calculation by setting the corresponding INCIC1J1 and INCIPL register bits high, respectively. Odd parity is selected by setting the corresponding IOP register bit high, and even parity is selected by setting the IOP bit low. IDP[1] is sampled on the rising edge of HSCLK.</p> |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDP[2]   | Input | A19     | <p>The incoming data parity #2 (IDP[2]) signal carries the parity of the incoming signals for the STM-1 #2 stream.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), the parity calculation encompasses the ID[15:8] bus and optionally the IC1J1[2] and the IPL[2] signals. IC1J1[2] and IPL[2] can be included in the parity calculation by setting the corresponding INCIC1J1 and INCIPL register bits high, respectively. Odd parity is selected by setting the corresponding IOP register bit high, and even parity is selected by setting the IOP bit low. IDP[2] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IDP[2] is unused and must be strapped low.</p>  |
| IDP[3]   | Input | Y19     | <p>The incoming data parity #3 (IDP[3]) signal carries the parity of the incoming signals for the STM-1 #3 stream.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), the parity calculation encompasses the ID[23:16] bus and optionally the IC1J1[3] and the IPL[3] signals. IC1J1[3] and IPL[3] can be included in the parity calculation by setting the corresponding INCIC1J1 and INCIPL register bits high, respectively. Odd parity is selected by setting the corresponding IOP register bit high, and even parity is selected by setting the IOP bit low. IDP[3] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IDP[3] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDP[4]   | Input | AA6     | <p>The incoming data parity #4 (IDP[4]) signal carries the parity of the incoming signals for the STM-1 #4 stream.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), the parity calculation encompasses the ID[31:24] bus and optionally the IC1J1[4] and the IPL[4] signals. IC1J1[4] and IPL[4] can be included in the parity calculation by setting the corresponding INCIC1J1 and INCIPL register bits high, respectively. Odd parity is selected by setting the corresponding IOP register bit high, and even parity is selected by setting the IOP bit low. IDP[4] is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), IDP[4] is unused and must be strapped low.</p> |



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| Pin Name                                                                   | Type  | Pin No.                                              | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------------------------------------------------------|-------|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ID[0]<br>ID[1]<br>ID[2]<br>ID[3]<br>ID[4]<br>ID[5]<br>ID[6]<br>ID[7]       | Input | R2<br>R3<br>T2<br>U1<br>T3<br>T4<br>U3<br>V2         | <p>The incoming data bus (ID[7:0]) carries the STM-4 or STM-1 #1 SONET/SDH frame data in byte serial format.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), the ID[7:0] bus carries the STM-1 #1 stream. ID[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. ID[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The ID[7:0] bus is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), the ID[7:0] bus carries the STM-4 stream. ID[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. ID[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The ID[7:0] bus is sampled on the rising edge of HSCLK.</p> |
| ID[8]<br>ID[9]<br>ID[10]<br>ID[11]<br>ID[12]<br>ID[13]<br>ID[14]<br>ID[15] | Input | B15<br>C15<br>B16<br>C16<br>A17<br>D16<br>C17<br>B18 | <p>The incoming data bus (ID[15:8]) carries the STM-1 #2 SONET/SDH frame data in byte serial format.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ID[15] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. ID[8] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The ID[15:8] bus is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), the ID[15:8] bus is unused and all bus signals must be strapped low.</p>                                                                                                                                                                                                                                                                                                     |

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| Pin Name                                                                     | Type  | Pin No.                                                     | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------------------------------------------------------------------|-------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ID[16]<br>ID[17]<br>ID[18]<br>ID[19]<br>ID[20]<br>ID[21]<br>ID[22]<br>ID[23] | Input | AC19<br>Y17<br>AA18<br>AB19<br>AC20<br>AA19<br>AB20<br>AC21 | <p>The incoming data bus (ID[23:16]) carries the STM-1 #3 SONET/SDH frame data in byte serial format.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ID[23] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. ID[16] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The ID[23:16] bus is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), the ID[23:16] bus is unused and all bus signals must be strapped low.</p> |
| ID[24]<br>ID[25]<br>ID[26]<br>ID[27]<br>ID[28]<br>ID[29]<br>ID[30]<br>ID[31] | Input | Y3<br>AA4<br>Y5<br>AC3<br>AB4<br>AA5<br>AC4<br>AB5          | <p>The incoming data bus (ID[31:24]) carries the STM-1 #4 SONET/SDH frame data in byte serial format.</p> <p>In incoming STM-1 (STS-3) interface mode (IHSMODEB set high), ID[31] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. ID[24] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The ID[31:24] bus is sampled on the rising edge of SCLK.</p> <p>In incoming STM-4 (STS-12) interface mode (IHSMODEB set low), the ID[31:24] bus is unused and all bus signals must be strapped low.</p> |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GSCLK_FP | Input | J1      | <p>The active high generated system clock frame position (GSCLK_FP) signal aligns the HSCLK divide by four logic which generates the GSCLK[1:0] signals when STM-4 (STS-12) interface mode is selected at the incoming or outgoing interface (IHSMODEB or OHSMODEB set low). GSCLK_FP should be set high for one HSCLK period at an interval of four or multiples of four HSCLK periods.</p> <p>GSCLK_FP is sampled on the rising edge of HSCLK.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| OTMF[1]  | Input | J2      | <p>The active high outgoing tributary multiframe #1 (OTMF[1]) signal identifies the first frame of the tributary multiframe for each AU3, or AU4 administrative unit, or STS-1 synchronous payload envelope in the outgoing STM-4 or STM-1 #1 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), the OTMF[1] identifies the first frame of the tributary multiframe in the STM-1 stream on the OD[7:0] bus. OTMF[1] is selectable to pulse high during the third byte after J1 of the first STS-1 stream or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking the third byte after each J1 or H4 bytes is controlled by the corresponding OTMFH4 register bit. Pulses on OTMF[1] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. OTMF[1] is ignored at other byte positions. OTMF[1] is sampled on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OTMF[1] identifies</p> |

| Pin Name | Type | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |      |         | the first frame of the tributary multiframe in each STM-1 within the STM-4 (OD[7:0]) stream. OTMF[1] is selectable to pulse high during the third byte after J1 of the first STS-1 in each STM-1 or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking the third byte after each J1 or H4 bytes is controlled by the corresponding OTMFH4 register bit. Pulses on OTMF[1] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. OTMF[1] is ignored at other byte positions. OTMF[1] is sampled on the rising edge of HSCLK. |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTMF[2]  | Input | D23     | <p>The active high outgoing tributary multiframe #2 (OTMF[2]) signal identifies the first frame of the tributary multiframe for each AU3, or AU4 administrative unit, or STS-1 synchronous payload envelope in the outgoing STM-1 #2 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), the OTMF[2] identifies the first frame of the tributary multiframe in the STM-1 stream on the OD[15:8] bus. OTMF[2] is selectable to pulse high during the third byte after J1 of the first STS-1 stream or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking the third byte after each J1 or H4 bytes is controlled by the corresponding OTMFH4 register bit. Pulses on OTMF[2] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. OTMF[2] is ignored at other byte positions. OTMF[2] is sampled on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OTMF[2] is unused and must be strapped low.</p> |

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| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTMF[3]  | Input | L21     | <p>The active high outgoing tributary multiframe #3 (OTMF[3]) signal identifies the first frame of the tributary multiframe for each AU3, or AU4 administrative unit, or STS-1 synchronous payload envelope in the outgoing STM-1 #3 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), the OTMF[3] identifies the first frame of the tributary multiframe in the STM-1 stream on the OD[23:16] bus. OTMF[3] is selectable to pulse high during the third byte after J1 of the first STS-1 stream or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking the third byte after each J1 or H4 bytes is controlled by the corresponding OTMFH4 register bit. Pulses on OTMF[3] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. OTMF[3] is ignored at other byte positions. OTMF[3] is sampled on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OTMF[3] is unused and must be strapped low.</p> |

| Pin Name | Type  | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTMF[4]  | Input | AA11    | <p>The active high outgoing tributary multiframe #4 (OTMF[4]) signal identifies the first frame of the tributary multiframe for each AU3, or AU4 administrative unit, or STS-1 synchronous payload envelope in the outgoing STM-1 #4 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), the OTMF[4] identifies the first frame of the tributary multiframe in the STM-1 stream on the OD[31:24] bus. OTMF[4] is selectable to pulse high during the third byte after J1 of the first STS-1 stream or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking the third byte after each J1 or H4 bytes is controlled by the corresponding OTMFH4 register bit. Pulses on OTMF[4] are only effective during the H4 or third byte after each J1 byte positions, as appropriate. OTMF[4] is ignored at other byte positions. OTMF[4] is sampled on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OTMF[4] is unused and must be strapped low.</p> |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| COUT[1]  | Output | J3      | <p>The controlled output signal #1 (COUT[1]) is a software programmable output that is controlled by the COUTx register bit associated with each tributary in the STM-4 or STM-1 #1 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), COUT[1] is synchronized to the STM-1 #1 stream on OD[7:0] bus. COUT[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), COUT[1] is synchronized to the STM-4 stream on OD[7:0] bus. COUT[1] is updated on the rising edge of HSCLK.</p> |
| COUT[2]  | Output | L20     | <p>The controlled output signal #2 (COUT[2]) is a software programmable output that is controlled by the COUTx register bit associated with each tributary in the STM-1 #2 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), COUT[2] is synchronized to the OD[15:8] bus. COUT[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), COUT[2] is invalid.</p>                                                                                                                    |
| COUT[3]  | Output | U23     | <p>The controlled output signal #3 (COUT[3]) is a software programmable output that is controlled by the COUTx register bit associated with each tributary in the STM-1 #3 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), COUT[3] is synchronized to the OD[23:16] bus. COUT[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), COUT[3] is invalid.</p>                                                                                                                   |



| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| COUT[4]  | Output | AA16    | <p>The controlled output signal #4 (COUT[4]) is a software programmable output that is controlled by the COUTx register bit associated with each tributary in the STM-1 #4 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), COUT[4] is synchronized to the OD[31:24] bus. COUT[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), COUT[4] is invalid.</p> |

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| Pin Name                                                             | Type   | Pin No.                                      | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------------------|--------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OD[0]<br>OD[1]<br>OD[2]<br>OD[3]<br>OD[4]<br>OD[5]<br>OD[6]<br>OD[7] | Output | C1<br>D2<br>E3<br>D1<br>E2<br>F3<br>G4<br>E1 | <p>The outgoing data bus (OD[7:0]) carries the STM-4 or STM-1 #1 SONET/SDH frame data in byte serial format.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), the OD[7:0] bus carries the STM-1 #1 stream. OD[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. OD[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. OD[7:0] is set to all-zeros at transport overhead bytes, except for the A1 and A2 framing bytes and the H1 and H2 pointer bytes. Pointer offset is determined by the STP Outgoing Pointer MSB and LSB registers. The OD[7:0] bus is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the ID[7:0] bus carries the STM-4 stream. OD[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. OD[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. OD[7:0] is set to all-zeros at transport overhead bytes, except for the A1 and A2 framing bytes and the H1 and H2 pointer bytes. Pointer offset is determined by the STP Outgoing Pointer MSB and LSB registers. The OD[7:0] bus is updated on the rising edge of HSCLK.</p> |

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| Pin Name                                                                   | Type   | Pin No.                                              | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------------------------------------------------|--------|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OD[8]<br>OD[9]<br>OD[10]<br>OD[11]<br>OD[12]<br>OD[13]<br>OD[14]<br>OD[15] | Output | E23<br>F22<br>G21<br>H20<br>G22<br>H21<br>G23<br>H22 | <p>The outgoing data bus (OD[15:8]) carries the STM-1 #2 SONET/SDH frame data in byte serial format.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OD[15] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. OD[8] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. OD[15:8] is set to all-zeros at transport overhead bytes, except for the A1 and A2 framing bytes and the H1 and H2 pointer bytes. Pointer offset is determined by the STP Outgoing Pointer MSB and LSB registers. The OD[15:8] bus is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OD[15:8] bus is unused and all bus signals are invalid.</p> |

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| Pin Name                                                                     | Type   | Pin No.                                              | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------------------------------------------------------|--------|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OD[16]<br>OD[17]<br>OD[18]<br>OD[19]<br>OD[20]<br>OD[21]<br>OD[22]<br>OD[23] | Output | M22<br>M21<br>N23<br>N21<br>N20<br>P23<br>P22<br>P21 | <p>The outgoing data bus (OD[23:16]) carries the STM-1 #3 SONET/SDH frame data in byte serial format.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OD[23] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. OD[16] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. OD[23:16] is set to all-zeros at transport overhead bytes, except for the A1 and A2 framing bytes and the H1 and H2 pointer bytes. Pointer offset is determined by the STP Outgoing Pointer MSB and LSB registers. The OD[23:16] bus is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OD[23:16] bus is unused and all bus signals are invalid.</p> |

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| Pin Name                                                                     | Type   | Pin No.                                                     | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------------------------------------------------------|--------|-------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OD[24]<br>OD[25]<br>OD[26]<br>OD[27]<br>OD[28]<br>OD[29]<br>OD[30]<br>OD[31] | Output | AA12<br>AB12<br>AC13<br>AA13<br>Y13<br>AC14<br>AB14<br>AA14 | <p>The outgoing data bus (OD[31:24]) carries the STM-1 #4 SONET/SDH frame data in byte serial format.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OD[31] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. OD[24] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. OD[31:24] is set to all-zeros at transport overhead bytes, except for the A1 and A2 framing bytes and the H1 and H2 pointer bytes. Pointer offset is determined by the STP Outgoing Pointer MSB and LSB registers. The OD[31:24] bus is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), the OD[31:24] bus is unused and all bus signals are invalid.</p> |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ODP[1]   | Output | F2      | <p>The outgoing data parity #1 (ODP[1]) signal carries the parity of the outgoing STM-4 or STM-1 #1 data stream on OD[7:0] and optionally including the OC1J1V1[1] and the OPL[1] signals. OC1J1V1[1] and OPL[1] can be included in the parity calculation by setting the corresponding INCOC1J1 and INCOPL register bits high, respectively. Odd parity is selected by setting the corresponding OOP register bit high, and even parity is selected by setting the OOP bit low.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), ODP[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), ODP[1] is updated on the rising edge of HSCLK.</p> |
| ODP[2]   | Output | J21     | <p>The outgoing data parity #2 (ODP[2]) signal carries the parity of the outgoing STM-1 #2 data stream on OD[15:8] and optionally including the OC1J1V1[2] and the OPL[2] signals. OC1J1V1[2] and OPL[2] can be included in the parity calculation by setting the corresponding INCOC1J1 and INCOPL register bits high, respectively. Odd parity is selected by setting the corresponding OOP register bit high, and even parity is selected by setting the OOP bit low.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), ODP[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), ODP[2] is invalid.</p>                                     |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ODP[3]   | Output | R23     | <p>The outgoing data parity #3 (ODP[3]) signal carries the parity of the outgoing STM-1 #3 data stream on OD[23:16] and optionally including the OC1J1V1[3] and the OPL[3] signals. OC1J1V1[3] and OPL[3] can be included in the parity calculation by setting the corresponding INCOC1J1 and INCOPL register bits high, respectively. Odd parity is selected by setting the corresponding OOP register bit high, and even parity is selected by setting the OOP bit low.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), ODP[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), ODP[3] is invalid.</p> |
| ODP[4]   | Output | AC15    | <p>The outgoing data parity #4 (ODP[4]) signal carries the parity of the outgoing STM-1 #4 data stream on OD[31:24] and optionally including the OC1J1V1[4] and the OPL[4] signals. OC1J1V1[4] and OPL[4] can be included in the parity calculation by setting the corresponding INCOC1J1 and INCOPL register bits high, respectively. Odd parity is selected by setting the corresponding OOP register bit high, and even parity is selected by setting the OOP bit low.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), ODP[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), ODP[4] is invalid.</p> |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTPL[1]  | Output | H4      | <p>The outgoing tributary payload active #1 (OTPL[1]) signal marks the bytes carrying the tributary payload for the STM-4 or STM-1 #1 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTPL[1] is set high to mark each tributary payload byte of the STM-1 #1 stream on the OD[7:0] bus. OTPL[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTPL[1] is set high to mark each tributary payload byte of the STM-4 stream on the OD[7:0] bus. OTPL[1] is updated on the rising edge of HSCLK.</p> |
| OTPL[2]  | Output | J23     | <p>The outgoing tributary payload active #2 (OTPL[2]) signal marks the bytes carrying the tributary payload for the STM-1 #2 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTPL[2] is set high to mark each tributary payload byte on the OD[15:8] bus. OTPL[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTPL[2] is invalid.</p>                                                                                                                                                            |



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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTPL[3]  | Output | R22     | <p>The outgoing tributary payload active #3 (OTPL[3]) signal marks the bytes carrying the tributary payload for the STM-1 #3 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTPL[3] is set high to mark each tributary payload byte on the OD[23:16] bus. OTPL[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTPL[3] is invalid.</p> |
| OTPL[4]  | Output | AB15    | <p>The outgoing tributary payload active #4 (OTPL[4]) signal marks the bytes carrying the tributary payload for the STM-1 #4 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTPL[4] is set high to mark each tributary payload byte on the OD[31:24] bus. OTPL[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTPL[4] is invalid.</p> |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTV5[1]  | Output | G3      | <p>The outgoing tributary V5 byte #1 (OTV5[1]) signal marks the tributary V5 bytes of the STM-4 or STM-1 #1 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTV5[1] is set high to mark each tributary V5 byte of the STM-1 #1 stream on the OD[7:0] bus. When the outgoing tributary is a TU3, OTV5[1] marks the J1 byte of the TU3. OTV5[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTV5[1] is set high to mark each tributary V5 byte of the STM-4 stream on the OD[7:0] bus. When the outgoing tributary is a TU3, OTV5[1] marks the J1 byte of the TU3. OTV5[1] is updated on the rising edge of HSCLK.</p> |
| OTV5[2]  | Output | K20     | <p>The outgoing tributary V5 byte #2 (OTV5[2]) signal marks the tributary V5 bytes of the STM-1 #2 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTV5[2] is set high to mark each tributary V5 byte on the OD[15:8] bus. When the outgoing tributary is a TU3, OTV5[2] marks the J1 byte of the TU3. OTV5[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTV5[2] is invalid.</p>                                                                                                                                                                                                                                   |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OTV5[3]  | Output | P20     | <p>The outgoing tributary V5 byte #3 (OTV5[3]) signal marks the tributary V5 bytes of the STM-1 #3 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTV5[3] is set high to mark each tributary V5 byte on the OD[23:16] bus. When the outgoing tributary is a TU3, OTV5[3] marks the J1 byte of the TU3. OTV5[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTV5[3] is invalid.</p> |
| OTV5[4]  | Output | Y14     | <p>The outgoing tributary V5 byte #4 (OTV5[4]) signal marks the tributary V5 bytes of the STM-1 #4 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OTV5[4] is set high to mark each tributary V5 byte on the OD[31:24] bus. When the outgoing tributary is a TU3, OTV5[4] marks the J1 byte of the TU3. OTV5[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OTV5[4] is invalid.</p> |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AIS[1]   | Output | G1      | <p>The tributary alarm indication signal output #1 (AIS[1]) marks tributaries on the outgoing STM-4 or STM-1 #1 stream that are in AIS state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), AIS[1] is set high when AIS is inserted in the associated tributary of the STM-1 #1 stream on the OD[7:0] and is set low when the AIS is not inserted. AIS[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), AIS[1] is set high when AIS is inserted in the associated tributary of the STM-4 stream on the OD[7:0] and is set low when the AIS is not inserted. AIS[1] is set low for transport overhead bytes. AIS[1] is updated on the rising edge of HSCLK.</p> |
| AIS[2]   | Output | K21     | <p>The tributary alarm indication signal output #2 (AIS[2]) marks tributaries on the outgoing STM-4 or STM-1 #2 stream that are in AIS state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), AIS[2] is set high when AIS is inserted in the associated tributary on the OD[15:8] and is set low when the AIS is not inserted. AIS[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), AIS[2] is invalid.</p>                                                                                                                                                                                                                                                       |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AIS[3]   | Output | R21     | <p>The tributary alarm indication signal output #3 (AIS[3]) marks tributaries on the outgoing STM-4 or STM-1 #3 stream that are in AIS state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), AIS[3] is set high when AIS is inserted in the associated tributary on the OD[23:16] and is set low when the AIS is not inserted. AIS[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), AIS[3] is invalid.</p> |
| AIS[4]   | Output | AA15    | <p>The tributary alarm indication signal output #4 (AIS[4]) marks tributaries on the outgoing STM-4 or STM-1 #4 stream that are in AIS state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), AIS[4] is set high when AIS is inserted in the associated tributary on the OD[31:24] and is set low when the AIS is not inserted. AIS[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), AIS[4] is invalid.</p> |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDLE[1]  | Output | H3      | <p>The tributary idle indication signal output #1 (IDLE[1]) marks tributaries on the outgoing STM-4 or STM-1 #1 stream that are in idle state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), IDLE[1] is set high when idle code is inserted in the associated tributary of the STM-1 #1 stream on the OD[7:0] and is set low when the idle code is not inserted. IDLE[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), IDLE[1] is set high when idle code is inserted in the associated tributary of the STM-4 stream on the OD[7:0] and is set low when the idle code is not inserted. IDLE[1] is updated on the rising edge of HSCLK.</p> |
| IDLE[2]  | Output | K22     | <p>The tributary idle indication signal output #2 (IDLE[2]) marks tributaries on the outgoing STM-1 #2 stream that are in idle state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), IDLE[2] is set high when idle code is inserted in the associated tributary on the OD[15:8] and is set low when the idle code is not inserted. IDLE[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), IDLE[2] is invalid.</p>                                                                                                                                                                                                                             |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDLE[3]  | Output | T22     | <p>The tributary idle indication signal output #3 (IDLE[3]) marks tributaries on the outgoing STM-1 #3 stream that are in idle state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), IDLE[3] is set high when idle code is inserted in the associated tributary on the OD[23:16] and is set low when the idle code is not inserted. IDLE[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), IDLE[3] is invalid.</p> |
| IDLE[4]  | Output | AB16    | <p>The tributary idle indication signal output #4 (IDLE[4]) marks tributaries on the outgoing STM-1 #4 stream that are in idle state.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), IDLE[4] is set high when idle code is inserted in the associated tributary on the OD[31:24] and is set low when the idle code is not inserted. IDLE[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), IDLE[4] is invalid.</p> |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TPOH[1]  | Output | H2      | <p>The outgoing tributary path overhead byte #1 (TPOH[1]) signal marks the tributary path overhead bytes in the outgoing STM-4 or STM-1 #1 stream. For streams in TU3 mode, the J1, B3, C2, G1, F2, H4, Z3, Z4 and Z5 bytes are marked. For streams out of TU3 mode, V5, J2, Z6 and Z7 bytes are marked.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), TPOH[1] is set high to mark each tributary path overhead byte of the STM-1 #1 stream on the OD[7:0] bus. TPOH[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), TPOH[1] is set high to mark each tributary path overhead byte of the STM-4 stream on the OD[7:0] bus. TPOH[1] is set low for transport overhead bytes. TPOH[1] is updated on the rising edge of HSCLK.</p> |
| TPOH[2]  | Output | K23     | <p>The outgoing tributary path overhead byte #2 (TPOH[2]) signal marks the tributary path overhead bytes in the outgoing STM-1 #2 stream. For streams in TU3 mode, the J1, B3, C2, G1, F2, H4, Z3, Z4 and Z5 bytes are marked. For streams out of TU3 mode, V5, J2, Z6 and Z7 bytes are marked.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), TPOH[2] is set high to mark each tributary path overhead byte on the OD[15:8] bus. TPOH[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), TPOH[2] is invalid.</p>                                                                                                                                                                                                                   |



| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TPOH[3]  | Output | T21     | <p>The outgoing tributary path overhead byte #3 (TPOH[3]) signal marks the tributary path overhead bytes in the outgoing STM-1 #3 stream. For streams in TU3 mode, the J1, B3, C2, G1, F2, H4, Z3, Z4 and Z5 bytes are marked. For streams out of TU3 mode, V5, J2, Z6 and Z7 bytes are marked.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), TPOH[3] is set high to mark each tributary path overhead byte on the OD[23:16] bus. TPOH[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), TPOH[3] is invalid.</p> |
| TPOH[4]  | Output | AC17    | <p>The outgoing tributary path overhead byte #4 (TPOH[4]) signal marks the tributary path overhead bytes in the outgoing STM-1 #4 stream. For streams in TU3 mode, the J1, B3, C2, G1, F2, H4, Z3, Z4 and Z5 bytes are marked. For streams out of TU3 mode, V5, J2, Z6 and Z7 bytes are marked.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), TPOH[4] is set high to mark each tributary path overhead byte on the OD[31:24] bus. TPOH[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), TPOH[4] is invalid.</p> |

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| Pin Name   | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OC1J1V1[1] | Output | D3      | <p>The outgoing composite frame pulse #1 (OC1J1V1[1]) marks the transport, synchronous payload envelope and tributary multiframe frame boundaries on the outgoing STM-4 or STM-1 #1 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OC1J1V1[1] pulses high to mark the first C1 byte of the STM-1 #1 transport envelope frame on the OD[7:0] bus. It also pulses high to mark the J1 byte(s). When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), the AU3/AU4 pointer offset (J1 position relative to C1) is determined by the corresponding STP Outgoing Pointer MSB and LSB registers. Optionally, OC1J1V1[1] also marks the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the corresponding OV1EN register bit is set high. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), the J1 and V1 byte position pulses are delayed versions from the IC1J1[1] input. OC1J1V1[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OC1J1V1[1] pulses high to mark the first C1 byte of the STM-4 transport envelope frame on the OD[7:0] bus. It also pulses high to mark the STM-1 J1 bytes. When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), the AU3/AU4 pointer offset (J1 position relative to C1) of each STM-1 is determined by the corresponding STP Outgoing Pointer MSB and LSB registers. Optionally, OC1J1V1[1] also marks the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the corresponding OV1EN</p> |

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| Pin Name   | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|            |        |         | <p>register bit is set high. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), the J1 and V1 byte position pulses are delayed versions from the IC1J1[1] input. OC1J1V1[1] is updated on the rising edge of HSCLK.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| OC1J1V1[2] | Output | F21     | <p>The outgoing composite frame pulse #2 (OC1J1V1[2]) marks the transport, synchronous payload envelope and tributary multiframe frame boundaries on the outgoing STM-1 #2 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OC1J1V1[2] pulses high to mark the first C1 byte of the STM-1 #2 transport envelope frame on the OD[15:8] bus. It also pulses high to mark the J1 byte(s). When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), the AU3/AU4 pointer offset (J1 position relative to C1) is determined by the corresponding STP Outgoing Pointer MSB and LSB registers. Optionally, OC1J1V1[2] also marks the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the corresponding OV1EN register bit is set high. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), the J1 and V1 byte position pulses are delayed versions from the IC1J1[2] input. OC1J1V1[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OC1J1V1[2] is invalid.</p> |

| Pin Name   | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OC1J1V1[3] | Output | L22     | <p>The outgoing composite frame pulse #3 (OC1J1V1[3]) marks the transport, synchronous payload envelope and tributary multiframe frame boundaries on the outgoing STM-1 #3 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OC1J1V1[3] pulses high to mark the first C1 byte of the STM-1 #3 transport envelope frame on the OD[23:16] bus. It also pulses high to mark the J1 byte(s). When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), the AU3/AU4 pointer offset (J1 position relative to C1) is determined by the corresponding STP Outgoing Pointer MSB and LSB registers. Optionally, OC1J1V1[3] also marks the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the corresponding OV1EN register bit is set high. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), the J1 and V1 byte position pulses are delayed versions from the IC1J1[3] input. OC1J1V1[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OC1J1V1[3] is invalid.</p> |

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| Pin Name   | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OC1J1V1[4] | Output | AB11    | <p>The outgoing composite frame pulse #4 (OC1J1V1[4]) marks the transport, synchronous payload envelope and tributary multiframe frame boundaries on the outgoing STM-1 #4 stream.</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OC1J1V1[4] pulses high to mark the first C1 byte of the STM-1 #4 transport envelope frame on the OD[31:24] bus. It also pulses high to mark the J1 byte(s). When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), the AU3/AU4 pointer offset (J1 position relative to C1) is determined by the corresponding STP Outgoing Pointer MSB and LSB registers. Optionally, OC1J1V1[4] also marks the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the corresponding OV1EN register bit is set high. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), the J1 and V1 byte position pulses are delayed versions from the IC1J1[4] input. OC1J1V1[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OC1J1V1[4] is invalid.</p> |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OPL[1]   | Output | E4      | <p>The outgoing payload active #1 (OPL[1]) signal identifies synchronous payload envelope bytes on the outgoing STM-4 or STM-1 #1 stream. When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), OPL[1] is set high to mark synchronous payload envelop bytes and set low to mark transport overhead bytes. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), OPL[1] is a delayed version of IPL[1].</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OPL[1] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OPL[1] is updated on the rising edge of HSCLK.</p> |
| OPL[2]   | Output | G20     | <p>The outgoing payload active #2 (OPL[2]) signal identifies synchronous payload envelope bytes on the outgoing STM-1 #2 stream. When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), OPL[2] is set high to mark synchronous payload envelop bytes and set low to mark transport overhead bytes. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), OPL[2] is a delayed version of IPL[2].</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OPL[2] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OPL[2] is invalid.</p>                                      |

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| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OPL[3]   | Output | L23     | <p>The outgoing payload active #3 (OPL[3]) signal identifies synchronous payload envelope bytes on the outgoing STM-1 #3 stream. When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), OPL[3] is set high to mark synchronous payload envelop bytes and set low to mark transport overhead bytes. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), OPL[3] is a delayed version of IPL[3].</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OPL[3] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OPL[3] is invalid.</p> |
| OPL[4]   | Output | AC11    | <p>The outgoing payload active #4 (OPL[4]) signal identifies synchronous payload envelope bytes on the outgoing STM-1 #4 stream. When AU3/TUG3 bypass is disabled (TUGEN set high and TUGBYP set low), OPL[4] is set high to mark synchronous payload envelop bytes and set low to mark transport overhead bytes. When AU3/TUG3 bypass is enabled (TUGEN set low or TUGBYP set high), OPL[4] is a delayed version of IPL[4].</p> <p>In outgoing STM-1 (STS-3) interface mode (OHSMODEB set high), OPL[4] is updated on the rising edge of SCLK.</p> <p>In outgoing STM-4 (STS-12) interface mode (OHSMODEB set low), OPL[4] is invalid.</p> |

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| Pin Name                   | Type   | Pin No.        | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POHCK                      | Output | L2             | The tributary path overhead clock (POHCK) signal provides timing to sample the extracted tributary path overhead stream and the receive alarm port for STM-1 #1, #2, #3 and #4. POHCK is a nominally 9.72 MHz clock. The POH[12:1], POHEN[12:1], POHFP[12:1] and RAD[4:1] outputs are updated on the falling edge of POHCK.                                                                                                                                                                                                                                                                                                                                          |
| POH[1]<br>POH[2]<br>POH[3] | Output | L4<br>M3<br>P2 | The tributary path overhead (POH[3:1]) signals contain the tributary path overhead bytes (V5, J2, Z6 and Z7) extracted from the incoming STM-1 #1 stream. POH[1], POH[2] and POH[3] contain the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POH[1], POH[2] and POH[3] contain the tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. All four tributary overhead bytes of each tributary is shifted out once per payload frame. The corresponding POHEN signal is set high to identify overhead bytes that are presented for the first time. Each POH signal is updated on the falling edge of POHCK. |



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| Pin Name                   | Type   | Pin No.           | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------|--------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POH[4]<br>POH[5]<br>POH[6] | Output | A21<br>D21<br>D22 | The tributary path overhead (POH[6:4]) signals contain the tributary path overhead bytes (V5, J2, Z6 and Z7) extracted from the incoming STM-1 #2 stream. POH[4], POH[5] and POH[6] contain the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POH[4], POH[5] and POH[6] contain the tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. All four tributary overhead bytes of each tributary is shifted out once per payload frame. The corresponding POHEN signal is set high to identify overhead bytes that are presented for the first time. Each POH signal is updated on the falling edge of POHCK. |
| POH[7]<br>POH[8]<br>POH[9] | Output | V22<br>V21<br>W21 | The tributary path overhead (POH[9:7]) signals contain the tributary path overhead bytes (V5, J2, Z6 and Z7) extracted from the incoming STM-1 #3 stream. POH[7], POH[8] and POH[9] contain the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POH[7], POH[8] and POH[9] contain the tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. All four tributary overhead bytes of each tributary is shifted out once per payload frame. The corresponding POHEN signal is set high to identify overhead bytes that are presented for the first time. Each POH signal is updated on the falling edge of POHCK. |

| Pin Name                         | Type   | Pin No.            | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POH[10]<br>POH[11]<br>POH[12]    | Output | AB8<br>Y10<br>AC10 | The tributary path overhead (POH[12:10]) signals contain the tributary path overhead bytes (V5, J2, Z6 and Z7) extracted from the incoming STM-1 #4 stream. POH[10], POH[11] and POH[12] contain the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POH[10], POH[11] and POH[12] contain the tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. All four tributary overhead bytes of each tributary is shifted out once per payload frame. The corresponding POHEN signal is set high to identify overhead bytes that are presented for the first time. Each POH signal is updated on the falling edge of POHCK. |
| POHFP[1]<br>POHFP[2]<br>POHFP[3] | Output | K1<br>L1<br>N1     | The tributary path overhead frame pulse (POHFP[3:1]) signals may be used to locate the individual path overhead bits of each tributary for the corresponding STS-1 (TUG3) in the incoming STM-1 #1 stream. Each POHFP signal is set high to mark bit 1 (the most significant bit) of the V5 byte of the first tributary. POHFP[1], POHFP[2] and POHFP[3] identify frame boundaries of the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHFP[1], POHFP[2] and POHFP[3] identify frame boundaries of TUG3 #1, #2 and #3, respectively. Each POHFP signal is updated on the falling edge of POHCK.                                 |

| Pin Name                         | Type   | Pin No.           | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------|--------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POHFP[4]<br>POHFP[5]<br>POHFP[6] | Output | B20<br>C20<br>C23 | The tributary path overhead frame pulse (POHFP[6:4]) signals may be used to locate the individual path overhead bits of each tributary for the corresponding STS-1 (TUG3) in the incoming STM-1 #2 stream. Each POHFP signal is set high to mark bit 1 (the most significant bit) of the V5 byte of the first tributary. POHFP[4], POHFP[5] and POHFP[6] identify frame boundaries of the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHFP[4], POHFP[5] and POHFP[6] identify frame boundaries of TUG3 #1, #2 and #3, respectively. Each POHFP signal is updated on the falling edge of POHCK. |
| POHFP[7]<br>POHFP[8]<br>POHFP[9] | Output | U21<br>U20<br>Y23 | The tributary path overhead frame pulse (POHFP[9:7]) signals may be used to locate the individual path overhead bits of each tributary for the corresponding STS-1 (TUG3) in the incoming STM-1 #3 stream. Each POHFP signal is set high to mark bit 1 (the most significant bit) of the V5 byte of the first tributary. POHFP[7], POHFP[8] and POHFP[9] identify frame boundaries of the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHFP[7], POHFP[8] and POHFP[9] identify frame boundaries of TUG3 #1, #2 and #3, respectively. Each POHFP signal is updated on the falling edge of POHCK. |

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| Pin Name                            | Type   | Pin No.            | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------------|--------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POHFP[10]<br>POHFP[11]<br>POHFP[12] | Output | AA8<br>AB9<br>AA10 | The tributary path overhead frame pulse (POHFP[12:10]) signals may be used to locate the individual path overhead bits of each tributary for the corresponding STS-1 (TUG3) in the incoming STM-1 #4 stream. Each POHFP signal is set high to mark bit 1 (the most significant bit) of the V5 byte of the first tributary. POHFP[10], POHFP[11] and POHFP[12] identify frame boundaries of the tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHFP[10], POHFP[11] and POHFP[12] identify frame boundaries of TUG3 #1, #2 and #3, respectively. Each POHFP signal is updated on the falling edge of POHCK.                                                                                                                                                    |
| POHEN[1]<br>POHEN[2]<br>POHEN[3]    | Output | L3<br>M2<br>P3     | The tributary path overhead enable (POHEN[3:1]) signals may be used to identify tributary path overhead bytes that are being presented on the corresponding POH stream of STM-1 #1 for the first time. Each POHEN signal is set high when a fresh overhead byte is available on the corresponding POH stream. POHEN is set low when the tributary path overhead byte available on the corresponding POH stream has already been shifted out in a previous frame. POHEN[1], POHEN[2] and POHEN[3] identify the status of tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHEN[1], POHEN[2] and POHEN[3] identify the status of tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. Each POHEN signal is updated on the falling edge of POHCK. |

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| Pin Name                         | Type   | Pin No.           | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------------------|--------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POHEN[4]<br>POHEN[5]<br>POHEN[6] | Output | D19<br>E20<br>E21 | The tributary path overhead enable (POHEN[6:4]) signals may be used to identify tributary path overhead bytes that are being presented on the corresponding POH stream of STM-1 #2 for the first time. Each POHEN signal is set high when a fresh overhead byte is available on the corresponding POH stream. POHEN is set low when the tributary path overhead byte available on the corresponding POH stream has already been shifted out in a previous frame. POHEN[4], POHEN[5] and POHEN[6] identify the status of tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHEN[4], POHEN[5] and POHEN[6] identify the status of tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. Each POHEN signal is updated on the falling edge of POHCK. |
| POHEN[7]<br>POHEN[8]<br>POHEN[9] | Output | W23<br>W22<br>Y22 | The tributary path overhead enable (POHEN[9:7]) signals may be used to identify tributary path overhead bytes that are being presented on the corresponding POH stream of STM-1 #3 for the first time. Each POHEN signal is set high when a fresh overhead byte is available on the corresponding POH stream. POHEN is set low when the tributary path overhead byte available on the corresponding POH stream has already been shifted out in a previous frame. POHEN[7], POHEN[8] and POHEN[9] identify the status of tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHEN[7], POHEN[8] and POHEN[9] identify the status of tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. Each POHEN signal is updated on the falling edge of POHCK. |

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| Pin Name                            | Type   | Pin No.           | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------------------------|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POHEN[10]<br>POHEN[11]<br>POHEN[12] | Output | AA9<br>AC9<br>Y11 | The tributary path overhead enable (POHEN[12:10]) signals may be used to identify tributary path overhead bytes that are being presented on the corresponding POH stream of STM-1 #4 for the first time. Each POHEN signal is set high when a fresh overhead byte is available on the corresponding POH stream. POHEN is set low when the tributary path overhead byte available on the corresponding POH stream has already been shifted out in a previous frame. POHEN[10], POHEN[11] and POHEN[12] identify the status of tributary path overhead bytes from STS-1 (AU3) #1, #2 and #3, respectively. In AU4 mode, POHEN[10], POHEN[11] and POHEN[12] identify the status of tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. Each POHEN signal is updated on the falling edge of POHCK. |
| RAD[1]                              | Output | K3                | The receive alarm port #1 (RAD[1]) contains the tributary path BIP error count, the RDI status and the PDI status of each tributary in the STM-1 #1. RAD[1] is updated on the falling edge of POHCK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RAD[2]                              | Output | C19               | The receive alarm port #2 (RAD[2]) contains the tributary path BIP error count, the RDI status and the PDI status of each tributary in the STM-1 #2. RAD[2] is updated on the falling edge of POHCK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RAD[3]                              | Output | T20               | The receive alarm port #3 (RAD[3]) contains the tributary path BIP error count, the RDI status and the PDI status of each tributary in the STM-1 #3. RAD[3] is updated on the falling edge of POHCK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| Pin Name | Type   | Pin No. | Function                                                                                                                                                                                                                                                                                                                                  |
|----------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RAD[4]   | Output | AC7     | The receive alarm port #4 (RAD[4]) contains the tributary path BIP error count, the RDI status and the PDI status of each tributary in the STM-1 #4. RAD[4] is updated on the falling edge of POHCK.                                                                                                                                      |
| MBEB     | Input  | C6      | The active low Motorola bus enable (MBEB) signal configures the TUPP+622 for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the TUPP+622 is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor. |
| CSB      | Input  | A4      | The active low chip select (CSB) signal is low during TUPP+622 register accesses. If CSB is not required (i.e., register accesses are controlled by using the RDB/E and WRB/RWB signals only), CSB must be connected to an inverted version of RSTB.                                                                                      |
| RDB/     | Input  | B6      | The active low read enable (RDB) signal is low during TUPP+622 register read accesses while in Intel bus mode. The TUPP+622 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.                                                                                                                  |
| E        |        |         | The active high external access (E) signal is high during TUPP+622 register access while in Motorola bus mode.                                                                                                                                                                                                                            |

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| Pin Name                                                     | Type  | Pin No.                                              | Function                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------------------------------------------|-------|------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WRB/                                                         | Input | C7                                                   | The active low write strobe (WRB) signal is low during a TUPP+622 register write accesses while in Intel bus mode. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.                                                                                                                                       |
| RWB                                                          |       |                                                      | The read/write select (RWB) signal selects between TUPP+622 register read and write accesses while in Motorola bus mode. The TUPP+622 drives the D[7:0] bus with the contents of the addressed register while CSB is low and RWB and E are high. The D[7:0] bus contents are clocked into the addressed register on the falling E edge while CSB and RWB are low. |
| D[0]<br>D[1]<br>D[2]<br>D[3]<br>D[4]<br>D[5]<br>D[6]<br>D[7] | I/O   | A11<br>B12<br>C12<br>A13<br>B13<br>C13<br>D13<br>A14 | The bidirectional data bus D[7:0] is used during TUPP+622 register read and write accesses.                                                                                                                                                                                                                                                                       |



| Pin Name                                                                                                | Type  | Pin No.                                                                         | Function                                                                                                                                                                                                                                                                 |
|---------------------------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[0]<br>A[1]<br>A[2]<br>A[3]<br>A[4]<br>A[5]<br>A[6]<br>A[7]<br>A[8]<br>A[9]<br>A[10]<br>A[11]<br>A[12] | Input | D8<br>B7<br>C8<br>A7<br>B8<br>C9<br>B9<br>D10<br>A9<br>C10<br>B10<br>A10<br>D11 | The address bus A[13:0] selects specific registers during TUPP+622 register accesses.                                                                                                                                                                                    |
| A[13]/TRS                                                                                               |       | C11                                                                             | The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.                                                                           |
| RSTB                                                                                                    | Input | D7                                                                              | The active low reset (RSTB) signal provides an asynchronous TUPP+622 reset. RSTB is a Schmitt triggered input with an integral pull up resistor.                                                                                                                         |
| ALE                                                                                                     | Input | A5                                                                              | The address latch enable (ALE) is active high and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the TUPP+622 to interface to a multiplexed address/data bus. ALE has an integral pull up resistor. |

| Pin Name | Type      | Pin No. | Function                                                                                                                                                                                                                                               |
|----------|-----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INTB     | OD Output | C14     | The active low interrupt (INTB) signal goes low when a TUPP+622 interrupt source is active. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.                                     |
| TCK      | Input     | C5      | The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TCK has an integral pull up resistor.                                                                                 |
| TMS      | Input     | C4      | The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.                                        |
| TDI      | Input     | B4      | The test data input (TDI) signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.                                                              |
| TDO      | Tristate  | A3      | The test data output (TDO) signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output that is always tristated except when scanning of data is in progress. |
| TRSTB    | Input     | D5      | The active low test reset (TRSTB) signal provides an asynchronous test access port reset. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence.                                   |

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| Pin Name | Type  | Pin No. | Function                                                                                       |
|----------|-------|---------|------------------------------------------------------------------------------------------------|
| VDDI1    | Power | G2      | The core power (VDDI1 – VDDI16) pins should be connected to a well decoupled +2.5 V DC supply. |
| VDDI2    |       | K2      |                                                                                                |
| VDDI3    |       | N2      |                                                                                                |
| VDDI4    |       | U2      |                                                                                                |
| VDDI5    |       | AB7     |                                                                                                |
| VDDI6    |       | AB10    |                                                                                                |
| VDDI7    |       | AB13    |                                                                                                |
| VDDI8    |       | AB17    |                                                                                                |
| VDDI9    |       | U22     |                                                                                                |
| VDDI10   |       | N22     |                                                                                                |
| VDDI11   |       | J22     |                                                                                                |
| VDDI12   |       | E22     |                                                                                                |
| VDDI13   |       | B17     |                                                                                                |
| VDDI14   |       | B14     |                                                                                                |
| VDDI15   |       | B11     |                                                                                                |
| VDDI16   |       | B5      |                                                                                                |

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| Pin Name  | Type  | Pin No.                                                                                                                                                                                                                                       | Function                                                                                                |
|-----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|
| VDD[35:0] | Power | A1<br>A23<br>AA3<br>AA21<br>AB2<br>AB22<br>AC1<br>AC23<br>B2<br>B22<br>C3<br>C21<br>D4<br>D6<br>D9<br>D12<br>D15<br>D18<br>D20<br>F4<br>F20<br>J4<br>J20<br>M4<br>M20<br>R4<br>R20<br>V4<br>V20<br>Y4<br>Y6<br>Y9<br>Y12<br>Y15<br>Y18<br>Y20 | The pad ring switching power (VDD[35:0]) pins should be connected to a well decoupled +3.3 V DC supply. |

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| Pin Name  | Type   | Pin No.                                                                                                                                                                                                                                              | Function                                                                                                                                                                            |
|-----------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSS[35:0] | Ground | A2<br>A6<br>A8<br>A12<br>A16<br>A18<br>A22<br>AA2<br>AA22<br>AB1<br>AB3<br>AB21<br>AB23<br>AC2<br>AC6<br>AC8<br>AC12<br>AC16<br>AC18<br>AC22<br>B1<br>B3<br>B21<br>B23<br>C2<br>C22<br>F1<br>F23<br>H1<br>H23<br>M1<br>M23<br>T1<br>T23<br>V1<br>V23 | The pad ring and core power ground (VSS[35:0]) pins should be connected to the common ground plane of the DC supplies connected to the VDD[35:0] and the VDDI1 – VDDI16 power pins. |
| NC1       |        | Y7                                                                                                                                                                                                                                                   | Reserved. Must not be connected.                                                                                                                                                    |

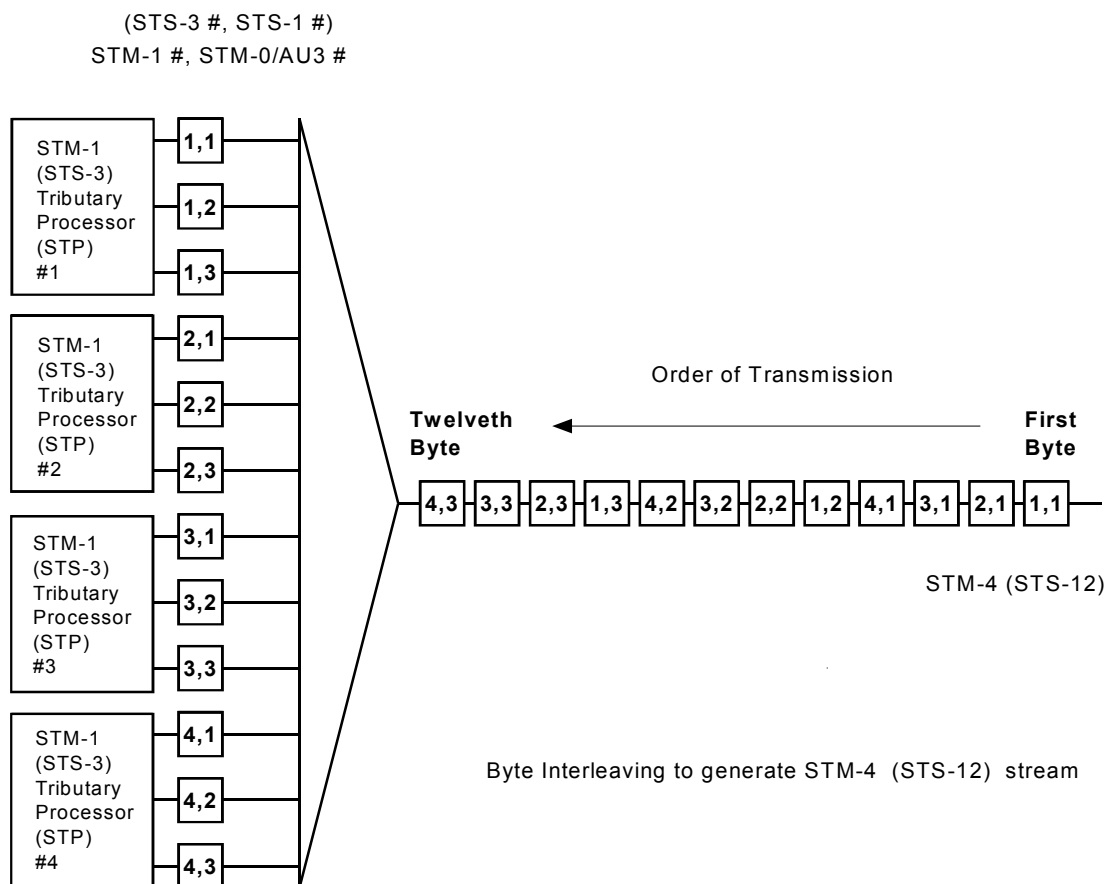
| Pin Name | Type | Pin No. | Function                         |
|----------|------|---------|----------------------------------|
| NC2      |      | Y16     | Reserved. Must not be connected. |

**Notes on Pin Description:**

1. All TUPP+622 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.
2. All TUPP+622 digital outputs and bidirectionals have 8 mA drive capability.
3. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.
4. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
5. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

## **10 FUNCTIONAL DESCRIPTION**

The TUPP+622 consists of four independent STM-1 (STS-3) tributary processors (STP) each having the equivalent functionality of a TUPP-PLUS (PM5362) device. Each STP consists of three sets of tributary payload processor (VTPP), tributary path overhead processor (RTOP) and tributary trace buffer (RTTB). Each set of VTPP, RTOP and RTTB is capable of processing all the tributaries in a TUG3, AU3 or STS-1. Four STP's, #1, #2, #3 and #4 process the STM-1 #1, #2, #3 and #4 streams, respectively. In the STM-1 (STS-3) interface mode, the incoming STM-1 #1, #2, #3 and #4 streams are sourced from the ID[7:0], ID[15:8], ID[23:16] and ID[31:24] buses, respectively. The outgoing STM-1 #1, #2, #3 and #4 streams are provided on the OD[7:0], OD[15:8], OD[23:16] and OD[31:24] buses, respectively. In the STM-4 (STS-12) interface mode, the byte-interleaved incoming STM-1 (#1, #2, #3, #4) streams of an STM-4 are sourced from the ID[7:0] bus and the outgoing STM-1 (#1, #2, #3, #4) streams are byte-interleaved and provided on the OD[7:0] bus as an STM-4 stream. The incoming and outgoing interface modes may be configured independently. The incoming or outgoing byte interleaved order corresponds to the STM-4 (STS-12) order of byte transmission as shown in the diagram below. The VC (SPE) columns or bytes are labeled using an STM-1 (STS-3) group and AU3 (STS-1) sub-group numbering scheme. Distribution of incoming STM-1 streams to the STP's is performed by the Input Bus Demultiplexer. Consolidation of outgoing STM-1 streams from the STP's is performed by the Output Bus Multiplexer.

**Figure 4 - STM-4 (STS-12) Order of Byte Transmission**


## 10.1 Input Bus Demultiplexer

In STM-4 (STS-12) interface mode, the first stage of the input bus demultiplexer captures data sampled on the ID[7:0] bus and distributes this data as four STM-1 (STS-3) streams to the corresponding four STM-1 (STS-3) tributary processors (STP). In STM-1 (STS-3) interface mode, the first stage of the input bus demultiplexer is bypassed and the STM-1 (STS-3) data on the ID[7:0], ID[15:8], ID[23:16] and ID[31:24] is forwarded to the respective STP's. The input STM-1 (STS-3) demultiplexing logic of each STP provides the second stage of the input bus demultiplexer. It distributes the STS-1 (AU3) or TUG3 data to the three tributary payload processors within the STP.



The input bus demultiplexer also provides timing signals for the other blocks within the STP. Frame alignment signals for the incoming data stream, IC1J1, ITMF, IPL, ITV5 and ITPL are sampled, buffered and distributed to the associated tributary payload processors (VTPPs). In order to have synchronous operation of the VTPPs with a single clock, the incoming data and control signals may be delayed by a number of system clock cycles before distribution to the VTPPs. The delay is used to align the incoming data with the outgoing data at each VTPP. The amount of delay is adjusted such that the separation of the incoming STS/AU frame and the outgoing frame at each VTPP appears to be in multiples of three SCLK or twelve HSCLK periods.

When configured for AU4 mode, the input bus demultiplexer provides the necessary timing coordination between the three tributary payload processors in the STP. The single J1 byte marker input on IC1J1 is retimed and distributed to each of the three tributary payload processors in the STP. The tributary multiframe detected by VTPP #1 is distributed to the two other VTPPs, as VTPP #1 is the only one receiving a valid H4 byte within the STP.

## **10.2 Output Bus Multiplexer**

The first stage of the output bus multiplexer is formed by the output multiplexing logic of each STP. It gathers payload data from the three tributary payload processors within the STP and multiplexes this data into an STM-1 (STS-3) payload data stream. It also multiplexes signals from each tributary payload processor that mark tributary SPEs and tributary V5 bytes into the respective STM-1 (STS-3) signals. The extracted tributary path overhead serial signals (POH[12:1], POHFP[12:1], POHEN[12:1], POHCK and RAD[4:1]) are buffered by this stage of the output bus multiplexer block.

The output bus multiplexer also provides timing signals for other blocks within an STP. Frame alignment signal for the outgoing data stream, OTMF, is sampled, buffered and distributed to the tributary payload processors (VTPPs), tributary path overhead processors (RTOPs) and tributary trace buffers (RTTBs) of the STP. The output bus multiplexer contains a four frame counter that will flywheel in the absence of an active OTMF input, internally generating tributary multiframe timing for the outgoing STM-1 data stream. The output bus multiplexer will internally generate J1 and SPE timing for the outgoing STM-1 data stream at the STS-1 (AU3) or AU4 level. The transport and payload frame boundaries are reported on the corresponding OC1J1V1 and OPL outputs. This timing drives the outputs of the three VTPPs, RTOPs and RTTBs within the STP.

In STM-4 (STS-12) interface mode, the second stage of the output bus multiplexer gathers the STM-1 (STS-3) payload data from the four STP's and multiplexes this data onto the OD[7:0] bus. It also multiplexes the STM-1 tributary SPE and tributary V5 byte indication signals from the STP's onto the OTPL[1] and OTV5[1] signals, respectively. In STM-1 (STS-3) interface mode, the second stage of the output bus is bypassed and the STM-1 (STS-3) payload data from the four STP's are provided directly to the respective OD[7:0], OD[15:8], OD[23:16] and OD[31:24] buses. Similarly, the STM-1 tributary SPE and tributary V5 byte indication signals from the STP's are provided directly to the respective OTPL[4:1] and OTV5[4:1] signals.

### **10.3 Tributary Payload Processor (VTPP)**

Each tributary payload processor (VTPP) processes the tributaries within an STS-1, AU3, or TUG3. Each VTPP can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each VTPP ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or equivalently all TU11s).

#### **10.3.1 Clock Generator**

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary payload processor. The overall design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary payload processor.

#### **10.3.2 Incoming Timing Generator**

The incoming timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the VTPP (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The H4 byte is identified for the incoming multiframe detector so that it can determine the incoming tributary multiframe boundaries. The identification of specific tributaries allows the pointer interpreter to be time-sliced across the mix of tributaries present in the incoming data

stream. The identification of the V1-V3 bytes of VTs, or TUs (or H1-H3 bytes in the case of TU3s) allows the pointer interpreter to function.

### 10.3.3 Incoming Multiframe Detector

The multiframe alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, 11 in the two least significant bits. If an unexpected value is detected, the primary multiframe will be kept, and a second multiframe process will, in parallel, check for a phase shift. The primary process will enter out of multiframe state (OOM). A new multiframe alignment is chosen, and OOM state is exited when four consecutive correct multiframe patterns are detected. Loss of multiframe (LOM) is declared after residing in the OOM state at the ninth H4 byte without re-alignment. In counting to nine, the out of sequence H4 byte that triggered the transition to the OOM state is counted as the first. A new multiframe alignment is chosen, and LOM state is exited when four consecutive correct multiframe patterns are detected. Changes in multiframe alignments are detected and reported.

### 10.3.4 Pointer Interpreter

The pointer interpreter is a time-sliced state machine that can process up to 28 independent tributaries. The state vector is saved in RAM as directed by the incoming timing generator. The pointer interpreter processes the incoming tributary pointers such that all bytes within the tributary synchronous payload envelope can be identified and written into the unique payload first-in first-out buffer for the tributary in question. A marker that tags the V5 byte (or J1 byte in the case of a TU3) is passed through the payload buffer. The incoming timing generator directs the pointer interpreter to the correct payload buffer for the tributary being processed.

The pointer interpreter processes the incoming pointers (V1/V2 or H1/H2 in TU3 mode) as specified in the references. The pointer value is used to determine the location of the tributary path overhead byte (V5 or J1 in TU3) in the incoming TUG3 or STS-1 (AU3) stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined (as shown in Figure 5):

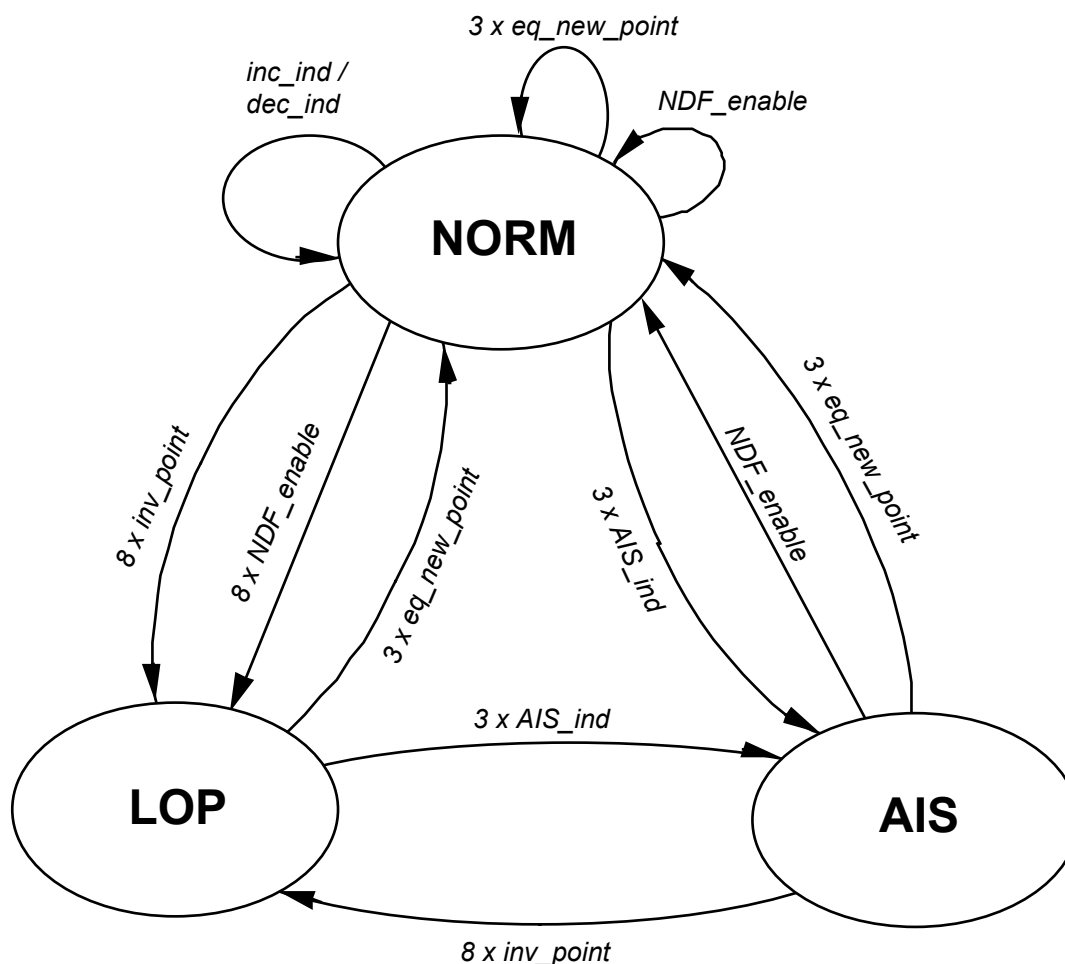
NORM\_state (NORM)

AIS\_state (AIS)

### LOP\_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM\_state to the AIS\_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER. The only transition on a single event is the one from the AIS\_state to the NORM\_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP\_state.

**Figure 5 - Pointer Interpretation State Diagram**



The following events (indications) are defined

|              |                                                                                                                                                   |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| norm_point : | disabled NDF + ss + offset value equal to active offset                                                                                           |
| NDF_enable:  | enabled NDF + ss + offset value in range for the configured tributary type                                                                        |
| AIS_ind:     | H1 = 'hFF, H2 = 'hFF                                                                                                                              |
| inc_ind:     | disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago |
| dec_ind:     | disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago |
| inv_point:   | not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)                                     |
| new_point:   | disabled_NDF + ss + offset value in range for the configured tributary type but not equal to active offset                                        |
| inc_req:     | disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted                                                                  |
| dec_req:     | disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted                                                                  |

### Notes:

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM\_state and is undefined in the other states.
2. Enabled NDF is defined as the following bit patterns:  
1001, 0001, 1101, 1011, 1000.
3. Disabled NDF is defined as the following bit patterns:  
0110, 1110, 0010, 0100, 0111.

4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an `inv_point` indication.
5. The legal range of pointer values for the five supported tributary types are:  
  
VT1.5 : 0 .. 103  
VT2 : 0 .. 139  
VT3 : 0 .. 211  
VT6 : 0 .. 427  
TU3 : 0 .. 764
6. The requirement for previous `NDF_enable`, `inc_ind` or `dec_ind` be more than 3 frames ago may be optionally disabled.
7. `New_point` is also an `inv_point`.
8. The requirement for 3 consecutive AIS indications may be optionally disabled.

The transitions indicated in the state diagram are defined as follows:

`inc_ind/dec_ind`: offset adjustment (increment or decrement indication)

3 x `eq_new_point`: three consecutive equal `new_point` indications

`NDF_enable`: single `NDF_enable` indication

3 x `AIS_ind`: three consecutive AIS indications

8 x `inv_point`: eight consecutive `inv_point` indications

8 x `NDF_enable` eight consecutive `NDF_enable` indications

#### Notes:

1. The transitions from `NORM_state` to `NORM_state` do not represent state changes but imply offset changes.
2. 3 x `eq_new_point` takes precedence over other events.

3. All three offset values received in 3 x eq\_new\_point must be identical.
4. "consecutive event counters" are reset to zero on a change of state.

The pointer interpreter block detects loss of pointer (LOP) in the incoming tributaries. LOP is declared on entry to the LOP\_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. LOP is removed when the same valid pointer with normal NDF is detected for three consecutive frames. Incoming tributary path AIS (pointer bytes set to all ones) does not cause entry into the LOP state.

The pointer interpreter block also detects tributary path AIS in the incoming tributaries. PAIS is declared on entry to the AIS\_state after three consecutive AIS indications. PAIS is removed when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid pointer with NDF enabled is detected.

The pointer interpreter may be bypassed. External logic upstream would identify tributary payload bytes and tributary payload frame boundaries via the ITPL and ITV5 signals, respectively. Loss of pointer and tributary path AIS alarm detection will be disabled. Alarm conditions are conveyed by the IAIS input signal.

### 10.3.5 Payload Buffer

The payload buffer is a bank FIFO buffers. It is synchronous in operation and is based on a time-sliced RAM. The three 19.44 MHz clock cycles in each 6.48 MHz period are shared between the read and write operations. The pointer interpreter writes tributary payload data and the V5 (or TU3 J1) tag into the payload buffer. A 16 byte FIFO buffer is provided for each of the (up to 28) tributaries. Address information is also passed through the payload buffer to allow FIFO fill status to be determined by the pointer generator.

### 10.3.6 Outgoing Timing Generator

The outgoing timing generator identifies the outgoing tributary byte being processed. Based on the configuration of the VTPP, the outgoing timing generator effectively constructs the STS-1 SPE, VC3, or VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and bytes that carry specific tributaries. The identification of specific tributaries allows the pointer generator to be time-sliced across the mix of tributaries to be sourced

in the outgoing data stream. The identification of the V1-V3 bytes of VTs, or TUs (H1-H3 bytes of TU3s) allows the pointer generator to function.

The sequence of H4 bytes is generated by each tributary payload processor and inserted into the outgoing administrative units. The six most significant bits of H4 are set to logic 1. The sequence of the remaining two H4 bits is determined by the corresponding OTMF input.

### 10.3.7 Pointer Generator

The pointer generator block generates the tributary pointers (V1/V2 or H1/H2 in TU3 mode) as specified in the references. The pointer value is used to determine the location of the tributary path overhead byte (V5 or J1 in TU3 mode) on the outgoing stream. The algorithm can be modeled by a finite state machine. Within the pointer generator algorithm, five states are defined (as shown in Figure 6):

NORM\_state (NORM)

AIS\_state (AIS)

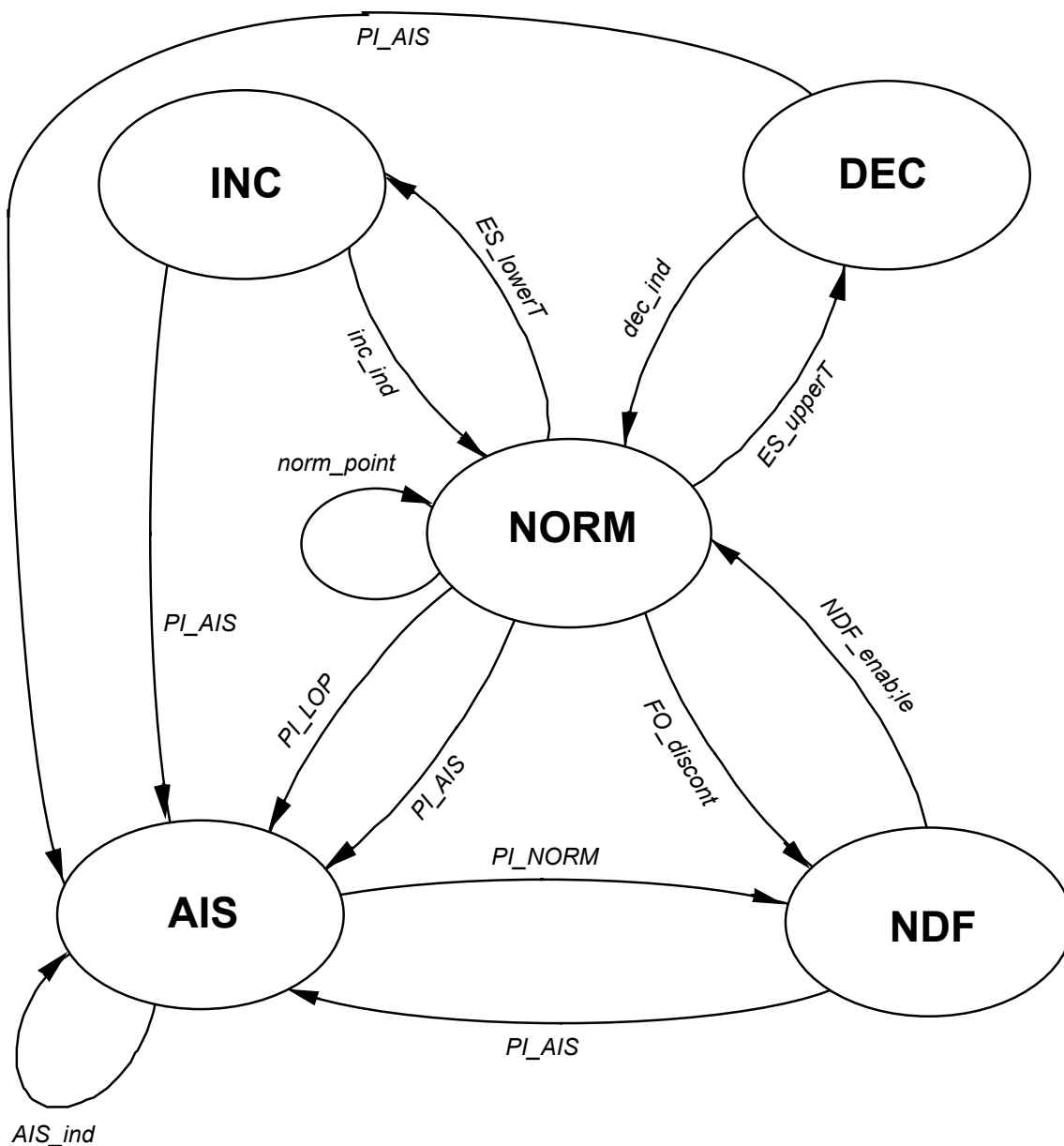
NDF\_state (NDF)

INC\_state (INC)

DEC\_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the payload buffer block. The transition to/from the AIS state are controlled by the pointer interpreter block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.



**Figure 6 - Pointer Generation State Diagram**


The following events, indicated in the state diagram (Figure 6), are defined:

|             |                                                                                                               |
|-------------|---------------------------------------------------------------------------------------------------------------|
| ES_lowerT:  | ES filling is below the lower threshold + previous inc_ind,dec_ind or NDF_enable more than three frames ago.  |
| ES_upperT:  | ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago. |
| FO_discont: | frame offset discontinuity                                                                                    |
| PI_AIS:     | PI in AIS state                                                                                               |
| PI_LOP:     | PI in LOP state                                                                                               |
| PI_NORM:    | PI in NORM state                                                                                              |

### Notes

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an elastic store overflow/underflow occurred.
2. Transition to AIS state due to PI\_LOP event may be optionally disabled.

The autonomous transitions indicated in the state diagram are defined as follows:

|             |                                                                                                                                  |
|-------------|----------------------------------------------------------------------------------------------------------------------------------|
| inc_ind:    | transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset. |
| dec_ind:    | transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.        |
| NDF_enable: | accept new offset as active offset, transmit the pointer with NDF enabled and new offset.                                        |
| norm_point: | transmit the pointer with NDF disabled and active offset.                                                                        |
| AIS_ind:    | active offset is undefined, transmit an all-1's pointer and payload.                                                             |

### Notes:

1. Active offset is defined as the phase of the SPE (VC).

2. Enabled NDF is defined as the bit pattern 1001.
3. Disabled NDF is defined as the bit pattern 0110.

The pointer generator is a time-sliced state machine that can process up to 28 independent tributaries. The state vector is saved in RAM at the address associated with the current tributary. The pointer generator fills the outgoing tributary synchronous payload envelopes with bytes read from the associated FIFO in the payload buffer for the current tributary. The pointer generator creates pointers in the V1-V3 bytes (or H1-H3 bytes in the case of TU3s) of the outgoing data stream. The marker that tags the V5 byte (or J1 byte in the case of a TU3) that is passed through the payload buffer is used to align the pointer. The outgoing timing generator directs the pointer generator to the FIFO in the payload buffer that is associated with the tributary being processed. The pointer generator monitors the fill levels of the payload buffers and inserts outgoing pointer justifications as necessary to avoid FIFO spillage. Normally, the pointer generator has a FIFO dead band of two bytes. The dead band can be collapse to one so that any incoming pointer justifications will be reflected by a corresponding outgoing justification with no attenuation. Signals are output by the pointer generator that identify outgoing V5 bytes (or J1 bytes in the case of a TU3) and the tributary synchronous payload envelopes. These simplify the design of mappers downstream of the TUPP+622. On a per tributary basis, tributary path AIS and tributary idle (unequipped) can be inserted as controlled by microprocessor accessible registers. The idle code is selectable globally for the entire VC3 or TUG3 to be all-zeros or all-ones. It is also possible to force an inverted new data flag on individual tributaries for the purpose of diagnosing downstream pointer processors. Tributary path AIS is automatically inserted into outgoing tributaries if the pointer interpreter detects tributary path AIS on the corresponding incoming tributary.

#### **10.4 Tributary Path Overhead Processor (RTOP)**

Each tributary path overhead processor (RTOP) monitors the outgoing stream of an associated tributary payload processor (VTPP) and processes the tributaries within an STS-1, AU3, or TUG3. Each RTOP can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each RTOP ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or all TU11s).

The RTOP provides tributary performance monitoring of incoming tributaries. Bit interleaved parity of the incoming tributaries is computed and compared with the BIP-2 code encoded in the V5 byte of the tributary. Errors between the computed and received values are accumulated. RTOP also accumulates remote error indication codes. Incoming path signal label is debounced and compared with the provisioned value. Path signal label unstable, path signal label mismatch and change of path signal label event are identified.

#### 10.4.1 Clock Generator

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary path overhead processor. The overall design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary path overhead processor.

#### 10.4.2 Timing Generator

The timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the RTOP (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The identification of specific tributaries allows the error monitor and extract blocks to be time-sliced across the mix of tributaries present in the incoming data stream.

#### 10.4.3 Error Monitor

The error monitor block is a time-sliced state machine. It relies on the timing generator block to identify the tributary being processed. The error monitor block contains a set of 12-bit counters that are used to accumulate tributary path BIP-2 errors, and a set of 11-bit counters to accumulate remote error indications (REI). The contents of the counters may be transferred to a holding RAM, and the counters reset under microprocessor control.

Tributary path BIP-2 errors are detected by comparing the tributary path BIP-2 bits in the V5 byte extracted from the current multiframe, to the BIP-2 value computed for the previous multiframe. BIP-2 errors may be accumulated on a block or nibble basis as controlled by software configurable registers. Remote

error indications (REIs) are detected by extracting the REI bit from the tributary path overhead byte (V5).

Tributary path remote defect indication (RDI) and remote failure indication (RFI) are detected by extracting bit 8 and bit 4 respectively of the tributary path overhead byte (V5). The RDI is recognized when bit 8 of the V5 byte is set high for five or ten consecutive multiframes while RFI is recognized when bit 4 of V5 is set high for five or ten consecutive multiframes. In TU3 mode, RDI is recognized when bit 5 of the G1 byte is set high for five or ten consecutive frames. Bit 5 of the G1 byte is similarly processed for the status of the auxiliary RDI state. The RDI and RFI bits, and similarly bits 4 and 5 of a TU3 stream, may be treated as a two-bit code word. A code change is only recognized when the code is unchanged for five or ten frames.

The tributary path signal label (PSL) found in the tributary path overhead byte (V5) is processed. (C2 in TU3 mode). An incoming PSL is accepted when it is received unchanged for five consecutive multiframes. The accepted PSL is compared with the associated provisioned value. The PSL match/mismatch state is determined by the following:

**Table 1 - Path Signal Label Mismatch State**

| <b>Expected PSL</b> | <b>Accepted PSL</b>           | <b>PSLM State</b> | <b>UNEQ State</b> |
|---------------------|-------------------------------|-------------------|-------------------|
| 000                 | 000                           | Match             | Inactive          |
| 000                 | 001                           | Mismatch          | Inactive          |
| 000                 | PDI Code                      | Mismatch          | Inactive          |
| 000                 | XXX $\neq$ 000, 001, PDI Code | Mismatch          | Inactive          |
| 001                 | 000                           | Mismatch          | Active            |
| 001                 | 001                           | Match             | Inactive          |
| 001                 | PDI Code                      | Match             | Inactive          |
| 001                 | XXX $\neq$ 000, 001, PDI Code | Match             | Inactive          |
| PDI Code            | 000                           | Mismatch          | Active            |
| PDI Code            | 001                           | Match             | Inactive          |

| <b>Expected PSL</b>           | <b>Accepted PSL</b>           | <b>PSLM State</b> | <b>UNEQ State</b> |
|-------------------------------|-------------------------------|-------------------|-------------------|
| PDI Code                      | PDI Code                      | Match             | Inactive          |
| PDI Code                      | XXX $\neq$ 000, 001, PDI Code | Mismatch          | Inactive          |
| XXX $\neq$ 000, 001, PDI Code | 000                           | Mismatch          | Active            |
| XXX $\neq$ 000, 001, PDI Code | 001                           | Match             | Inactive          |
| XXX $\neq$ 000, 001, PDI Code | XXX                           | Match             | Inactive          |
| XXX $\neq$ 000, 001, PDI Code | YYY                           | Mismatch          | Inactive          |

Each time an incoming PSL differs from the one in the previous multiframe, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once on the errored PSL and again on the first error-free PSL. The incoming PSL is considered unstable when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive multiframes.

The UNEQ (unequipped) State column shows the response to an Accepted PSL value of 000 for various Expected PSL settings.

#### 10.4.4 In-band Error Report

The in-band error report block optionally modifies the V5 byte of outgoing non-TU3 streams to report the number of detected BIP errors and tributary path alarms. In-band error reporting is enabled by the IBER register bits in the RTOP In-band Error Reporting Configuration registers.

When in-band error reporting is enabled for non-TU3 streams, bit 3 of the V5 byte is set high when a BIP-2 error is detected in the previous multiframe. Bit 4 reports the RDI status. It is set high when the tributary path alarms named in the Tributary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Similarly, bit 8 reports the auxiliary RDI status. It is set high when the tributary path alarms named in the Tributary Auxiliary Remote Defect Indication Control registers is detected and the

corresponding enable register bits is also set high. Bits 1, 2, 5, 6 and 7 are unmodified.

### 10.4.5 Extract

The extract block uses timing information from the timing generator block to extract, serialize and output the tributary path overhead bytes (V5, J2, Z6, Z7) of all the processed tributaries on the corresponding POH output. The corresponding POHFP output is provided to identify the most significant bit of the V5 byte of the first tributary on the POH output. All four tributary path overhead bytes are shifted out within each payload frame period. Therefore, each byte is shifted out more than once. The corresponding POHEN output is used to identify fresh overhead bytes. POHEN is set high when the tributary path overhead byte is shifted out for the first time. POHEN is set low when the overhead byte is merely repeated. The corresponding tributary path overhead clock, POHCK, is nominally a 9.72 MHz clock.

## 10.5 Tributary Trace Buffer (RTTB)

Each tributary trace buffer (RTTB) monitors the outgoing stream of an associated tributary payload processor (VTPP) and processes the tributaries within an STS-1, AU3, or TUG3. Each RTTB can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each RTTB ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or all TU11s).

The RTTB extracts the tributary path trace message contained in the J2 byte (J1 byte in TU3) to a set of internal buffers. The buffers are microprocessor accessible to allow system software to examine the messages. Another set of buffers is provided for system software to download the expected message. The RTTB compares the received message with the provisioned message and reports on the state of match. The RTTB also monitors for unstable incoming tributary path trace messages.

### 10.5.1 Clock Generator

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary trace buffer. The overall

design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary trace buffer.

### 10.5.2 Timing Generator

The timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the RTTB (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The identification of specific tributaries allows the alarm monitor and extract blocks to be time-sliced across the mix of tributaries present in the incoming data stream.

### 10.5.3 Extract

The extract block is a time-sliced state machine. It uses timing information from the timing generator block to extract the tributary path trace message bytes (J2) from all the processed tributaries in the incoming stream. Each tributary in the incoming stream is allocated an individual receive buffer in the buffer block. The length of the message and, consequently, the depth of the corresponding buffer are register programmable to be 16 or 64 bytes. Bytes in the message may be written to the corresponding buffer in a circular fashion or optionally be synchronized to the framing pattern embedded in the message. For a 16 byte message, the first byte is identified by a logic one in the most significant bit. For a 64 byte message, the last two bytes are set to the ASCII characters of carriage-return (0DH) and linefeed (0AH).

### 10.5.4 Alarm Monitor

The alarm monitor block is a time-sliced state machine. It relies on the timing generator block to identify the tributary being processed. The alarm monitor block accesses an individual capture and expected buffers in the buffer block for each tributary in the incoming stream. It also monitors the received message for consistency. When the identical message is received three or five times, as controlled by the PER5 register bit, the message is accepted. This accepted message is then compared with the expected message provisioned in the buffer block. If the accepted message differs from the expected message, the trail trace identifier mismatch (TIM) alarm is raised. TIM alarm is negated if the accepted



and expected messages match. An accepted message that contains all-zero bytes is treated specially. If the expected messages is not also all-zeros, the TIM alarm is not affected upon accepting of an all-zero message. If the expected message is all-zeros, accepting an all-zeros message would negate TIM.

The alarm monitor block also monitors the incoming messages for stability. Two algorithms are provided. In the first algorithm, each time the current incoming message differs from the previous message, the corresponding unstable counter is incremented by one. Thus, a single bit error in a message of a sequence of constant messages will cause the counter to increment twice, once on the corrupted message, and again on the first error free message. A trail trace identifier unstable (TIU) alarm is raised when the counter exceeds the register programmable threshold. The counter is cleared and TIU negated when a set of identical messages is received and becomes the accepted message. In the second algorithm, when the current incoming message differs from the previous message, the corresponding counter starts incrementing once per message. A trail trace identifier unstable (TIU) alarm is raised when the counter exceeds the register programmable threshold. The counter is cleared and TIU negated when a set of identical messages is received and becomes the accepted message.

### 10.5.5 Buffer

The buffer block contains two pages of memory, one page for capturing the receive tributary path trace messages and the other for storing the expected messages. Each tributary in the incoming stream is allocated a range of addresses using high order interleaving keyed on the tributary group number and the tributary number within the group. At the J2 byte (J1 byte in TU3 mode) of each tributary, the receive and expected pages are read. The data from the incoming stream, the receive page and the expected page are supplied to the alarm monitor block for determination of trace identifier mismatch (TIM) and trace identifier unstable (TIU) alarms. At the end of the cycle, the incoming data is written to the receive page. The buffer block also contains an arbiter to allow access to the receive and expected pages by the microprocessor when neither the extract nor alarm monitor block requires access.

### 10.6 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST

instructions are supported. The TUPP+622 identification code is 053630CD hexadecimal.

## 10.7 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the TUPP+622 to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the TUPP+622 while the test mode registers are used to enhance the testability of the TUPP+622. The register set is accessed as shown in the Register Memory Map table below. Tributary based normal mode registers in each STM-1 (STS-3) Tributary Processor (STP) are arranged in order of transmission; TU #1 in TUG2 #1 of STS-1 #1 is the first tributary transmitted, while TU #4 in TUG2 #7 of STS-1 #3 is the last. Every register is documented and identified using the register number (REG #). The corresponding memory map address for every STM-1 (STS-3) Tributary Processor (STP #1, #2, #3, #4) is given in the table. Register numbers or addresses that are not shown are not used and must be treated as Reserved.

Table 2 - Register Memory Map

| REG # | Address A[13:0] |        |        |        | Description                                                |
|-------|-----------------|--------|--------|--------|------------------------------------------------------------|
|       | STP #1          | STP #2 | STP #3 | STP #4 |                                                            |
| 00    | 0000            | 0800   | 1000   | 1800   | STP Incoming Configuration                                 |
| 01    | 0001            | 0801   | 1001   | 1801   | STP Outgoing Configuration                                 |
| 02    | 0002            | 0802   | 1002   | 1802   | STP Input Signal Activity Monitor #1, Accumulation Trigger |
| 03    | 0003            | 0803   | 1003   | 1803   | STP Reset and Identity                                     |
| 04    | 0004            | 0804   | 1004   | 1804   | STP VTPP #1 Configuration #1                               |
| 05    | 0005            | 0805   | 1005   | 1805   | STP VTPP #2 Configuration #1                               |
| 06    | 0006            | 0806   | 1006   | 1806   | STP VTPP #3 Configuration #1                               |
| 07    | 0007            | 0807   | 1007   | 1807   | STP Tributary Payload Processor and LOM Interrupt Enable   |
| 08    | 0008            | 0808   | 1008   | 1808   | STP Tributary Payload Processor Interrupt and LOM Status   |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                |
|----------|-----------------|-----------|-----------|-----------|------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                            |
| 09       | 0009            | 0809      | 1009      | 1809      | STP Parity Error and LOM Interrupt                         |
| 0A       | 000A            | 080A      | 100A      | 180A      | STP RTOP and RTTB Interrupt Enable                         |
| 0B       | 000B            | 080B      | 100B      | 180B      | STP RTOP and RTTB Interrupt Status                         |
| 0C       | 000C            | 080C      | 100C      | 180C      | STP RTOP #1 and RTTB #1 Configuration                      |
| 0D       | 000D            | 080D      | 100D      | 180D      | STP RTOP #2 and RTTB #2 Configuration                      |
| 0E       | 000E            | 080E      | 100E      | 180E      | STP RTOP #3 and RTTB #3 Configuration                      |
| 10       | 0010            | 0810      | 1010      | 1810      | STP Tributary Alarm AIS Control                            |
| 11       | 0011            | 0811      | 1011      | 1811      | STP Tributary Remote Defect Indication Control             |
| 12       | 0012            | 0812      | 1012      | 1812      | STP Tributary Auxiliary Remote Defect Indication Control   |
| 13       | 0013            | 0813      | 1013      | 1813      | STP Tributary Path Defect Indication Control               |
| 14       | 0014            | 0814      | 1014      | 1814      | STP Input Signal Activity Monitor #2                       |
| 15       | 0015            | 0815      | 1015      | 1815      | STP Outgoing Pointer LSB                                   |
| 16       | 0016            | 0816      | 1016      | 1816      | STP Outgoing Pointer MSB                                   |
| 17       | 0017            | 0817      | 1017      | 1817      | STP VTPP #1 Configuration #2                               |
| 18       | 0018            | 0818      | 1018      | 1818      | STP VTPP #2 Configuration #2                               |
| 19       | 0019            | 0819      | 1019      | 1819      | STP VTPP #3 Configuration #2                               |
| 20       | 0020            | 0820      | 1020      | 1820      | VTPP #1, TU3 or TU #1 in TUG2 #1, Configuration and Status |
| 21       | 0021            | 0821      | 1021      | 1821      | VTPP #1, TU #1 in TUG2 #2, Configuration and Status        |
| 22       | 0022            | 0822      | 1022      | 1822      | VTPP #1, TU #1 in TUG2 #3, Configuration and Status        |
| 23       | 0023            | 0823      | 1023      | 1823      | VTPP #1, TU #1 in TUG2 #4, Configuration and Status        |
| 24       | 0024            | 0824      | 1024      | 1824      | VTPP #1, TU #1 in TUG2 #5, Configuration and Status        |
| 25       | 0025            | 0825      | 1025      | 1825      | VTPP #1, TU #1 in TUG2 #6, Configuration and Status        |
| 26       | 0026            | 0826      | 1026      | 1826      | VTPP #1, TU #1 in TUG2 #7, Configuration and Status        |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                    |
|----------|-----------------|-----------|-----------|-----------|----------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                                |
| 27       | 0027            | 0827      | 1027      | 1827      | VTPP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt     |
| 28-2E    | 0028-002E       | 0828-082E | 1028-102E | 1828-182E | VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 2F       | 002F            | 082F      | 102F      | 182F      | VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt            |
| 30-36    | 0030-0036       | 0830-0836 | 1030-1036 | 1830-1836 | VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 37       | 0037            | 0837      | 1037      | 1837      | VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt            |
| 38-3E    | 0038-003E       | 0838-083E | 1038-103E | 1838-183E | VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 3F       | 003F            | 083F      | 103F      | 183F      | VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt            |
| 40-5F    | 0040-005F       | 0840-085F | 1040-105F | 1840-185F | VTPP #2 Configuration and Status, and LOP Interrupt Registers  |
| 60-7F    | 0060-007F       | 0860-087F | 1060-107F | 1860-187F | VTPP #3 Configuration and Status, and LOP Interrupt Registers  |
| A0       | 00A0            | 08A0      | 10A0      | 18A0      | VTPP #1, TU3, or TU #1 in TUG2 #1, Alarm Status                |
| A1       | 00A1            | 08A1      | 10A1      | 18A1      | VTPP #1, TU #1 in TUG2 #2, Alarm Status                        |
| A2       | 00A2            | 08A2      | 10A2      | 18A2      | VTPP #1, TU #1 in TUG2 #3, Alarm Status                        |
| A3       | 00A3            | 08A3      | 10A3      | 18A3      | VTPP #1, TU #1 in TUG2 #4, Alarm Status                        |
| A4       | 00A4            | 08A4      | 10A4      | 18A4      | VTPP #1, TU #1 in TUG2 #5, Alarm Status                        |
| A5       | 00A5            | 08A5      | 10A5      | 18A5      | VTPP #1, TU #1 in TUG2 #6, Alarm Status                        |
| A6       | 00A6            | 08A6      | 10A6      | 18A6      | VTPP #1, TU #1 in TUG2 #7, Alarm Status                        |
| A7       | 00A7            | 08A7      | 10A7      | 18A7      | VTPP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt     |
| A8-AE    | 00A8-00AE       | 08A8-08AE | 10A8-10AE | 18A8-18AE | VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status             |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                   |
|----------|-----------------|-----------|-----------|-----------|---------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                               |
| AF       | 00AF            | 08AF      | 10AF      | 18AF      | VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, AIS Interrupt           |
| B0-B6    | 00B0-00B6       | 08B0-08B6 | 10B0-10B6 | 18B0-18B6 | VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status            |
| B7       | 00B7            | 08B7      | 10B7      | 18B7      | VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt           |
| B8-BE    | 00B8-00BE       | 08B8-08BE | 10B8-10BE | 18B8-18BE | VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status            |
| BF       | 00BF            | 08BF      | 10BF      | 18BF      | VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt           |
| C0-DF    | 00C0-00DF       | 08C0-08DF | 10C0-10DF | 18C0-18DF | VTPP #2 Alarm Status, and AIS Interrupt Registers             |
| E0-FF    | 00E0-00FF       | 08E0-08FF | 10E0-10FF | 18E0-18FF | VTPP #3 Alarm Status, and AIS Interrupt Registers             |
| 100      | 0100            | 0900      | 1100      | 1900      | RTOP #1, TU3 or TU #1 in TUG2 #1, Configuration               |
| 101      | 0101            | 0901      | 1101      | 1901      | RTOP #1, TU3 or TU #1 in TUG2 #1, Config. and Alarm Status    |
| 102      | 0102            | 0902      | 1102      | 1902      | RTOP #1, TU3 or TU #1 in TUG2 #1, Expected Path Signal Label  |
| 103      | 0103            | 0903      | 1103      | 1903      | RTOP #1, TU3 or TU #1 in TUG2 #1, Accepted Path Signal Label  |
| 104      | 0104            | 0904      | 1104      | 1904      | RTOP #1, TU3 or TU #1 in TUG2 #1, BIP Count LSB               |
| 105      | 0105            | 0905      | 1105      | 1905      | RTOP #1, TU3 or TU #1 in TUG2 #1, BIP Count MSB               |
| 106      | 0106            | 0906      | 1106      | 1906      | RTOP #1, TU3 or TU #1 in TUG2 #1, REI Count LSB               |
| 107      | 0107            | 0907      | 1107      | 1907      | RTOP #1, TU3 or TU #1 in TUG2 #1, REI Count MSB               |
| 108-10F  | 0108-010F       | 0908-090F | 1108-110F | 1908-190F | RTOP #1, TU #1 in TUG2 #2, Configuration and Status Registers |
| 110-117  | 0110-0117       | 0910-0917 | 1110-1117 | 1910-1917 | RTOP #1, TU #1 in TUG2 #3, Configuration and Status Registers |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                   |
|----------|-----------------|-----------|-----------|-----------|---------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                               |
| 118-11F  | 0118-011F       | 0918-091F | 1118-111F | 1918-191F | RTOP #1, TU #1 in TUG2 #4, Configuration and Status Registers |
| 120-127  | 0120-0127       | 0920-0927 | 1120-1127 | 1920-1927 | RTOP #1, TU #1 in TUG2 #5, Configuration and Status Registers |
| 128-12F  | 0128-012F       | 0928-092F | 1128-112F | 1928-192F | RTOP #1, TU #1 in TUG2 #6, Configuration and Status Registers |
| 130-137  | 0130-0137       | 0930-0937 | 1130-1137 | 1930-1937 | RTOP #1, TU #1 in TUG2 #7, Configuration and Status Registers |
| 138      | 0138            | 0938      | 1138      | 1938      | RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, COPSL Interrupt  |
| 139      | 0139            | 0939      | 1139      | 1939      | RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, PSLM Interrupt   |
| 13A      | 013A            | 093A      | 113A      | 193A      | RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, PSLU Interrupt   |
| 13B      | 013B            | 093B      | 113B      | 193B      | RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, RDI Interrupt    |
| 13C      | 013C            | 093C      | 113C      | 193C      | RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, RFI Interrupt    |
| 13D      | 013D            | 093D      | 113D      | 193D      | RTOP #1, TU #1 In Band Error Reporting Configuration          |
| 13E      | 013E            | 093E      | 113E      | 193E      | RTOP #1, TU #1 Controllable Output Configuration              |
| 140-147  | 0140-0147       | 0940-0947 | 1140-1147 | 1940-1947 | RTOP #1, TU #2 in TUG2 #1, Configuration and Status Registers |
| 148-14F  | 0148-014F       | 0948-094F | 1148-114F | 1948-194F | RTOP #1, TU #2 in TUG2 #2, Configuration and Status Registers |
| 150-157  | 0150-0157       | 0950-0957 | 1150-1157 | 1950-1957 | RTOP #1, TU #2 in TUG2 #3, Configuration and Status Registers |
| 158-15F  | 0158-015F       | 0958-095F | 1158-115F | 1958-195F | RTOP #1, TU #2 in TUG2 #4, Configuration and Status Registers |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                   |
|----------|-----------------|-----------|-----------|-----------|---------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                               |
| 160-167  | 0160-0167       | 0960-0967 | 1160-1167 | 1960-1967 | RTOP #1, TU #2 in TUG2 #5, Configuration and Status Registers |
| 168-16F  | 0168-016F       | 0968-096F | 1168-116F | 1968-196F | RTOP #1, TU #2 in TUG2 #6, Configuration and Status Registers |
| 170-177  | 0170-0177       | 0970-0977 | 1170-1177 | 1970-1977 | RTOP #1, TU #2 in TUG2 #7, Configuration and Status Registers |
| 178      | 0178            | 0978      | 1178      | 1978      | RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, COPSL Interrupt         |
| 179      | 0179            | 0979      | 1179      | 1979      | RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, PSLM Interrupt          |
| 17A      | 017A            | 097A      | 117A      | 197A      | RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, PSLU Interrupt          |
| 17B      | 017B            | 097B      | 117B      | 197B      | RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, RDI Interrupt           |
| 17C      | 017C            | 097C      | 117C      | 197C      | RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, RFI Interrupt           |
| 17D      | 017D            | 097D      | 117D      | 197D      | RTOP #1, TU #2 In Band Error Reporting Configuration          |
| 17E      | 017E            | 097E      | 117E      | 197E      | RTOP #1, TU #2 Configurable Output Control                    |
| 180-187  | 0180-0187       | 0980-0987 | 1180-1187 | 1980-1987 | RTOP #1, TU #3 in TUG2 #1, Configuration and Status Registers |
| 188-18F  | 0188-018F       | 0988-098F | 1188-118F | 1988-198F | RTOP #1, TU #3 in TUG2 #2, Configuration and Status Registers |
| 190-197  | 0190-0197       | 0990-0997 | 1190-1197 | 1990-1997 | RTOP #1, TU #3 in TUG2 #3, Configuration and Status Registers |
| 198-19F  | 0198-019F       | 0998-099F | 1198-119F | 1998-199F | RTOP #1, TU #3 in TUG2 #4, Configuration and Status Registers |
| 1A0-1A7  | 01A0-01A7       | 09A0-09A7 | 11A0-11A7 | 19A0-19A7 | RTOP #1, TU #3 in TUG2 #5, Configuration and Status Registers |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                   |
|----------|-----------------|-----------|-----------|-----------|---------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                               |
| 1A8-1AF  | 01A8-01AF       | 09A8-09AF | 11A8-11AF | 19A8-19AF | RTOP #1, TU #3 in TUG2 #6, Configuration and Status Registers |
| 1B0-1B7  | 01B0-01B7       | 09B0-09B7 | 11B0-11B7 | 19B0-19B7 | RTOP #1, TU #3 in TUG2 #7, Configuration and Status Registers |
| 1B8      | 01B8            | 09B8      | 11B8      | 19B8      | RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, COPSL Interrupt         |
| 1B9      | 01B9            | 09B9      | 11B9      | 19B9      | RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, PSLM Interrupt          |
| 1BA      | 01BA            | 09BA      | 11BA      | 19BA      | RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, PSLU Interrupt          |
| 1BB      | 01BB            | 09BB      | 11BB      | 19BB      | RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, RDI Interrupt           |
| 1BC      | 01BC            | 09BC      | 11BC      | 19BC      | RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, RFI Interrupt           |
| 1BD      | 01BD            | 09BD      | 11BD      | 19BD      | RTOP #1, TU #3 In Band Error Reporting Configuration          |
| 1BE      | 01BE            | 09BE      | 11BE      | 19BE      | RTOP #1, TU #3 Configurable Output Control                    |
| 1C0-1C7  | 01C0-01C7       | 09C0-09C7 | 11C0-11C7 | 19C0-19C7 | RTOP #1, TU #4 in TUG2 #1, Configuration and Status Registers |
| 1C8-1CF  | 01C8-01CF       | 09C8-09CF | 11C8-11CF | 19C8-19CF | RTOP #1, TU #4 in TUG2 #2, Configuration and Status Registers |
| 1D0-1D7  | 01D0-01D7       | 09D0-09D7 | 11D0-11D7 | 19D0-19D7 | RTOP #1, TU #4 in TUG2 #3, Configuration and Status Registers |
| 1D8-1DF  | 01D8-01DF       | 09D8-09DF | 11D8-11DF | 19D8-19DF | RTOP #1, TU #4 in TUG2 #4, Configuration and Status Registers |
| 1E0-1E7  | 01E0-01E7       | 09E0-09E7 | 11E0-11E7 | 19E0-19E7 | RTOP #1, TU #4 in TUG2 #5, Configuration and Status Registers |
| 1E8-1EF  | 01E8-01EF       | 09E8-09EF | 11E8-11EF | 19E8-19EF | RTOP #1, TU #4 in TUG2 #6, Configuration and Status Registers |



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| REG<br># | Address A[13:0] |           |           |           | Description                                                   |
|----------|-----------------|-----------|-----------|-----------|---------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                               |
| 1F0-1F7  | 01F0-01F7       | 09F0-09F7 | 11F0-11F7 | 19F0-19F7 | RTOP #1, TU #4 in TUG2 #7, Configuration and Status Registers |
| 1F8      | 01F8            | 09F8      | 11F8      | 19F8      | RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, COPSL Interrupt         |
| 1F9      | 01F9            | 09F9      | 11F9      | 19F9      | RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, PSLM Interrupt          |
| 1FA      | 01FA            | 09FA      | 11FA      | 19FA      | RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, PSLU Interrupt          |
| 1FB      | 01FB            | 09FB      | 11FB      | 19FB      | RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, RDI Interrupt           |
| 1FC      | 01FC            | 09FC      | 11FC      | 19FC      | RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, RFI Interrupt           |
| 1FD      | 01FD            | 09FD      | 11FD      | 19FD      | RTOP #1, TU #4 In Band Error Reporting Configuration          |
| 1FE      | 01FE            | 09FE      | 11FE      | 19FE      | RTOP #1, TU #4 Configurable Output Control                    |
| 1FF      | 01FF            | 09FF      | 11FF      | 19FF      | RTOP #1 Status                                                |
| 200-2FF  | 0200-02FF       | 0A00-0AFF | 1200-12FF | 1A00-1AFF | RTOP #2 Registers                                             |
| 300-3FF  | 0300-03FF       | 0B00-0BFF | 1300-13FF | 1B00-1BFF | RTOP #3 Registers                                             |
| 400      | 0400            | 0C00      | 1400      | 1C00      | RTTB #1, TU3 or TU #1 in TUG2 #1 Configuration and Status     |
| 401      | 0401            | 0C01      | 1401      | 1C01      | RTTB #1, TU #1 in TUG2 #2 Configuration and Status            |
| 402      | 0402            | 0C02      | 1402      | 1C02      | RTTB #1, TU #1 in TUG2 #3 Configuration and Status            |
| 403      | 0403            | 0C03      | 1403      | 1C03      | RTTB #1, TU #1 in TUG2 #4 Configuration and Status            |
| 404      | 0404            | 0C04      | 1404      | 1C04      | RTTB #1, TU #1 in TUG2 #5 Configuration and Status            |
| 405      | 0405            | 0C05      | 1405      | 1C05      | RTTB #1, TU #1 in TUG2 #6 Configuration and Status            |
| 406      | 0406            | 0C06      | 1406      | 1C06      | RTTB #1, TU #1 in TUG2 #7 Configuration and Status            |

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| REG<br># | Address A[13:0] |           |           |           | Description                                                    |
|----------|-----------------|-----------|-----------|-----------|----------------------------------------------------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                                                                |
| 408-40E  | 0408-040E       | 0C08-0C0E | 1408-140E | 1C08-1C0E | RTTB #1, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 410-416  | 0410-0416       | 0C10-0C16 | 1410-1416 | 1C10-1C16 | RTTB #1, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 418-41E  | 0418-041E       | 0C18-0C1E | 1418-141E | 1C18-1C1E | RTTB #1, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 420      | 0420            | 0C20      | 1420      | 1C20      | RTTB #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIM Interrupt     |
| 421      | 0421            | 0C21      | 1421      | 1C21      | RTTB #1, TU #2 in TUG2 #1 to TUG2 #7, TIM Interrupt            |
| 422      | 0422            | 0C22      | 1422      | 1C22      | RTTB #1, TU #3 in TUG2 #1 to TUG2 #7, TIM Interrupt            |
| 423      | 0423            | 0C23      | 1423      | 1C23      | RTTB #1, TU #4 in TUG2 #1 to TUG2 #7, TIM Interrupt            |
| 424      | 0424            | 0C24      | 1424      | 1C24      | RTTB #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIU Interrupt     |
| 425      | 0425            | 0C25      | 1425      | 1C25      | RTTB #1, TU #2 in TUG2 #1 to TUG2 #7, TIU Interrupt            |
| 426      | 0426            | 0C26      | 1426      | 1C26      | RTTB #1, TU #3 in TUG2 #1 to TUG2 #7, TIU Interrupt            |
| 427      | 0427            | 0C27      | 1427      | 1C27      | RTTB #1, TU #4 in TUG2 #1 to TUG2 #7, TIU Interrupt            |
| 428      | 0428            | 0C28      | 1428      | 1C28      | RTTB #1, TIU Threshold                                         |
| 429      | 0429            | 0C29      | 1429      | 1C29      | RTTB #1, Indirect Tributary Select                             |
| 42A      | 042A            | 0C2A      | 142A      | 1C2A      | RTTB #1, Indirect Buffer Address                               |
| 42B      | 042B            | 0C2B      | 142B      | 1C2B      | RTTB #1, Indirect Data                                         |
| 440-47F  | 0440-047F       | 0C40-0C7F | 1440-147F | 1C40-1C7F | RTTB #2 Registers                                              |

| REG<br># | Address A[13:0] |           |           |           | Description       |
|----------|-----------------|-----------|-----------|-----------|-------------------|
|          | STP<br>#1       | STP<br>#2 | STP<br>#3 | STP<br>#4 |                   |
| 480-4BF  | 0480-04BF       | 0C80-0CBF | 1480-14BF | 1C80-1CBF | RTTB #3 Registers |
|          | 2000            |           |           |           | Master Test       |
|          | 2001-3FFF       |           |           |           | Reserved for Test |

**Notes on Register Memory Map:**

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is the test resistor select (TRS) and should be set to logic 0 for normal mode register access.
4. All register numbers and addresses shown are in hexadecimal.

## **11 NORMAL MODE REGISTER DESCRIPTION**

Normal mode registers are used to configure and monitor the operation of the TUPP+622. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

### **Notes on Normal Mode Register Bits:**

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TUPP+622 to determine the programming state of the device.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect TUPP+622 operation unless otherwise noted.
5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the TUPP+622 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

## **11.1 Top Level Configuration Registers**

### **Register 00H: STP Incoming Configuration**

| <b>Bit</b> | <b>Type</b> | <b>Function</b> | <b>Default</b> |
|------------|-------------|-----------------|----------------|
| Bit 7      | R/W         | IPE             | 0              |
| Bit 6      | R/W         | LOPAIS          | 0              |
| Bit 5      | R/W         | INCIPL          | 0              |
| Bit 4      | R/W         | INCIC1J1        | 0              |
| Bit 3      | R/W         | IOP             | 0              |
| Bit 2      | R/W         | ITMFH4          | 0              |
| Bit 1      | R/W         | ITMFEN          | 0              |
| Bit 0      | R/W         | ICONCAT         | 0              |

This register configures the STP functionality in the TUPP+622 that are related to the incoming data stream.

#### **ICONCAT:**

When set high, the ICONCAT bit configures the incoming section of the STP to operate in AU4 mode. When the ICONCAT bit is set low, the incoming section operates in AU3 mode (or equivalently, STS-1 mode).

#### **ITMFEN:**

When set high, the ITMFEN bit enables the TUPP+622 to use the corresponding ITMF input signal to locate tributary multiframe boundaries. The H4 bytes in the corresponding incoming data stream are ignored. When ITMFEN is set low, the H4 bytes are used to locate the boundaries, and the ITMF signal is ignored.

#### **ITMFH4:**

The ITMFH4 bit selects the location of the ITMF in the tributary multiframe. When ITMFH4 is set high, ITMF is pulsed high to mark the H4 byte which indicates that the next AU3/4 or STS-1 frame is the first frame of the tributary

multiframe. When ITMFH4 is set low, ITMF marks the third byte after J1. ITMFH4 is ignored if ITMF is disabled by setting the ITMFEN bit low.

#### IOP:

The IOP bit controls the expected parity on the corresponding incoming parity signal IDP. When IOP is set high, the parity of the parity signal set, together with IDP is expected to be odd. When IOP is set low, the expected parity is even. Membership of the parity signal set always includes ID[7:0], and may include input signals IC1J1 and IPL as controlled by the INCIC1J1 and INCIPL bits, respectively.

#### INCIC1J1:

The INCIC1J1 bit controls whether the corresponding IC1J1 input signal participates in the incoming parity calculations. When INCIC1J1 is set high, the parity signal set includes the IC1J1 input. When INCIC1J1 is set low, parity is calculated without regard to the state of IC1J1. Selection of odd or even parity is controlled by the IOP bit.

#### INCIPL:

The INCIPL bit controls whether the corresponding IPL input signal participates in the incoming parity calculations. When INCIPL is set high, the parity signal set includes the IPL input. When INCIPL is set low, parity is calculated without regard to the state of IPL. Selection of odd or even parity is controlled by the IOP bit.

#### LOPAIS:

The LOP AIS bit is an active high AIS insertion enable. When LOP AIS is set high, AIS is automatically generated on the corresponding outgoing data stream for all tributaries that are in loss of pointer state. When LOP AIS is set low, the generation of AIS on the outgoing data stream is inhibited. This bit is logically OR'ed with the bit of the same name in Tributary Alarm AIS Control register.

#### IPE:

The IPE bit is an active high interrupt enable. When IPE is set high, the occurrence of a parity error on the corresponding incoming parity signal set will cause an interrupt to be asserted on the interrupt (INTB) output. When IPE is set low, incoming parity errors will not cause an interrupt.

### Register 01H: STP Outgoing Configuration

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | INCOPL   | 0       |
| Bit 6 | R/W  | INCOC1J1 | 0       |
| Bit 5 | R/W  | POHPT    | 0       |
| Bit 4 | R/W  | OV1EN    | 0       |
| Bit 3 | R/W  | OOP      | 0       |
| Bit 2 | R/W  | OTMFH4   | 0       |
| Bit 1 | R/W  | Reserved | 0       |
| Bit 0 | R/W  | OCONCAT  | 0       |

This register configures the STP functionality in the TUPP+622 that are related to the outgoing data stream.

#### OCONCAT:

When set high, the OCONCAT bit configures the outgoing section of the STP to operate in AU4 mode. When the OCONCAT bit is set low, the outgoing section operates in AU3 mode (or equivalently, STS-1 mode).

#### Reserved:

The Reserved bit must be set low for correct operation of the TUPP+622.

#### OTMFH4:

The OTMFH4 bit selects the location of the corresponding OTMF in the tributary multiframe. When OTMFH4 is set high, OTMF is pulsed high to mark the H4 byte which indicates that the next AU3/4 or STS-1 frame is the first frame of the tributary multiframe. When OTMFH4 is set low, OTMF marks the third byte after J1.

#### OOP:

The OOP bit controls the parity placed on the corresponding outgoing parity signal ODP. When OOP is set low, the parity of outgoing data stream OD[7:0], together with ODP is even. When OOP is set high, the parity is odd.

OV1EN:

The OV1EN bit controls the identification of the third byte after J1 in the V1 frame. When OV1EN is set low, the corresponding OC1J1V1 output only indicates the C1 and J1 bytes. The third byte after J1 is not indicated. When OV1EN is set high, the corresponding OC1J1V1 output indicates the C1, J1 and the third byte after J1.

POHPT:

The POHPT bit controls the data of the path overhead column on the corresponding outgoing STS-1 (AU3, AU4) streams. When POHPT is set low, the outgoing POH columns (except the H4 byte) are set to all-zeros. When POHPT is set high, the POH column (except the H4 byte) of the corresponding incoming stream is transferred to the outgoing stream. A two frame elastic store buffer is provided to absorb phase variations between the incoming and outgoing frames.

INCOC1J1:

The INCOC1J1 bit controls whether the corresponding OC1J1V1 output signal participates in the outgoing parity calculations. When INCOC1J1 is set high, the parity signal set includes the OC1J1V1 output. When INCOC1J1 is set low, parity is calculated without regard to the state of OC1J1V1. Selection of odd or even parity is controlled by the OOP bit.

INCOPL:

The INCOPL bit controls whether the corresponding OPL output signal participates in the outgoing parity calculations. When INCOPL is set high, the parity signal set includes the OPL output. When INCOPL is set low, parity is calculated without regard to the state of OPL. Selection of odd or even parity is controlled by the OOP bit.



**Register 02H: STP Input Signal Activity Monitor #1, Accumulation Trigger**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | OTMFA     | X       |
| Bit 6 |      | Unused    | X       |
| Bit 5 | R    | GSCLK_FPA | X       |
| Bit 4 | R    | IDA       | X       |
| Bit 3 | R    | ITMFA     | X       |
| Bit 2 | R    | IPLA      | X       |
| Bit 1 | R    | IC1J1A    | X       |
| Bit 0 | R    | SCLKA     | X       |

This register, along with the STP Input Signal Activity Monitor #2, provides activity monitoring on major TUPP+622 inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect for stuck at conditions.

Writing to this register delimits the accumulation intervals in the RTOP accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 0.5 second or shorter. The bits in this register are not affected by write accesses.

**SCLKA:**

The SCLK active (SCLKA) bit monitors for low to high transitions on the SCLK input. SCLKA is set high on a rising edge of SCLK, and is set low when this register is read.

**IC1J1A:**

The IC1J1 active (IC1J1A) bit monitors for low to high transitions on the corresponding IC1J1 input. IC1J1A is set high on a rising edge of IC1J1, and is set low when this register is read.

**IPLA:**

The IPL active (IPLA) bit monitors for low to high transitions on the corresponding IPL input. IPLA is set high on a rising edge of IPL, and is set low when this register is read.

**ITMFA:**

The ITMF active (ITMFA) bit monitors for low to high transitions on the corresponding ITMF input. ITMFA is set high on a rising edge of ITMF, and is set low when this register is read.

**IDA:**

The ID bus active (IDA) bit monitors for low to high transitions on the corresponding input data bus. IDA is set high when rising edges have been observed on all the signals on the input data bus, and is set low when this register is read.

**GSCLK\_FPA:**

The GSCLK\_FP active (GSCLK\_FPA) bit monitors for low to high transitions on the corresponding GSCLK\_FP input. GSCLK\_FPA is set high on a rising edge of GSCLK\_FP, and is set low when this register is read.

**OTMFA:**

The OTMF active (OTMFA) bit monitors for low to high transitions on the corresponding OTMF input. OTMFA is set high on a rising edge of OTMF, and is set low when this register is read.

**Register 03H: STP Reset and Identity**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | RESET    | 0       |
| Bit 6 | R    | TYPE     | 1       |
| Bit 5 | R    | ID[5]    | 0       |
| Bit 4 | R    | ID[4]    | 0       |
| Bit 3 | R    | ID[3]    | 0       |
| Bit 2 | R    | ID[2]    | 0       |
| Bit 1 | R    | ID[1]    | 0       |
| Bit 0 | R    | ID[0]    | 1       |

This register allows the revision of the TUPP+622 to be read by software permitting graceful migration to support for newer, feature enhanced versions of the TUPP+622, should revision of the TUPP+622 occur. It also provides software reset capability.

**ID[5:0]:**

The ID bits can be read to provide a binary TUPP+622 revision number.

**TYPE:**

This legacy TYPE bit is set high in the TUPP+622 to indicate the TUPP-PLUS (like) functionality provided by each STP. This bit is implemented in the TUPP+622 to maintain software backward compatibility with the TUPP-PLUS (PM5362) device.

**RESET:**

The RESET bit allows the associated STP in the TUPP+622 to be reset under software control. If the RESET bit is a logic 1, the STP is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the STP out of reset. Holding the STP in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset for the STP.

**Register 04H: STP VTPP #1 Configuration #1**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | TUGEN    | 0       |
| Bit 6 | R/W  | SOS      | 0       |
| Bit 5 | R/W  | MONIS    | 0       |
| Bit 4 | R/W  | Reserved | 0       |
| Bit 3 | R/W  | NOFILT   | 0       |
| Bit 2 | R/W  | TU3      | 0       |
| Bit 1 | R/W  | ITUG3    | 0       |
| Bit 0 | R/W  | OTUG3    | 0       |

This register is used to enable the processing of STS-1 #1 (TUG3 #1) and configure the major operational modes of VTPP #1.

**OTUG3:**

When set high, the OTUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the outgoing data stream. When set low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

**ITUG3:**

When set high, the ITUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the incoming data stream. When set low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

**TU3:**

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. The programming of the ITUG3 and OTUG3 bits are ignored. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. In TU3 mode, registers

20H and 27H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are disabled; data written is ignored, data read is invalid. Out of TU3 mode, register 20H reflects status and configuration of TUG2 #1, TU #1 and register 27H reflect LOP interrupt status of TU #1 in all seven TUG #2s. When changing the value of the TU3 bit, tributary processing must be disabled (TUGEN must have a value of logic zero).

#### NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

#### Reserved:

The Reserved bit must be set low for correct operation of the TUPP+622.

#### MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

#### SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc\_ind and dec\_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change. This bit does not apply to set new pointer events (i.e. NDF's).

**TUGEN:**

When set high, the TUGEN bit enables the processing of tributaries in STS-1 #1 (TUG3 #1). When TUGEN is low, VTPP #1, RTOP #1 and RTTB #1 are held in a low power, reset state. The data in STS-1 #1 (TUG3 #1) is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. When TUGEN is set low, all VTPP #1, RTOP #1, and RTTB #1 registers are reset to their default states.

Before the TUGEN bit is set high, it is essential to first set the NOIC1J1PLBYP bit in the STP VTPP #1 Configuration #2 register high. This will ensure that the re-transmission of the corresponding input Telecom Bus signals, IC1J1 and IPL, to the output Telecom Bus is terminated gracefully.

**Register 05H: STP VTPP #2 Configuration #1**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | TUGEN    | 0       |
| Bit 6 | R/W  | SOS      | 0       |
| Bit 5 | R/W  | MONIS    | 0       |
| Bit 4 | R/W  | Reserved | 0       |
| Bit 3 | R/W  | NOFILT   | 0       |
| Bit 2 | R/W  | TU3      | 0       |
| Bit 1 | R/W  | ITUG3    | 0       |
| Bit 0 | R/W  | OTUG3    | 0       |

This register is used to enable the processing of STS-1 #2 (TUG3 #2) and configure the major operational modes of VTPP #2.

**OTUG3:**

When set high, the OTUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the outgoing data stream. When set low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

**ITUG3:**

When set high, the ITUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the incoming data stream. When set low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

**TU3:**

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. The programming of the ITUG3 and OTUG3 bits are ignored. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. In TU3 mode, registers

40H and 47H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are disabled; data written is ignored, and read data is invalid. Out of TU3 mode, register 40H reflects status and configuration of TUG2 #1, TU #1 and register 47H reflect LOP interrupt status of TU #1 in all seven TUG #2s. When changing the value of the TU3 bit, tributary processing must be disabled (TUGEN must have a value of logic zero).

#### NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

#### Reserved:

The Reserved bit must be set low for correct operation of the TUPP+622.

#### MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

#### SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc\_ind and dec\_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change. This bit does not apply to set new pointer events (i.e. NDF's).



**TUGEN:**

When set high, the TUGEN bit enables the processing of tributaries in STS-1 #2 (TUG3 #2). When TUGEN is low, VTPP #2, RTOP #2 and RTTB #2 are held in a low power, reset state. The data in STS-1 #2 (TUG3 #2) is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. When TUGEN is set low, all VTPP #2, RTOP #2, and RTTB #2 registers are reset to their default states.

Before the TUGEN bit is set high, it is essential to first set the NOIC1J1PLBYP bit in the STP VTPP #2 Configuration #2 register high. This will ensure that the re-transmission of the corresponding input Telecom Bus signals, IC1J1 and IPL, to the output Telecom Bus is terminated gracefully.

**Register 06H: STP VTPP #3 Configuration #1**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | TUGEN    | 0       |
| Bit 6 | R/W  | SOS      | 0       |
| Bit 5 | R/W  | MONIS    | 0       |
| Bit 4 | R/W  | Reserved | 0       |
| Bit 3 | R/W  | NOFILT   | 0       |
| Bit 2 | R/W  | TU3      | 0       |
| Bit 1 | R/W  | ITUG3    | 0       |
| Bit 0 | R/W  | OTUG3    | 0       |

This register is used to enable the processing of STS-1 #3 (TUG3 #3) and configure the major operational modes of VTPP #1.

**OTUG3:**

When set high, the OTUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the outgoing data stream. When set low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

**ITUG3:**

When set high, the ITUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the incoming data stream. When set low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

**TU3:**

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. The programming of the ITUG3 and OTUG3 bits are ignored. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. In TU3 mode, registers

60H and 67H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are disabled; data written is ignored and read data is invalid. Out of TU3 mode, register 60H reflects status and configuration of TUG2 #1, TU #1 and register 67H reflect LOP interrupt status of TU #1 in all seven TUG #2s. When changing the value of the TU3 bit, tributary processing must be disabled (TUGEN must have a value of logic zero).

#### NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

#### Reserved:

The Reserved bit must be set low for correct operation of the TUPP+622.

#### MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

#### SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc\_ind and dec\_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change. This bit does not apply to set new pointer events (i.e. NDF's).

**TUGEN:**

When set high, the TUGEN bit enables the processing of tributaries in STS-1 #3 (TUG3 #3). When TUGEN is low, VTPP #3, RTOP #3 and RTTB #3 are held in a low power, reset state. The data in STS-1 #3 (TUG3 #3) is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. When TUGEN is set low, all VTPP #3, RTOP #3, and RTTB #3 registers are reset to their default states.

Before the TUGEN bit is set high, it is essential to first set the NOIC1J1PLBYP bit in the STP VTPP #3 Configuration #2 register high. This will ensure that the re-transmission of the corresponding input Telecom Bus signals, IC1J1 and IPL, to the output Telecom Bus is terminated gracefully.

**Register 07H: STP Tributary Payload Processor and LOM Interrupt Enable**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | R/W  | LOM3E    | 0       |
| Bit 4 | R/W  | LOM2E    | 0       |
| Bit 3 | R/W  | LOM1E    | 0       |
| Bit 2 | R/W  | VTPP3E   | 0       |
| Bit 1 | R/W  | VTPP2E   | 0       |
| Bit 0 | R/W  | VTPP1E   | 0       |

This register provides interrupt enable of the three H4 byte framers and of the three tributary payload processors in the STP.

**VTPP1E:**

VTPP1E is the interrupt enable bit for tributary payload processor #1 in the STP. Interrupts enabled at tributary processor #1 but masked by VTPP1E will still be reported by the VTPP1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #1 will not be reported by the VTPP1I bit.

**VTPP2E:**

VTPP2E is the interrupt enable bit for tributary processor #2 in the STP. Interrupts enabled at tributary payload processor #2 but masked by VTPP2E will still be reported by the VTPP2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #2 will not be reported by the VTPP2I bit.

**VTPP3E:**

VTPP3E is the interrupt enable bit for tributary payload processor #3 in the STP. Interrupts enabled at tributary processor #3 but masked by VTPP3E will still be reported by the VTPP3I bit, although the interrupt output will not be

activated. Interrupts disabled at tributary payload processor #3 will not be reported by the VTPP3I bit.

#### LOM1E:

The LOM1E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #1. When LOM1E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when LOME is set low.

#### LOM2E:

The LOM2E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #2. When LOM2E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when LOME is set low. When ICONCAT is set to logic 1 this interrupt enable bit should be set to logic 0. In the AU4 mode the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

#### LOM3E:

The LOM3E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #3. When LOM3E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when LOME is set low. When ICONCAT is set to logic 1 this interrupt enable bit should be set to logic 0. In the AU4 mode the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

**Register 08H: STP Tributary Payload Processor Interrupt and LOM Status**

| Bit    | Type | Function | Default |
|--------|------|----------|---------|
| ZBit 7 |      | Unused   | X       |
| Bit 6  |      | Unused   | X       |
| Bit 5  | R    | LOM3V    | 0       |
| Bit 4  | R    | LOM2V    | 0       |
| Bit 3  | R    | LOM1V    | 0       |
| Bit 2  | R    | VTPP3I   | 0       |
| Bit 1  | R    | VTPP2I   | 0       |
| Bit 0  | R    | VTPP1I   | 0       |

This register provides interrupt status of the three H4 byte framers and of the three tributary payload processors in the STP.

**VTPP1I:**

VTPP1I identifies tributary payload processor #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary payload processor #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #1 will not be reported by the VTPP1I bit.

**VTPP2I:**

VTPP2I identifies tributary payload processor #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary payload processor #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #2 will not be reported by the VTPP2I bit.

**VTPP3I:**

VTPP3I identifies tributary payload processor #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary payload processor #3 to determine the event causing the interrupt

and to clear the interrupt. Interrupts disabled at tributary payload processor #3 will not be reported by the VTPP3I bit.

#### LOM1V:

The LOM1V bit indicates the status of the H4 byte framer in tributary payload processor #1. LOM1V is set high when the H4 framer is in loss of multiframe state and is set low when it re-acquires multiframe alignment.

#### LOM2V:

The LOM2V bit indicates the status of the H4 byte framer in tributary payload processor #2. LOM2V is set high when the H4 framer is in loss of multiframe state and is set low when it re-acquires multiframe alignment. When ICONCAT is set to logic 1 this status bit should be ignored since the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

#### LOM3V:

The LOM3V bit indicates the status of the H4 byte framer in tributary payload processor #3. LOM3V is set high when the H4 framer is in loss of multiframe state and is set low when it re-acquires multiframe alignment. When ICONCAT is set to logic 1 this status bit should be ignored since the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.



**Register 09H: STP Parity Error and LOM Interrupt**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | IPI       | 0       |
| Bit 6 |      | Unused    | X       |
| Bit 5 | R    | LOM3I     | 0       |
| Bit 4 | R    | LOM2I     | 0       |
| Bit 3 | R    | LOM1I     | 0       |
| Bit 2 | R/W  | Reserved3 | 1       |
| Bit 1 | R/W  | Reserved2 | 1       |
| Bit 0 | R/W  | Reserved1 | 1       |

This register provides interrupt status of the H4 byte framers in the three tributary payload processor and of the input parity checker in the STP.

**Reserved[3:1]:**

The Reserved[3:1] bits must be set high for the correct operation of the TUPP+622.

**LOM1I:**

The LOM1I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #1 enters loss of multiframe state and when it re-acquires multiframe alignment. The LOM1I bit is set high on entry and exit to the loss of multiframe state and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The LOMI bit remains valid when interrupts are not enabled (LOM1E set low) and may be polled to detect out of frame events.

**LOM2I:**

The LOM2I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #2 enters loss of multiframe state and when it re-acquires multiframe alignment. The LOM2I bit is set high on entry and exit to the loss of multiframe state and is

cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The LOM2I bit remains valid when interrupts are not enabled (LOM2E set low) and may be polled to detect out of frame events.

#### LOM3I:

The LOM3I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #3 enters loss of multiframe state and when it re-acquires multiframe alignment. The LOM3I bit is set high on entry and exit to the loss of multiframe state and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The LOM3I bit remains valid when interrupts are not enabled (LOM3E set low) and may be polled to detect out of frame events.

#### IPI:

The incoming parity error interrupt bit (IPI) is set high when a parity error is detected on the incoming parity signal set. If the IPE bit in the STP incoming configuration register is set high, the interrupt output (INTB) is activated. When this register is read, IPI (and the corresponding interrupt) is cleared.

**Register 0AH: STP RTOP and RTTB Interrupt Enable**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | R/W  | RTTB3E   | 0       |
| Bit 4 | R/W  | RTTB2E   | 0       |
| Bit 3 | R/W  | RTTB1E   | 0       |
| Bit 2 | R/W  | RTOP3E   | 0       |
| Bit 1 | R/W  | RTOP2E   | 0       |
| Bit 0 | R/W  | RTOP1E   | 0       |

This register provides interrupt enable of the three tributary path overhead processors and of the three tributary trace buffers in the STP.

**RTOP1E:**

RTOP1E is the interrupt enable bit for tributary path overhead processor #1 in the STP. Interrupts enabled at tributary path overhead processor #1 but masked by RTOP1E will still be reported by the RTOP1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary path overhead processor #1 will not be reported by the RTOP1I bit.

**RTOP2E:**

RTOP2E is the interrupt enable bit for tributary path overhead processor #2 in the STP. Interrupts enabled at tributary path overhead processor #2 but masked by RTOP2E will still be reported by the RTOP2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary path overhead processor #2 will not be reported by the RTOP2I bit.

**RTOP3E:**

RTOP3E is the interrupt enable bit for tributary path overhead processor #3 in the STP. Interrupts enabled at tributary path overhead processor #3 but masked by RTOP3E will still be reported by the RTOP3I bit, although the

interrupt output will not be activated. Interrupts disabled at tributary path overhead processor #3 will not be reported by the RTOP3I bit.

#### RTTB1E:

RTTB1E is the interrupt enable bit for tributary trace buffer #1 in the STP. Interrupts enabled at tributary trace buffer #1 but masked by RTTB1E will still be reported by the RTTB1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary trace buffer #1 will not be reported by the RTTB1I bit.

#### RTTB2E:

RTTB2E is the interrupt enable bit for tributary trace buffer #2 in the STP. Interrupts enabled at tributary trace buffer #2 but masked by RTTB2E will still be reported by the RTTB2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary trace buffer #2 will not be reported by the RTTB2I bit.

#### RTTB3E:

RTTB3E is the interrupt enable bit for tributary trace buffer #3 in the STP. Interrupts enabled at tributary trace buffer #3 but masked by RTTB3E will still be reported by the RTTB3I bit, although the interrupt output will not be activated. Interrupts disabled at tributary trace buffer #3 will not be reported by the RTTB3I bit.

**Register 0BH: STP RTOP and RTTB Interrupt Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | R    | RTTB3I   | 0       |
| Bit 4 | R    | RTTB2I   | 0       |
| Bit 3 | R    | RTTB1I   | 0       |
| Bit 2 | R    | RTOP3I   | 0       |
| Bit 1 | R    | RTOP2I   | 0       |
| Bit 0 | R    | RTOP1I   | 0       |

This register provides interrupt status of the three tributary path overhead processor and of the three tributary trace buffers in the STP.

**RTOP1I:**

RTOP1I identifies tributary path overhead processor #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary path overhead processor #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary path overhead processor #1 will not be reported by the RTOP1I bit.

**RTOP2I:**

RTOP2I identifies tributary path overhead processor #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary path overhead processor #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary path overhead processor #2 will not be reported by the RTOP2I bit.

**RTOP3I:**

RTOP1I identifies tributary path overhead processor #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary path overhead processor #3 to determine the event causing the

interrupt and to clear the interrupt. Interrupts disabled at tributary path overhead processor #3 will not be reported by the RTOP3I bit.

#### RTTB1I:

RTTB1I identifies tributary trace buffer #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary trace buffer #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary trace buffer #1 will not be reported by the RTTB1I bit.

#### RTTB2I:

RTTB2I identifies tributary trace buffer #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary trace buffer #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary trace buffer #2 will not be reported by the RTTB2I bit.

#### RTTB3I:

RTTB3I identifies tributary trace buffer #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary trace buffer #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary trace buffer #3 will not be reported by the RTTB3I bit.

**Register 0CH: STP RTOP #1 and RTTB #1 Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | ALGO2    | 0       |
| Bit 6 | R/W  | PER5     | 0       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 | R/W  | RDI10    | 0       |
| Bit 2 | R/W  | PDI[2]   | 0       |
| Bit 1 | R/W  | PDI[1]   | 0       |
| Bit 0 | R/W  | PDI[0]   | 1       |

This register configures the operation of RTOP #1 and RTTB #1 in the STP.

**PDI[2:0]:**

The PDI[2:0] bits specifies the code used to convey tributary path defect indication (PDI-V) in the V5 byte (out of TU3 mode) or the C2 byte (in TU3 mode). For TU3 payloads, the PDI[2] bit is sign extended to form the byte value used for the PDI-V detection.

**RDI10:**

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

**PER5:**

The PER5 bit controls the number of identical tributary path trace messages needed for the message to become accepted. When PER5 is set high, a messages is accepted when it is received unchanged five times. When PER5 is set low, the message is accepted after three identical repetitions.

ALGO2:

The ALGO2 bit controls the algorithm used to detect trail trace identifier unstable alarms. When ALGO2 is set high, a counter starts on the first dissimilar identifier and cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold. When ALGO2 is set low, the counter increments on each dissimilar identifier and is cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold.



**Register 0DH: STP RTOP #2 and RTTB #2 Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | ALGO2    | 0       |
| Bit 6 | R/W  | PER5     | 0       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 | R/W  | RDI10    | 0       |
| Bit 2 | R/W  | PDI[2]   | 0       |
| Bit 1 | R/W  | PDI[1]   | 0       |
| Bit 0 | R/W  | PDI[0]   | 1       |

This register configures the operation of RTOP #2 and RTTB #2 in the STP.

**PDI[2:0]:**

The PDI[2:0] bits specifies the code used to convey tributary path defect indication (PDI-V) in the V5 byte (for non-TU3 payloads) or the C2 byte (for TU3 payloads). For TU3 payloads, the PDI[2] bit is sign extended to form the byte value used for the PDI-V detection.

**RDI10:**

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

**PER5:**

The PER5 bit controls the number of identical tributary path trace messages needed for the message to become accepted. When PER5 is set high, a messages is accepted when it is received unchanged five times. When PER5 is set low, the message is accepted after three identical repetitions.

ALGO2:

The ALGO2 bit controls the algorithm used to detect trail trace identifier unstable alarms. When ALGO2 is set high, a counter starts on the first dissimilar identifier and cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold. When ALGO2 is set low, the counter increments on each dissimilar identifier and is cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold.

### Register 0EH: STP RTOP #3 and RTTB #3 Configuration

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | ALGO2    | 0       |
| Bit 6 | R/W  | PER5     | 0       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 | R/W  | RDI10    | 0       |
| Bit 2 | R/W  | PDI[2]   | 0       |
| Bit 1 | R/W  | PDI[1]   | 0       |
| Bit 0 | R/W  | PDI[0]   | 1       |

This register configures the operation of RTOP #3 and RTTB #3 in the STP.

#### PDI[2:0]:

The PDI[2:0] bits specifies the code used to convey tributary path defect indication (PDI-V) in the V5 byte (for non-TU3 payloads) or the C2 byte (for TU3 payloads). For TU3 payloads, the PDI[2] bit is sign extended to form the byte value used for the PDI-V detection.

#### RDI10:

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

#### PER5:

The PER5 bit controls the number of identical tributary path trace messages needed for the message to become accepted. When PER5 is set high, a messages is accepted when it is received unchanged five times. When PER5 is set low, the message is accepted after three identical repetitions.

**ALGO2:**

The ALGO2 bit controls the algorithm used to detect trail trace identifier unstable alarms. When ALGO2 is set high, a counter starts on the first dissimilar identifier and cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold. When ALGO2 is set low, the counter increments on each dissimilar identifier and is cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold.

### Register 10H: STP Tributary Alarm AIS Control

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | LOMAIS   | 0       |
| Bit 6 | R/W  | LOPAIS   | 0       |
| Bit 5 |      | Unused   | X       |
| Bit 4 | R/W  | UNEQAIS  | 0       |
| Bit 3 | R/W  | PSLMAIS  | 0       |
| Bit 2 | R/W  | PSLUAIS  | 0       |
| Bit 1 | R/W  | TIM AIS  | 0       |
| Bit 0 | R/W  | TIU AIS  | 0       |

This register controls the insertion of tributary path AIS as a result of tributary path signal label alarms, tributary trace identifier alarms and tributary multiframe alarms.

#### TIU AIS:

The TIU AIS bit is an active high AIS insertion enable. When TIU AIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in trace identifier unstable state. When TIU AIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

#### TIM AIS:

The TIM AIS bit is an active high AIS insertion enable. When TIM AIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in trace identifier mismatch state. When TIM AIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

#### PSLUAIS:

The PSLUAIS bit is an active high AIS insertion enable. When PSLUAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in path signal label unstable state. When PSLUAIS is set

low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

#### PSLMAIS:

The PSLMAIS bit is an active high AIS insertion enable. When PSLMAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries. The generation of AIS is inhibited when UNEQ is active, regardless of the PSLM state.

#### UNEQAIS:

The UNEQAIS bit is an active high AIS insertion enable. When UNEQAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are unequipped. When UNEQAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

#### LOPAIS:

The LOP AIS bit is an active high AIS insertion enable. When LOP AIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in loss of pointer state. When LOP AIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries. This bit is logically OR'ed with the bit of the same name in STP Incoming Configuration register.

#### LOMAIS:

The LOM AIS bit is an active high AIS insertion enable. When LOM AIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in loss of tributary multiframe state. When LOM AIS is set low, the generation of AIS on the outgoing data stream is inhibited. LOM AIS has no effect on TU3 streams.

### Register 11H: STP Tributary Remote Defect Indication Control

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | LOMRDI   | 0       |
| Bit 6 | R/W  | LOPRDI   | 0       |
| Bit 5 | R/W  | AISRDI   | 0       |
| Bit 4 | R/W  | UNEQRDI  | 0       |
| Bit 3 | R/W  | PSLMRDI  | 0       |
| Bit 2 | R/W  | PSLURDI  | 0       |
| Bit 1 | R/W  | TIMRDI   | 0       |
| Bit 0 | R/W  | TIURDI   | 0       |

This register controls the insertion of tributary path RDI on the receive alarm port (RAD) and optionally on the V5 byte (G1 in TU3 mode) as a result of tributary pointer alarms, tributary path signal label alarms, tributary trace identifier alarms and tributary multiframe alarms.

#### TIURDI:

The TIURDI bit is an active high RDI insertion enable. When TIURDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier unstable state. When TIURDI is set low, reporting of RDI due to TIU is inhibited.

#### TIMRDI:

The TIMRDI bit is an active high RDI insertion enable. When TIMRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier mismatch state. When TIURDI is set low, reporting of RDI due to TIM is inhibited.

#### PSLURDI:

The PSLURDI bit is an active high RDI insertion enable. When PSLURDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in

TU3 mode) of the outgoing data stream for all tributaries that are in path signal label unstable state. When PSLURDI is set low, reporting of RDI due to PSLU is inhibited.

#### PSLMRDI:

The PSLMRDI bit is an active high RDI insertion enable. When PSLMRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMRDI is set low, reporting of RDI due to PSLM is inhibited. The generation of RDI is inhibited when UNEQ is active, regardless of the PSLM state.

#### UNEQRDI:

The UNEQRDI bit is an active high RDI insertion enable. When UNEQRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in unequipped state. When UNEQRDI is set low, reporting of RDI due to UNEQ is inhibited.

#### AISRDI:

The AISRDI bit is an active high RDI insertion enable. When AISRDI is set high, RDI is reported on RAD and optionally the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in incoming AIS state. When AISRDI is set low, reporting of RDI due to AIS is inhibited.

#### LOPRDI:

The LOPRDI bit is an active high RDI insertion enable. When LOPRDI is set high, RDI is reported on RAD and optionally the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of pointer state. When LOPRDI is set low, reporting of RDI due to LOP is inhibited.

#### LOMRDI:

The LOMRDI bit is an active high RDI insertion enable. When LOMRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of multiframe state. When LOMRDI is set low, reporting of RDI due to LOM is inhibited.



**Register 12H: STP Tributary Auxiliary Remote Defect Indication Control**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | NOLOMARDI | 1       |
| Bit 6 | R/W  | NOLOPARDI | 1       |
| Bit 5 | R/W  | NOAISARDI | 1       |
| Bit 4 | R/W  | UNEQARDI  | 0       |
| Bit 3 | R/W  | PSLMARDI  | 0       |
| Bit 2 | R/W  | PSLUARDI  | 0       |
| Bit 1 | R/W  | TIMARDI   | 0       |
| Bit 0 | R/W  | TIUARDI   | 0       |

This register controls the insertion of tributary path auxiliary RDI on the receive alarm port (RAD) and optionally on the V5 byte (G1 in TU3 mode) as a result of tributary pointer alarms, tributary path signal label alarms, tributary trace identifier alarms and tributary multiframe alarms.

**TIUARDI:**

The TIUARDI bit is an active high auxiliary RDI insertion enable. When TIUARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier unstable state. When TIUARDI is set low, reporting of auxiliary RDI due to TIM is inhibited.

**TIMARDI:**

The TIMARDI bit is an active high auxiliary RDI insertion enable. When TIMARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier mismatch state. When TIUARDI is set low, reporting of auxiliary RDI due to TIM is inhibited.

**PSLUARDI:**

The PSLUARDI bit is an active high auxiliary RDI insertion enable. When PSLUARDI is set high, ARDI is reported on RAD and optionally in the V5 byte

(G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in path signal label unstable state. When PSLUARDI is set low, reporting of auxiliary RDI due to PSLU is inhibited.

#### PSLMARDI:

The PSLMARDI bit is an active high auxiliary RDI insertion enable. When PSLMARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMARDI is set low, reporting of auxiliary RDI due to PSLM is inhibited. The generation of ARDI is inhibited when UNEQ is active, regardless of the PSLM state.

#### UNEQARDI:

The UNEQARDI bit is an active high auxiliary RDI insertion enable. When UNEQARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in unequipped state. When UNEQARDI is set low, the reporting of auxiliary RDI due to UNEQ is inhibited.

#### NOLOPARDI:

The NOLOPARDI bit is an active high auxiliary RDI insertion disable. When NOLOPARDI is set high, ARDI is not reported on RAD nor in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of pointer state. NOLOPARDI has precedence over TIUARDI, TIMARDI, PSLUARDI and PSLMARDI. When NOLOPARDI is set low, reporting of RDI is according to TIUARDI, TIMARDI, PSLUARDI and PSLMARDI and the associated alarm states.

#### NOAISARDI:

The NOAISARDI bit is an active high auxiliary RDI insertion disable. When NOAISARDI is set high, auxiliary RDI is not reported on RAD nor in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in incoming AIS state. NOAISARDI has precedence over TIUARDI, TIMARDI, PSLUARDI and PSLMARDI. When NOAISARDI is set low, reporting of RDI is according to TIUARDI, TIMARDI, PSLUARDI and PSLMARDI and the associated alarm states.

**NOLOMARDI:**

The NOLOMARDI bit is an active high auxiliary RDI insertion disable. When NOLOMARDI is set high, ARDI is not reported on RAD nor in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of multiframe state. When NOLOMARDI is set low, reporting of RDI is according to TIUARDI, TIMARDI, PSLUARDI and PSLMARDI and the associated alarm states.

**Register 13H: STP Tributary Path Defect Indication Control**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R/W  | LOPPDI   | 0       |
| Bit 5 | R/W  | AISPD    | 0       |
| Bit 4 | R/W  | UNEQPD   | 0       |
| Bit 3 | R/W  | PDIVPD   | 0       |
| Bit 2 |      | Unused   | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 |      | Unused   | X       |

This register controls the insertion of tributary path defect indications (PDI) on the receive alarm port (RAD) as a result of tributary pointer alarms, tributary unequipped alarms, and tributary path defect indication alarms.

**PDIVPD:**

The PDIVPD bit is an active high path PDI insertion enable. When PDIVPD is set high, PDI-P is reported on RAD when tributary path defect indication is detected in the tributary path signal label of the associated incoming tributary. When PDIVPD is set low, reporting of path PDI due to PDI-V is inhibited.

**UNEQPD:**

The UNEQPD bit is an active high path PDI insertion enable. When UNEQPD is set high, PDI-P is reported on RAD when tributary unequipped indication ('b000) is detected in the tributary path signal label of the associated incoming tributary. When UNEQPD is set low, reporting of path PDI due to UNEQ is inhibited.

**AISPD:**

The AISPD bit is an active high path PDI insertion enable. When AISPD is set high, PDI-P is reported on RAD when the associated incoming tributary is in AIS state. When AISPD is set low, reporting of path PDI due to AIS is inhibited.

**LOPPDI:**

The LOPPDI bit is an active high path PDI insertion enable. When LOPPDI is set high, PDI-P is reported on RAD when the associated incoming tributary is in loss of pointer state. When LOPPDI is set low, reporting of path PDI due to LOP is inhibited.

**Register 14H: STP Input Signal Activity Monitor #2**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 | R/W  | Reserved | X       |
| Bit 3 | R    | IAISA    | X       |
| Bit 2 | R    | ITPLA    | X       |
| Bit 1 | R    | ITV5A    | X       |
| Bit 0 | R    | HSCLKA   | X       |

This register, along with the STP Input Signal Activity Monitor #1, Accumulation Trigger register, provides activity monitoring on TUPP+622 input signals. When a monitored input signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect for stuck at conditions.

**HSCLKA:**

The HSCLK active (HSCLKA) bit monitors for low to high transitions on the HSCLK input. HSCLKA is set high on a rising edge of HSCLK, and is set low when this register is read.

**ITV5A:**

The ITV5 active (ITV5A) bit monitors for low to high transitions on the corresponding ITV5 input. ITV5A is set high on a rising edge of ITV5, and is set low when this register is read.

**ITPLA:**

The ITPL active (ITPLA) bit monitors for low to high transitions on the corresponding ITPL input. ITPLA is set high on a rising edge of ITPL, and is set low when this register is read.

IAISA:

The IAIS active (IAISA) bit monitors for low to high transitions on the corresponding IAIS input. IAISA is set high on a rising edge of IAIS, and is set low when this register is read.

**Register 15H: STP Outgoing Pointer LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | OPTR[7]  | 0       |
| Bit 6 | R/W  | OPTR[6]  | 0       |
| Bit 5 | R/W  | OPTR[5]  | 0       |
| Bit 4 | R/W  | OPTR[4]  | 0       |
| Bit 3 | R/W  | OPTR[3]  | 1       |
| Bit 2 | R/W  | OPTR[2]  | 0       |
| Bit 1 | R/W  | OPTR[1]  | 1       |
| Bit 0 | R/W  | OPTR[0]  | 0       |

**Register 16H: STP Outgoing Pointer MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | Reserved | 0       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 |      | Unused   | X       |
| Bit 1 | R/W  | OPTR[9]  | 1       |
| Bit 0 | R/W  | OPTR[8]  | 0       |

**OPTR[9:0]:**

The OPTR[9:0] bits are used to set an arbitrary active offset value in the corresponding outgoing (STM-1) stream. The arbitrary AU3/AU4 pointer value is transferred by writing to the STP Outgoing Pointer MSB register. A legal value (i.e.  $0 \leq \text{pointer value} \leq 782$ ) results in new AU3/AU4 pointer(s) in the



corresponding outgoing (STM-1) stream. A value of greater than 782 has no effect.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TUPP+622.

**Register 17H: STP VTPP #1 Configuration #2**

| Bit   | Type | Function     | Default |
|-------|------|--------------|---------|
| Bit 7 | R/W  | TUGBYP       | 0       |
| Bit 6 | R/W  | PIBYP        | 0       |
| Bit 5 | R/W  | NOIC1J1PLBYP | 0       |
| Bit 4 | R/W  | H4SQL        | 0       |
| Bit 3 |      | Unused       | X       |
| Bit 2 |      | Unused       | X       |
| Bit 1 |      | Unused       | X       |
| Bit 0 |      | Unused       | X       |

This register is used to configure the major operational modes of VTPP #1.

**H4SQL:**

The H4 squelch enable (H4SQL) bit controls the insertion of the H4 byte in the outgoing STS-1 #1 (TUG3 #1). When H4SQL is set high, an all zeroes byte is inserted in the H4 position of the outgoing data stream. When H4SQL is set low, normal tributary multiframe sequence in accordance with the corresponding OTMF signal is inserted in the H4 byte of the outgoing data stream.

**NOIC1J1PLBYP:**

The no IC1J1 and IPL bypass (NOIC1J1PLBYP) bit controls the bypassing of the corresponding IC1J1 and IPL signals to the OC1J1V1 and OPL outputs, respectively, when TUGEN is set low or bridge monitoring is enabled in STS-1 #1 (TUG3 #1). When NOIC1J1PLBYP is set low, the IC1J1 and IPL in the incoming data stream are transferred to the outgoing data stream unmodified. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. When NOIC1J1PLBYP is set high, IC1J1 and IPL are not bypassed, OC1J1V1 and OPL are generated signals. NOIC1J1PLBYP is ignored when TUGEN is set high or bridge monitoring is disabled in STS-1 #1 (TUG3 #1).

**PIBYP:**

When set high, the pointer bypass enable (PIBYP) bit configures the tributary payload processor to disable tributary pointer interpretation for the incoming STS-1 #1 (TUG3 #1). Pointer interpretation is performed by an external upstream pointer interpreter. Tributary payload bytes are identified by the ITPL signal and tributary payload frame boundaries are identified by the ITV5 signal. Tributary path AIS can be indicated by the IAIS signal. When PIBYP is set low, normal tributary pointer processing is performed on the incoming data stream.

**TUGBYP:**

The TUG bypass enable (TUGBYP) bit enables bridge monitoring of tributaries in STS-1 #1 (TUG3 #1). When TUGBYP is set high, control and data signals in the incoming data stream are transferred to the outgoing data stream unmodified. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. Performance monitoring by VTPP #1, RTOP #1 and RTTB #1 remains active while consequential actions are disabled. When TUGBYP is set low, STS-1 #1 (TUG3 #1) is processed normally. TUGBYP is ignored when TUGEN is set low.

Before the TUG bypass is disabled, it is essential to first set the NOIC1J1PLBYP bit in the STP VTPP #1 Configuration #2 register high. This will ensure that the re-transmission of the corresponding input Telecom Bus signals, IC1J1 and IPL, to the output Telecom Bus is terminated gracefully.

**Register 18H: STP VTPP #2 Configuration #2**

| Bit   | Type | Function     | Default |
|-------|------|--------------|---------|
| Bit 7 | R/W  | TUGBYP       | 0       |
| Bit 6 | R/W  | PIBYP        | 0       |
| Bit 5 | R/W  | NOIC1J1PLBYP | 0       |
| Bit 4 | R/W  | H4SQL        | 0       |
| Bit 3 |      | Unused       | X       |
| Bit 2 |      | Unused       | X       |
| Bit 1 |      | Unused       | X       |
| Bit 0 |      | Unused       | X       |

This register is used to configure the major operational modes of VTPP #2.

**H4SQL:**

The H4 squelch enable (NOIC1J1PLBYP) bit controls the insertion of the H4 byte in the outgoing STS-1 #2 (TUG3 #2). When H4SQL is set high, an all zeroes byte is inserted in the H4 position of the outgoing data stream. When H4SQL is set low, normal tributary multiframe sequence in accordance with the corresponding OTMF signal is inserted in the H4 byte of the outgoing data stream.

**NOIC1J1PLBYP:**

The no IC1J1 and IPL bypass (NOIC1J1PLBYP) bit controls the bypassing of the corresponding IC1J1 and IPL signals to the OC1J1V1 and OPL outputs, respectively, when TUGEN is set low or bridge monitoring is enabled in STS-1 #2 (TUG3 #2). When NOIC1J1PLBYP is set low, the IC1J1 and IPL in the incoming data stream are transferred to the outgoing data stream unmodified. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. When NOIC1J1PLBYP is set high, IC1J1 and IPL are not bypassed, OC1J1V1 and OPL are generated signals. NOIC1J1PLBYP is ignored when TUGEN is set high or bridge monitoring is disabled in STS-1 #2 (TUG3 #2).

**PIBYP:**

When set high, the pointer bypass enable (PIBYP) bit configures the tributary payload processor to disable tributary pointer interpretation for the incoming STS-1 #2 (TUG3 #2). Pointer interpretation is performed by an external upstream pointer interpreter. Tributary payload bytes are identified by the ITPL signal and tributary payload frame boundaries are identified by the ITV5 signal. Tributary path AIS can be indicated by the IAIS signal. When PIBYP is set low, normal tributary pointer processing is performed on the incoming data stream.

**TUGBYP:**

The TUG bypass enable (TUGBYP) bit enables bridge monitoring of tributaries in STS-1 #2 (TUG3 #2). When TUGBYP is set high, control and data signals in the incoming data stream are transferred to the outgoing data stream unmodified. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. Performance monitoring by VTPP #2, RTOP #2 and RTTB #2 remains active while consequential actions are disabled. When TUGBYP is set low, STS-1 #2 (TUG3 #2) is processed normally. TUGBYP is ignored when TUGEN is set low.

Before the TUG bypass is disabled, it is essential to first set the NOIC1J1PLBYP bit in the STP VTPP #2 Configuration #2 register high. This will ensure that the re-transmission of the corresponding input Telecom Bus signals, IC1J1 and IPL, to the output Telecom Bus is terminated gracefully.

**Register 19H: STP VTPP #3 Configuration #2**

| Bit   | Type | Function     | Default |
|-------|------|--------------|---------|
| Bit 7 | R/W  | TUGBYP       | 0       |
| Bit 6 | R/W  | PIBYP        | 0       |
| Bit 5 | R/W  | NOIC1J1PLBYP | 0       |
| Bit 4 | R/W  | H4SQL        | 0       |
| Bit 3 |      | Unused       | X       |
| Bit 2 |      | Unused       | X       |
| Bit 1 |      | Unused       | X       |
| Bit 0 |      | Unused       | X       |

This register is used to configure the major operational modes of VTPP #3.

**H4SQL:**

The H4 squelch enable (NOIC1J1PLBYP) bit controls the insertion of the H4 byte in the outgoing STS-1 #3 (TUG3 #3). When H4SQL is set high, an all zeroes byte is inserted in the H4 position of the outgoing data stream. When H4SQL is set low, normal tributary multiframe sequence in accordance with the corresponding OTMF signal is inserted in the H4 byte of the outgoing data stream.

**NOIC1J1PLBYP:**

The no IC1J1 and IPL bypass (NOIC1J1PLBYP) bit controls the bypassing of the corresponding IC1J1 and IPL signals to the OC1J1V1 and OPL outputs, respectively, when TUGEN is set low or bridge monitoring is enabled in STS-1 #3 (TUG3 #3). When NOIC1J1PLBYP is set low, the IC1J1 and IPL in the incoming data stream are transferred to the outgoing data stream unmodified. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. When NOIC1J1PLBYP is set high, IC1J1 and IPL are not bypassed, OC1J1V1 and OPL are generated signals. NOIC1J1PLBYP is ignored when TUGEN is set high or bridge monitoring is disabled in STS-1 #3 (TUG3 #3).

**PIBYP:**

When set high, the pointer bypass enable (PIBYP) bit configures the tributary payload processor to disable tributary pointer interpretation for the incoming STS-1 #3 (TUG3 #3). Pointer interpretation is performed by an external upstream pointer interpreter. Tributary payload bytes are identified by the ITPL signal and tributary payload frame boundaries are identified by the ITV5 signal. Tributary path AIS can be indicated by the IAIS signal. When PIBYP is set low, normal tributary pointer processing is performed on the incoming data stream.

**TUGBYP:**

The TUG bypass enable (TUGBYP) bit enables bridge monitoring of tributaries in STS-1 #3 (TUG3 #3). When TUGBYP is set high, control and data signals in the incoming data stream are transferred to the outgoing data stream unmodified. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and GSCLK\_FP input. See the bypass functional timing diagram for details. Performance monitoring by VTPP #3, RTOP #3 and RTTB #3 remains active while consequential actions are disabled. When TUGBYP is set low, STS-1 #3 (TUG3 #3) is processed normally. TUGBYP is ignored when TUGEN is set low.

Before the TUG bypass is disabled, it is essential to first set the NOIC1J1PLBYP bit in the STP VTPP #3 Configuration #2 register high. This will ensure that the re-transmission of the corresponding input Telecom Bus signals, IC1J1 and IPL, to the output Telecom Bus is terminated gracefully.

## **11.2 VTPP #1, VTPP #2 and VTPP #3 Registers**

### **Register 20H, 40H, 60H: VTPP, TU3 or TU #1 in TUG2 #1, Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | CONFIG[1] | 1       |
| Bit 6 | R/W  | CONFIG[0] | 1       |
| Bit 5 | R/W  | PF        | 0       |
| Bit 4 | R    | LOPV      | X       |
| Bit 3 | R/W  | ALARME    | 0       |
| Bit 2 | R/W  | DLOP      | 0       |
| Bit 1 | R/W  | IIDLE     | 0       |
| Bit 0 | R/W  | IP AIS    | 0       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the VTPP. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

#### **IP AIS:**

The IP AIS bit enables the insertion of path AIS for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IP AIS bit has no effect when IIDLE is set high.

#### **IIDLE:**

The IIDLE bit enables the insertion of path idle for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When IIDLE is set high, tributary payload bytes, including V5 are replaced by an all-zero code. The V5 byte is set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is forced to zero. The IIDLE bit has precedence over the IP AIS bit.



**DLOP:**

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode, is inverted to cause downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set high.

**ALARME:**

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

**LOPV:**

The LOPV bit indicates the loss of pointer status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode.

**PF:**

The PF bit enables pointer follower mode for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

**CONFIG[1:0]:**

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 21H-26H, 41H-46H, 61H-66H: VTPP, TU #1 in TUG2 #2 to TUG2 #7,  
Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | CONFIG[1] | 1       |
| Bit 6 | R/W  | CONFIG[0] | 1       |
| Bit 5 | R/W  | PF        | 0       |
| Bit 4 | R    | LOPV      | X       |
| Bit 3 | R/W  | ALARME    | 0       |
| Bit 2 | R/W  | DLOP      | 0       |
| Bit 1 | R/W  | IIDLE     | 0       |
| Bit 0 | R/W  | IPAIS     | 0       |

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

**IPAIS:**

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

**IIDLE:**

The IIDLE bit enables the insertion of path idle for tributary TU #1 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, including V5 is replaced by an all-zero code. The V5 byte is set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is forced to zero. The IIDLE bit has precedence over the IPAIS bit.

**DLOP:**

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set high.

### ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

### LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

### PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the TUG2 tributary group. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 27H, 47H, 67H: VTPP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | Reserved | 0       |
| Bit 6 | R    | LOP7I    | 0       |
| Bit 5 | R    | LOP6I    | 0       |
| Bit 4 | R    | LOP5I    | 0       |
| Bit 3 | R    | LOP4I    | 0       |
| Bit 2 | R    | LOP3I    | 0       |
| Bit 1 | R    | LOP2I    | 0       |
| Bit 0 | R    | LOP1I    | 0       |

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 loss of pointer interrupts.

**LOP1I:**

The LOP1I bit identifies the source of loss of pointer interrupts. In TU3 mode, the LOP1I bit reports and acknowledges LOP interrupt of the TU3 pointer. Out of TU3 mode, the LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set high when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

**LOP2I-LOP7I:**

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOPxI bit is set high when a loss of

pointer event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOPxl remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TUPP+622.

**Register 28H-2EH, 48H-4EH, 68H-6EH: VTPP, TU #2 in TUG2 #1 to TUG2 #7,  
Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | PF        | 0       |
| Bit 4 | R    | LOPV      | X       |
| Bit 3 | R/W  | ALARME    | 0       |
| Bit 2 | R/W  | DLOP      | 0       |
| Bit 1 | R/W  | IIDLE     | 0       |
| Bit 0 | R/W  | IPAIS     | 0       |

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

**IPAIS:**

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

**IIDLE:**

The IIDLE bit enables the insertion of path idle for tributary TU #2 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, including V5 is replaced by an all-zero code. The V5 byte is set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is forced to zero. The IIDLE bit has precedence over the IPAIS bit.

**DLOP:**

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set high.

#### ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #2 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

#### LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

#### PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

#### CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |



**Register 2FH, 4FH, 6FH: VTPP, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | LOP7I    | 0       |
| Bit 5 | R    | LOP6I    | 0       |
| Bit 4 | R    | LOP5I    | 0       |
| Bit 3 | R    | LOP4I    | 0       |
| Bit 2 | R    | LOP3I    | 0       |
| Bit 1 | R    | LOP2I    | 0       |
| Bit 0 | R    | LOP1I    | 0       |

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

**LOP1I-LOP7I:**

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated LOPxI bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOPxI bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOPxI remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

**Register 30H-36H, 50H-56H, 70H-76H: VTPP, TU #3 in TUG2 #1 to TUG2 #7,  
Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | PF        | 0       |
| Bit 4 | R    | LOPV      | X       |
| Bit 3 | R/W  | ALARME    | 0       |
| Bit 2 | R/W  | DLOP      | 0       |
| Bit 1 | R/W  | IIDLE     | 0       |
| Bit 0 | R/W  | IPAIS     | 0       |

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

**IPAIS:**

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

**IIDLE:**

The IIDLE bit enables the insertion of path idle for tributary TU #3 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, including V5 is replaced by an all-zero code. The V5 byte is set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is forced to zero. The IIDLE bit has precedence over the IPAIS bit.

**DLOP:**

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set high.

### ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #3 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

### LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

### PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

### CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 37H, 57H, 77H: VTPP, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | LOP7I    | 0       |
| Bit 5 | R    | LOP6I    | 0       |
| Bit 4 | R    | LOP5I    | 0       |
| Bit 3 | R    | LOP4I    | 0       |
| Bit 2 | R    | LOP3I    | 0       |
| Bit 1 | R    | LOP2I    | 0       |
| Bit 0 | R    | LOP1I    | 0       |

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**LOP1I-LOP7I:**

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated LOPxI bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOPxI bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOPxI remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

**Register 38H-3EH, 58H-5EH, 78H-7EH: VTPP, TU #4 in TUG2 #1 to TUG2 #7,  
Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | PF        | 0       |
| Bit 4 | R    | LOPV      | X       |
| Bit 3 | R/W  | ALARME    | 0       |
| Bit 2 | R/W  | DLOP      | 0       |
| Bit 1 | R/W  | IIDLE     | 0       |
| Bit 0 | R/W  | IPAIS     | 0       |

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or, TU12 (VT2) mode, the associated register in this set has no effect.

**IPAIS:**

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

**IIDLE:**

The IIDLE bit enables the insertion of path idle for tributary TU #4 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, including V5 is replaced by an all-zero code. The V5 byte is set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is forced to zero. The IIDLE bit has precedence over the IPAIS bit.

**DLOP:**

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set high.

#### ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #4 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

#### LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

#### PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

#### CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 3FH, 5FH, 7FH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | LOP7I    | 0       |
| Bit 5 | R    | LOP6I    | 0       |
| Bit 4 | R    | LOP5I    | 0       |
| Bit 3 | R    | LOP4I    | 0       |
| Bit 2 | R    | LOP3I    | 0       |
| Bit 1 | R    | LOP2I    | 0       |
| Bit 0 | R    | LOP1I    | 0       |

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

**LOP1I-LOP7I:**

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3, or TU12 (VT2) mode, the associated LOPxI bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOPxI bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOPxI remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

**Register A0H, C0H, E0H: VTPP, TU3 or TU #1 in TUG2 #1, Alarm Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | SS[1]    | X       |
| Bit 6 | R    | SS[0]    | X       |
| Bit 5 | R    | NJEI     | X       |
| Bit 4 | R    | PJEI     | X       |
| Bit 3 | R    | ESEI     | X       |
| Bit 2 | R/W  | PEE      | 0       |
| Bit 1 | R    | AISV     | X       |
| Bit 0 | R/W  | RELAYAIS | 0       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the alarm status of the TU3 mapped into a TUG3 handled by the VTPP. Out of TU3 mode, this register reports the alarm status of TU #1 in TUG2 #1.

**RELAYAIS:**

The RELAYAIS bit controls the number of consecutive AIS\_ind indications required to enter the AIS state for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS\_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS\_ind indications.

**AISV:**

The AISV bit indicates the tributary path AIS status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode.

**PEE:**

The PEE bit enables pointer event interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the



MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

#### ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

#### PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

#### NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

**SS[1:0]:**

The SS[1:0] bits report the value of the size bits in the V1 byte of tributary TU #1 in TUG2 #1 or the H1 byte of tributary TU3 depending on whether the VTPP is in TU3 mode. The SS[1:0] bits are not filtered and must be software de-bounced.

**Register A1H-A6H, C1H-C6H, E1H-E6H: VTPP, TU #1 in TUG2 #2 to TUG2 #7,  
Alarm Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | SS[1]    | X       |
| Bit 6 | R    | SS[0]    | X       |
| Bit 5 | R    | NJEI     | X       |
| Bit 4 | R    | PJEI     | X       |
| Bit 3 | R    | ESEI     | X       |
| Bit 2 | R/W  | PEE      | 0       |
| Bit 1 | R    | AISV     | X       |
| Bit 0 | R/W  | RELAYAIS | 0       |

This set of registers reports the alarm status of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

**RELAYAIS:**

The RELAYAIS bit controls the number of consecutive AIS\_ind indications required to enter the AIS state for tributary TU #1 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS\_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS\_ind indications.

**AISV:**

The AISV bit indicates the tributary path AIS status of tributary TU #1 in the corresponding TUG2.

**PEE:**

The PEE bit enables pointer event interrupts for tributary TU #1 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low.

Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

#### ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

#### PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

#### NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits report the value of the size bits in the V1 byte of tributary TU #1 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

**Register A7H, C7H, E7H: VTPP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, AIS  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | AIS7I    | 0       |
| Bit 5 | R    | AIS6I    | 0       |
| Bit 4 | R    | AIS5I    | 0       |
| Bit 3 | R    | AIS4I    | 0       |
| Bit 2 | R    | AIS3I    | 0       |
| Bit 1 | R    | AIS2I    | 0       |
| Bit 0 | R    | AIS1I    | 0       |

This register is used to identify and acknowledge alarm indication signal interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 AIS interrupts.

**AIS1I:**

The AIS1I bit identifies the source of tributary path AIS interrupts. In TU3 mode, the AIS1I bit reports and acknowledges AIS interrupt of the TU3 stream. Out of TU3 mode, the AIS1I bit reports and acknowledges AIS interrupt of TU #1 in TUG2 #1. Interrupts are generated upon detection and removal of tributary path AIS alarm. AIS1I is set high when the corresponding tributary path AIS event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

**AIS2I-AIS7I:**

The AIS2I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the AIS2I to AIS7I bits report and acknowledge AIS interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS. An AISxI bit is set high when a

tributary path AIS event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AISxl remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

**Register A8H-AEH, C8H-CEH, E8H-EEH: VTPP, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | SS[1]    | X       |
| Bit 6 | R    | SS[0]    | X       |
| Bit 5 | R    | NJEI     | X       |
| Bit 4 | R    | PJEI     | X       |
| Bit 3 | R    | ESEI     | X       |
| Bit 2 | R/W  | PEE      | 0       |
| Bit 1 | R    | AISV     | X       |
| Bit 0 | R/W  | RELAYAIS | 0       |

This set of registers reports the alarm status of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

**RELAYAIS:**

The RELAYAIS bit controls the number of consecutive AIS\_ind indications required to enter the AIS state for tributary TU #2 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS\_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS\_ind indications.

**AISV:**

The AISV bit indicates the tributary path AIS status of tributary TU #2 in the corresponding TUG2.

**PEE:**

The PEE bit enables pointer event interrupts for tributary TU #2 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection



of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

#### ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #2 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

#### PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

#### NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits report the value of the size bits in the V1 byte of tributary TU #2 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

**Register AFH, CFH, EFH: VTPP, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | AIS7I    | 0       |
| Bit 5 | R    | AIS6I    | 0       |
| Bit 4 | R    | AIS5I    | 0       |
| Bit 3 | R    | AIS4I    | 0       |
| Bit 2 | R    | AIS3I    | 0       |
| Bit 1 | R    | AIS2I    | 0       |
| Bit 0 | R    | AIS1I    | 0       |

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**AIS1I-AIS7I:**

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated AISxI bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AISxI bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AISxI remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

**Register B0H-B6H, D0H-D6H, F0H-F6H: VTPP, TU #3 in TUG2 #1 to TUG2 #7,  
Alarm Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | SS[1]    | X       |
| Bit 6 | R    | SS[0]    | X       |
| Bit 5 | R    | NJEI     | X       |
| Bit 4 | R    | PJEI     | X       |
| Bit 3 | R    | ESEI     | X       |
| Bit 2 | R/W  | PEE      | 0       |
| Bit 1 | R    | AISV     | X       |
| Bit 0 | R/W  | RELAYAIS | 0       |

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

**RELAYAIS:**

The RELAYAIS bit controls the number of consecutive AIS\_ind indications required to enter the AIS state for tributary TU #3 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS\_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS\_ind indications.

**AISV:**

The AISV bit indicates the tributary path AIS status of tributary TU #3 in the corresponding TUG2.

**PEE:**

The PEE bit enables pointer event interrupts for tributary TU #3 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection

of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

#### ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #3 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

#### PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

#### NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits report the value of the size bits in the V1 byte of tributary TU #3 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

**Register B7H, D7H, F7H: VTPP, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | AIS7I    | 0       |
| Bit 5 | R    | AIS6I    | 0       |
| Bit 4 | R    | AIS5I    | 0       |
| Bit 3 | R    | AIS4I    | 0       |
| Bit 2 | R    | AIS3I    | 0       |
| Bit 1 | R    | AIS2I    | 0       |
| Bit 0 | R    | AIS1I    | 0       |

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

**AIS1I-AIS7I:**

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated AISxI bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AISxI bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AISxI remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

**Register B8H-BEH, D8H-DEH, F8H-FEH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | SS[1]    | X       |
| Bit 6 | R    | SS[0]    | X       |
| Bit 5 | R    | NJEI     | X       |
| Bit 4 | R    | PJEI     | X       |
| Bit 3 | R    | ESEI     | X       |
| Bit 2 | R/W  | PEE      | 0       |
| Bit 1 | R    | AISV     | X       |
| Bit 0 | R/W  | RELAYAIS | 0       |

This set of registers reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

**RELAYAIS:**

The RELAYAIS bit controls the number of consecutive AIS\_ind indications required to enter the AIS state for tributary TU #4 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS\_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS\_ind indications.

**AISV:**

The AISV bit indicates the tributary path AIS status of tributary TU #4 in the corresponding TUG2.

**PEE:**

The PEE bit enables pointer event interrupts for tributary TU #4 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection



of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

#### ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #4 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

#### PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

#### NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits report the value of the size bits in the V1 byte of tributary TU #4 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

**Register BFH, DFH, FFH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | AIS7I    | 0       |
| Bit 5 | R    | AIS6I    | 0       |
| Bit 4 | R    | AIS5I    | 0       |
| Bit 3 | R    | AIS4I    | 0       |
| Bit 2 | R    | AIS3I    | 0       |
| Bit 1 | R    | AIS2I    | 0       |
| Bit 0 | R    | AIS1I    | 0       |

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

**AIS1I-AIS7I:**

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated AISxI bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AISxI bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AISxI remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

### **11.3 RTOP #1, RTOP #2 and RTOP #3 Registers**

#### **Register 100H, 200H, 300H: RTOP, TU3 or TU #1 in TUG2 #1, Configuration**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | CONFIG[1] | 1       |
| Bit 6 | R/W  | CONFIG[0] | 1       |
| Bit 5 | R/W  | BLKBIP    | 0       |
| Bit 4 | R/W  | PSLUE     | 0       |
| Bit 3 | R/W  | PSLME     | 0       |
| Bit 2 | R/W  | COPSLE    | 0       |
| Bit 1 | R/W  | RFIE      | 0       |
| Bit 0 | R/W  | RDIE      | 0       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

#### **RDIE:**

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTOP is in TU3 mode. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

#### **RFIE:**

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTOP is in TU3 mode. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE

is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

#### COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in TUG2 #1 or TU3. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

#### PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in TUG2 #1 or TU3. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

#### PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in TUG2 #1 or TU3. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

#### BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in TUG2 #1 or the TU3 mapped into a TUG3. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, BIP-2 two errors are counted on a nibble basis; the BIP error count is incremented once for each BIP-2 bit that is in error.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

### Register 101H, 201H, 301H: RTOP, TU3 or TU #1 in TUG2 #1, Configuration and Alarm Status

| Bit   | Type | Function      | Default |
|-------|------|---------------|---------|
| Bit 7 | R/W  | RDIZ7EN       | 0       |
| Bit 6 | R/W  | TUPTE         | 0       |
| Bit 5 | R/W  | PDIVEN        | 0       |
| Bit 4 | R    | PSLUV         | X       |
| Bit 3 | R    | PSLMV         | X       |
| Bit 2 | R    | ERDIV[2]      | X       |
| Bit 1 | R    | ERDIV[1]/RFIV | X       |
| Bit 0 | R    | ERDIV[0]/RDIV | X       |

In TU3 mode, this register reports the alarm status of the TU3 mapped into a TUG3. Out of TU3 mode, this register reports alarm status and configures TU #1 in TUG2 #1.

#### RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in TUG2 #1 or the TU3 mapped in a TUG3 when RDIZ7EN is low. Out of TU3 mode, RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

In TU3 mode, RDIV is set high when the RDI bit in the G1 byte is set high for five or ten consecutive frames as determined by the RDI10 bit. RDIV is set low when the RDI bit is set low for five or ten consecutive frames as determined by the RDI10 bit.

#### RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in TUG2 #1 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the

V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit. RFIV is not used when TU3 mode is enabled.

#### ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in TUG2 #1 or the TU3 mapped in a TUG3 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte or the G1 byte is seen for five or ten consecutive multiframes (frames in TU3 mode) as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

#### PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in TUG2 #1 or TU3. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

#### PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in TUG2 #1 or TU3. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

#### PDIVEN

The PDIVEN bit controls the insertion of tributary path defect indication for tributary TU #1 in TUG2 #1 or TU3 in the receive alarm port (RAD). When PDIVEN is set high, PDI-V is asserted regardless of the state of the path signal label. When PDIVEN is set low, PDI-V is asserted if the incoming path signal label matches the PDI code in the PDI[2:0] bit of the corresponding RTOP Configuration register.



TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in TUG2 #1 or TU3 mapped in TUG3. TUPTE is set high if tributary TU #1 or the TU3 is to be terminated in the network element containing this TUPP+622 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #1 or the TU3 is part of the through traffic in the network element containing this TUPP+622 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

Out of TU3 mode, the RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits. When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

In TU3 mode, the RDIZ7EN bit is used to control whether RDI or enhanced RDI is reported. When RDIZ7EN is set low, the RDI bit in the G1 byte is used to control the RDIV register bit. When RDIZ7EN is set high, the three bit extended RDI code in the G1 byte is used to control the ERDIV[2:0] register bits.

**Register 102H, 202H, 302H: RTOP, TU3 or TU #1 in TUG2 #1, Expected Path  
Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | EPSL[7]  | 0       |
| Bit 6 | R/W  | EPSL[6]  | 0       |
| Bit 5 | R/W  | EPSL[5]  | 0       |
| Bit 4 | R/W  | EPSL[4]  | 0       |
| Bit 3 | R/W  | EPSL[3]  | 0       |
| Bit 2 | R/W  | EPSL[2]  | 0       |
| Bit 1 | R/W  | EPSL[1]  | 0       |
| Bit 0 | R/W  | EPSL[0]  | 0       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register configures the expected path signal label of the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register configures the expected path signal label of TU #1 in TUG2 #1.

**EPSL[7:0]:**

In TU3 mode, the EPSL[7:0] bits specifies the expected path signal label of the TU3 stream. Out of TU3 mode, EPSL[2:0] specifies the expected path signal label of tributary TU #1 in TUG2 #1. The expected PSL is compared with the accepted PSL to determine the PSLM state.

**Register 103H, 203H, 303H: RTOP, TU3 or TU #1 in TUG2 #1, Accepted Path  
Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | APSL[7]  | 0       |
| Bit 6 | R    | APSL[6]  | 0       |
| Bit 5 | R    | APSL[5]  | 0       |
| Bit 4 | R    | APSL[4]  | 0       |
| Bit 3 | R    | APSL[3]  | 0       |
| Bit 2 | R    | APSL[2]  | 0       |
| Bit 1 | R    | APSL[1]  | 0       |
| Bit 0 | R    | APSL[0]  | 0       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the accepted path signal label of the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the accepted path signal label of TU #1 in TUG2 #1.

**APSL[7:0]:**

In TU3 mode, the APSL[7:0] bits report the accepted path signal label of the TU3 stream. Out of TU3 mode, APSL[2:0] specifies the accepted path signal label of tributary TU #1 in TUG2 #1. The expected PSL is compared with the accepted PSL to determine the PSLM state.

**Register 104H, 204H, 304H: RTOP, TU3 or TU #1 in TUG2 #1, BIP-2/BIP-8  
Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BIP[7]   | X       |
| Bit 6 | R    | BIP[6]   | X       |
| Bit 5 | R    | BIP[5]   | X       |
| Bit 4 | R    | BIP[4]   | X       |
| Bit 3 | R    | BIP[3]   | X       |
| Bit 2 | R    | BIP[2]   | X       |
| Bit 1 | R    | BIP[1]   | X       |
| Bit 0 | R    | BIP[0]   | X       |

**Register 105H, 205H, 305H: RTOP, TU3 or TU #1 in TUG2 #1, BIP-2/BIP-8  
Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BIP[15]  | X       |
| Bit 6 | R    | BIP[14]  | X       |
| Bit 5 | R    | BIP[13]  | X       |
| Bit 4 | R    | BIP[12]  | X       |
| Bit 3 | R    | BIP[11]  | X       |
| Bit 2 | R    | BIP[10]  | X       |
| Bit 1 | R    | BIP[9]   | X       |
| Bit 0 | R    | BIP[8]   | X       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), these registers report the number of block interleave parity (BIP-8) errors detected in the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #1. These registers do not saturate.

**BIP[15:0]:**

The BIP[15:0] bits report the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2/BIP-8 registers were polled. The BIP-2/BIP-8 registers are polled by writing to the Input Signal Activity, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2/BIP-8 registers within 10  $\mu$ s and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2/BIP-8 errors may be accumulated on a nibble/bit basis or block basis as controlled by the BLKBIP register bit. In TU3 mode, all BIP[15:0] are valid. Out of TU3 mode, only BIP[10:0] are valid, BIP[15:11] are held low.

**Register 106H, 206H, 306H: RTOP, TU3 or TU #1 in TUG2 #1, REI Error  
Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | REI[7]   | X       |
| Bit 6 | R    | REI[6]   | X       |
| Bit 5 | R    | REI[5]   | X       |
| Bit 4 | R    | REI[4]   | X       |
| Bit 3 | R    | REI[3]   | X       |
| Bit 2 | R    | REI[2]   | X       |
| Bit 1 | R    | REI[1]   | X       |
| Bit 0 | R    | REI[0]   | X       |

**Register 107H, 207H, 307H: RTOP, TU3 or TU #1 in TUG2 #1, REI Error  
Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | REI[15]  | X       |
| Bit 6 | R    | REI[14]  | X       |
| Bit 5 | R    | REI[13]  | X       |
| Bit 4 | R    | REI[12]  | X       |
| Bit 3 | R    | REI[11]  | X       |
| Bit 2 | R    | REI[10]  | X       |
| Bit 1 | R    | REI[9]   | X       |
| Bit 0 | R    | REI[8]   | X       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), these registers report the number of remote error indications (REI) detected in the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the number of remote error indications (REI) detected in TU #1 in TUG2 #1.

REI[15:0]:

The REI[15:0] bits report the number of tributary path remote error indications that have been detected since the last time the REI registers were polled. The REI registers are polled by writing to the Input Signal Activity, Accumulate Trigger register. The write access transfers the internally accumulated error counts to the REI registers within 10  $\mu$ s and simultaneously resets the internal counter to begin a new cycle of error accumulation. In TU3 mode, all REI[15:0] are valid. Out of TU3 mode, only REI[10:0] are valid, REI[15:11] are held low.

**Register 108H, 110H, 118H, 120H, 128H, 130H:  
Register 208H, 210H, 218H, 220H, 228H, 230H:  
Register 308H, 310H, 318H, 320H, 328H, 330H:  
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Configuration**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | CONFIG[1] | 1       |
| Bit 6 | R/W  | CONFIG[0] | 1       |
| Bit 5 | R/W  | BLKBIP    | 0       |
| Bit 4 | R/W  | PSLUE     | 0       |
| Bit 3 | R/W  | PSLME     | 0       |
| Bit 2 | R/W  | COPSLE    | 0       |
| Bit 1 | R/W  | RFIE      | 0       |
| Bit 0 | R/W  | RDIE      | 0       |

This set of registers configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

#### RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

#### RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.



**COPSLE:**

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

**PSLME:**

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

**PSLUE:**

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

**BLKBIP:**

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

**CONFIG[1:0]:**

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 109H, 111H, 119H, 121H, 129H, 131H:  
Register 209H, 211H, 219H, 221H, 229H, 231H:  
Register 309H, 311H, 319H, 321H, 329H, 331H:  
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Alarm Status**

| Bit   | Type | Function      | Default |
|-------|------|---------------|---------|
| Bit 7 | R/W  | RDIZ7EN       | 0       |
| Bit 6 | R/W  | TUPTE         | 0       |
| Bit 5 | R/W  | PDIVEN        | 0       |
| Bit 4 | R    | PSLUV         | X       |
| Bit 3 | R    | PSLMV         | X       |
| Bit 2 | R/W  | ERDIV[2]      | 0       |
| Bit 1 | R    | ERDIV[1]/RFIV | X       |
| Bit 0 | R    | ERDIV[0]/RDIV | X       |

This set of registers reports alarm status and configures TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

#### RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

#### RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #1 in the corresponding TUG2. The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] register bits for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in the corresponding TUG2. TUPTE is set high if tributary TU #1 is to be terminated in the network element containing this TUPP+622 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H).

TUPTE is set low if tributary TU #1 is part of the through traffic in the network element containing this TUPP+622 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

#### RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #1 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

**Register 10AH, 112H, 11AH, 122H, 12AH, 132H:  
Register 20AH, 212H, 21AH, 222H, 22AH, 232H:  
Register 30AH, 312H, 31AH, 322H, 32AH, 332H:  
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Expected Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R/W  | EPSL[2]  | 0       |
| Bit 1 | R/W  | EPSL[1]  | 0       |
| Bit 0 | R/W  | EPSL[0]  | 0       |

This set of registers configures the expected path signal label of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

#### EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #1 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

**Register 10BH, 113H, 11BH, 123H, 12BH, 133H:  
Register 20BH, 213H, 21BH, 223H, 22BH, 233H:  
Register 30BH, 313H, 31BH, 323H, 32BH, 333H:  
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Accepted Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | APSL[2]  | 0       |
| Bit 1 | R    | APSL[1]  | 0       |
| Bit 0 | R    | APSL[0]  | 0       |

This set of registers reports the accepted path signal label of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

#### APSL[2:0]:

The APSL[2:0] bits report the accepted path signal label of tributary TU #1 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

**Register 10CH, 114H, 11CH, 124H, 12CH, 134H:  
Register 20CH, 214H, 21CH, 224H, 22CH, 234H:  
Register 30CH, 314H, 31CH, 324H, 32CH, 334H:  
RTOP, TU #1 in TUG2 #2 to TUG2 #7, BIP-2 Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BIP[7]   | X       |
| Bit 6 | R    | BIP[6]   | X       |
| Bit 5 | R    | BIP[5]   | X       |
| Bit 4 | R    | BIP[4]   | X       |
| Bit 3 | R    | BIP[3]   | X       |
| Bit 2 | R    | BIP[2]   | X       |
| Bit 1 | R    | BIP[1]   | X       |
| Bit 0 | R    | BIP[0]   | X       |

**Register 10DH, 115H, 11DH, 125H, 12DH, 135H:  
Register 20DH, 215H, 21DH, 225H, 22DH, 235H:  
Register 30DH, 315H, 31DH, 325H, 32DH, 335H:  
RTOP, TU #1 in TUG2 #2 to TUG2 #7, BIP-2 Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | BIP[10]  | X       |
| Bit 1 | R    | BIP[9]   | X       |
| Bit 0 | R    | BIP[8]   | X       |



These sets of registers report the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #2 to TUG2 #7 in the previous accumulation interval. These registers have no effect in TU3 mode. These registers do not saturate.

**BIP[10:0]:**

The BIP[10:0] bits report the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to any of the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10  $\mu$ s and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2 errors may be accumulated on a nibble basis or block basis as controlled by the BLKBIP register bit.

**Register 10EH, 116H, 11EH, 126H, 12EH, 136H:  
Register 20EH, 216H, 21EH, 226H, 22EH, 236H:  
Register 30EH, 316H, 31EH, 326H, 32EH, 336H:  
TU #1 in TUG2 #2 to TUG2 #7, REI Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | REI[7]   | X       |
| Bit 6 | R    | REI[6]   | X       |
| Bit 5 | R    | REI[5]   | X       |
| Bit 4 | R    | REI[4]   | X       |
| Bit 3 | R    | REI[3]   | X       |
| Bit 2 | R    | REI[2]   | X       |
| Bit 1 | R    | REI[1]   | X       |
| Bit 0 | R    | REI[0]   | X       |

**Register 10FH, 117H, 11FH, 127H, 12FH, 137H:  
Register 20FH, 217H, 21FH, 227H, 22FH, 237H:  
Register 30FH, 317H, 31FH, 327H, 32FH, 337H:  
TU #1 in TUG2 #2 to TUG2 #7, REI Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | REI[10]  | X       |
| Bit 1 | R    | REI[9]   | X       |
| Bit 0 | R    | REI[8]   | X       |

These registers report the number of remote error indications (REI) detected in TU #1 in TUG2 #2 to TUG2 #7 in the previous accumulation interval. These registers have no effect in TU3 mode.

REI[10:0]:

The REI[10:0] bits report the number of tributary path remote error indications that have been detected since the last time the REI registers were polled. The REI registers are polled by applying by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the REI registers within 10  $\mu$ s and simultaneously resets the internal counter to begin a new cycle of error accumulation.

**Register 138H, 238H, 338H: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7,  
COPSL Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | Reserved | 0       |
| Bit 6 | R    | COPSL7I  | 0       |
| Bit 5 | R    | COPSL6I  | 0       |
| Bit 4 | R    | COPSL5I  | 0       |
| Bit 3 | R    | COPSL4I  | 0       |
| Bit 2 | R    | COPSL3I  | 0       |
| Bit 1 | R    | COPSL2I  | 0       |
| Bit 0 | R    | COPSL1I  | 0       |

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 change of path signal label interrupts.

**COPSL1I:**

The COPSL1I bit identifies the source of change of path signal label interrupts. In TU3 mode, the COPSL1I bit reports and acknowledges COPSL interrupts of the TU3 stream. Out of TU3 mode, the COPSL1I bit reports and acknowledges COPSL interrupt of TU #1 in TUG2 #1. Interrupts are generated when the accepted PSL changes. The COPSL1I bit is set high when a change of PSL event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL1I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

**COPSL2I-COPSL7I:**

The COPSL2I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, COPSL2I to COPSL7I bits report and acknowledge COPSL interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSLxI bit is

set high when a change of PSL event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPS�xl remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TUPP+622.

**Register 139H, 239H, 339H: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7,  
PSLM Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLM7I   | 0       |
| Bit 5 | R    | PSLM6I   | 0       |
| Bit 4 | R    | PSLM5I   | 0       |
| Bit 3 | R    | PSLM4I   | 0       |
| Bit 2 | R    | PSLM3I   | 0       |
| Bit 1 | R    | PSLM2I   | 0       |
| Bit 0 | R    | PSLM1I   | 0       |

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 path signal label mismatch interrupts.

**PSLM1I:**

The PSLM1I bit identifies the source of path signal label mismatch interrupts. In TU3 mode, the PSLM1I bit reports and acknowledges PSLM interrupts of the TU3 stream. Out of TU3 mode, the PSLM1I bit reports and acknowledges PSLM interrupt of TU #1 in TUG2 #1. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. The PSLM1I bit is set high when a change of in the PSL matched state occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM1I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

**PSLM1I-PSLM7I:**

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, PSLM2I to PSLM7I bits report and acknowledge PSLM interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are

generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLMxl bit is set high when a change of PSL matched state on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLMxl remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

**Register 13AH, 23AH, 33AH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7,  
PSLU Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLU7I   | 0       |
| Bit 5 | R    | PSLU6I   | 0       |
| Bit 4 | R    | PSLU5I   | 0       |
| Bit 3 | R    | PSLU4I   | 0       |
| Bit 2 | R    | PSLU3I   | 0       |
| Bit 1 | R    | PSLU2I   | 0       |
| Bit 0 | R    | PSLU1I   | 0       |

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 path signal label unstable interrupts.

**PSLU1I:**

The PSLU1I bit identifies the source of path signal label unstable interrupts. In TU3 mode, the PSLU1I bit reports and acknowledges PSLU interrupts of the TU3 stream. Out of TU3 mode, the PSLU1I bit reports and acknowledges PSLU interrupt of TU #1 in TUG2 #1. Interrupts are generated when the received PSL becomes unstable or returns to stable. The PSLU1I bit is set high when a change of in the PSL unstable state occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU1I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

**PSLU2I-PSLU7I:**

The PSLU2I to PSLU7I bits identify the source of path signal label mismatch interrupts. PSLU2I to PSLU7I bits report and acknowledge PSLU interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLUxI bit is set



high when a change of PSL unstable state on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLUxl remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

**Register 13BH, 23BH, 33BH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7,  
RDI Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RDI7I    | 0       |
| Bit 5 | R    | RDI6I    | 0       |
| Bit 4 | R    | RDI5I    | 0       |
| Bit 3 | R    | RDI4I    | 0       |
| Bit 2 | R    | RDI3I    | 0       |
| Bit 1 | R    | RDI2I    | 0       |
| Bit 0 | R    | RDI1I    | 0       |

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 remote defect indication interrupts.

**RDI1I:**

The RDI1I bit identify the source of remote defect indication interrupts. In TU3 mode, the RDI1I bit reports and acknowledges RDI interrupt of the TU3 stream. Out of TU3 mode, the RDI1I bit reports and acknowledges RDI interrupt of TU #1 in TUG2 #1. Interrupts are generated when the received RDI state changes. The RDI1I bit is set high when a change of RDI state event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI1I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

**RDI2I-RDI7I:**

The RDI2I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the RDI2I to RDI7I bits report and acknowledge RDI interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDIxI bit is set high

when a change of RDI state on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDIXI remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

**Register 13CH, 23CH, 33CH: RTOP, TU3 Auxiliary RDI Interrupt or TU #1 in  
TUG2 #1 to TUG2 #7 RFI Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RFI7I    | 0       |
| Bit 5 | R    | RFI6I    | 0       |
| Bit 4 | R    | RFI5I    | 0       |
| Bit 3 | R    | RFI4I    | 0       |
| Bit 2 | R    | RFI3I    | 0       |
| Bit 1 | R    | RFI2I    | 0       |
| Bit 0 | R    | RFI1I    | 0       |

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 auxiliary remote defect indication interrupts.

**RFI1I:**

The RFI1I bit identify the source of remote defect indication interrupts. In TU3 mode, the RFI1I bit reports and acknowledges auxiliary RDI interrupt of the TU3 stream. Out of TU3 mode, the RFI1I bit reports and acknowledges RFI interrupt of TU #1 in TUG2 #1. Interrupts are generated when the received RFI state changes. The RFI1I bit is set high when a change of RDI state event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI1I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote defect indication events.

**RFI2I-RFI7I:**

The RFI2I to RFI7I bits identify the source of remote failure indication interrupts. RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFIxI bit is set high when a change of RFI state on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared

immediately following a read of this register, which also acknowledges and clears the interrupt. RFlxl remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

### Register 13DH, 23DH, 33DH: RTOP, TU #1 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | IBER7    | 0       |
| Bit 5 | R/W  | IBER6    | 0       |
| Bit 4 | R/W  | IBER5    | 0       |
| Bit 3 | R/W  | IBER4    | 0       |
| Bit 2 | R/W  | IBER3    | 0       |
| Bit 1 | R/W  | IBER2    | 0       |
| Bit 0 | R/W  | IBER1    | 0       |

This register enables the inband error reporting mode of the tributaries TU #1 in TUG2 #1 to TUG2 #7.

#### IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #1 in TUG2 #1 to TUG2 #7, respectively. Setting an IBERx bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of the corresponding TUG2. When an IBERx bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of the corresponding TUG2 is not modified.

**Register 13EH, 23EH, 33EH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7,  
Controllable Output Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | COUT7    | 0       |
| Bit 5 | R/W  | COUT6    | 0       |
| Bit 4 | R/W  | COUT5    | 0       |
| Bit 3 | R/W  | COUT4    | 0       |
| Bit 2 | R/W  | COUT3    | 0       |
| Bit 1 | R/W  | COUT2    | 0       |
| Bit 0 | R/W  | COUT1    | 0       |

This register controls the configurable output (COUT) output for the tributaries TU #1 in TUG2 #1 to TUG2 #7 and COUT output for the TU3 mode.

**COUT1:**

The COUT1 bit controls the COUT output for tributary TU #1 in TUG2 #1 or TU3 in a TUG3. In TU3 mode, setting the COUT1 high will cause the COUT output to be set high when the incoming data stream is part of the TU3 in a TUG3. In non-TU3 modes, setting the COUT1 high will cause the COUT output to be high when the incoming data stream is part of tributary TU #1 in TUG2 #1. When COUT1 is set low, the COUT output will be low when the incoming data stream is part of tributary TU #1 in TUG2 #1 or a TU3 in a TUG3.

**COUT2-COUT7:**

The COUT2 to COUT7 bits control the COUT output for tributary TU #1 in TUG2 #2 to TUG2 #7, respectively. Setting a COUTx bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #1 of the corresponding TUG2. When an COUTx bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #1 of the corresponding TUG2.

**Register 140H, 148H, 150H, 158H, 160H, 168H, 170H:  
Register 240H, 248H, 250H, 258H, 260H, 268H, 270H:  
Register 340H, 348H, 350H, 358H, 360H, 368H, 370H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | BLKBIP    | 0       |
| Bit 4 | R/W  | PSLUE     | 0       |
| Bit 3 | R/W  | PSLME     | 0       |
| Bit 2 | R/W  | COPSLE    | 0       |
| Bit 1 | R/W  | RFIE      | 0       |
| Bit 0 | R/W  | RDIE      | 0       |

This set of registers configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

#### RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

#### RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set



low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

#### COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #2 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

#### PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #2 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

#### PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #2 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

#### BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #2 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 141H, 149H, 151H, 159H, 161H, 169H, 171H:  
Register 241H, 249H, 251H, 259H, 261H, 269H, 271H:  
Register 341H, 349H, 351H, 359H, 361H, 369H, 371H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status**

| Bit   | Type | Function      | Default |
|-------|------|---------------|---------|
| Bit 7 | R/W  | RDIZ7EN       | 0       |
| Bit 6 | R/W  | TUPTE         | 0       |
| Bit 5 | R/W  | PDIVEN        | 0       |
| Bit 4 | R    | PSLUV         | X       |
| Bit 3 | R    | PSLMV         | X       |
| Bit 2 | R    | ERDIV[2]      | X       |
| Bit 1 | R    | ERDIV[1]/RFIV | X       |
| Bit 0 | R    | ERDIV[0]/RDIV | X       |

This set of registers reports alarm status and configures TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

#### RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

#### RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers

(addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

#### ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

#### PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #2 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

#### PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #2 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

#### PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #2 in the corresponding TUG2. The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] input for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

#### TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #2 in the corresponding TUG2. TUPTE is set high if tributary

TU #2 is to be terminated in the network element containing this TUPP+622 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #2 is part of the through traffic in the network element containing this TUPP+622 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

**RDIZ7EN:**

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #2 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

**Register 142H, 14AH, 152H, 15AH, 162H, 16AH, 172H:  
Register 242H, 24AH, 252H, 25AH, 262H, 26AH, 272H:  
Register 342H, 34AH, 352H, 35AH, 362H, 36AH, 372H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Expected Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R/W  | EPSL[2]  | 0       |
| Bit 1 | R/W  | EPSL[1]  | 0       |
| Bit 0 | R/W  | EPSL[0]  | 0       |

This set of registers configures the expected path signal label of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

#### EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #2 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

**Register 143H, 14BH, 153H, 15BH, 163H, 16BH, 173H:  
Register 243H, 24BH, 253H, 25BH, 263H, 26BH, 273H:  
Register 343H, 34BH, 353H, 35BH, 363H, 36BH, 373H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | APSL[2]  | 0       |
| Bit 1 | R    | APSL[1]  | 0       |
| Bit 0 | R    | APSL[0]  | 0       |

This set of registers reports the accepted path signal label of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

#### APSL[2:0]:

The APSL[2:0] bits report the accepted path signal label of tributary TU #2 in TUG2 #1 to TUG2 #7. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

**Register 144H, 14CH, 154H, 15CH, 164H, 16CH, 174H:  
Register 244H, 24CH, 254H, 25CH, 264H, 26CH, 274H:  
Register 344H, 34CH, 354H, 35CH, 364H, 36CH, 374H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BIP[7]   | X       |
| Bit 6 | R    | BIP[6]   | X       |
| Bit 5 | R    | BIP[5]   | X       |
| Bit 4 | R    | BIP[4]   | X       |
| Bit 3 | R    | BIP[3]   | X       |
| Bit 2 | R    | BIP[2]   | X       |
| Bit 1 | R    | BIP[1]   | X       |
| Bit 0 | R    | BIP[0]   | X       |

**Register 145H, 14DH, 155H, 15DH, 165H, 16DH, 175H:  
Register 245H, 24DH, 255H, 25DH, 265H, 26DH, 275H:  
Register 345H, 34DH, 355H, 35DH, 365H, 36DH, 375H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | BIP[10]  | X       |
| Bit 1 | R    | BIP[9]   | X       |
| Bit 0 | R    | BIP[8]   | X       |



These registers report the number of block interleave parity (BIP-2) errors detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the data in associated registers are invalid. These registers do not saturate.

**BIP[10:0]:**

The BIP[10:0] bits report the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10  $\mu$ s and resets the internal counter simultaneously to begin a new cycle of error accumulation.

**Register 146H, 14EH, 156H, 15EH, 166H, 16EH, 176H:  
Register 246H, 24EH, 256H, 25EH, 266H, 26EH, 276H:  
Register 346H, 34EH, 356H, 35EH, 366H, 36EH, 376H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, REI Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | REI[7]   | X       |
| Bit 6 | R    | REI[6]   | X       |
| Bit 5 | R    | REI[5]   | X       |
| Bit 4 | R    | REI[4]   | X       |
| Bit 3 | R    | REI[3]   | X       |
| Bit 2 | R    | REI[2]   | X       |
| Bit 1 | R    | REI[1]   | X       |
| Bit 0 | R    | REI[0]   | X       |

**Register 147H, 14FH, 157H, 15FH, 167H, 16FH, 177H:  
Register 247H, 24FH, 257H, 25FH, 267H, 26FH, 277H:  
Register 347H, 34FH, 357H, 35FH, 367H, 36FH, 377H:  
RTOP, TU #2 in TUG2 #1 to TUG2 #7, REI Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | REI[10]  | X       |
| Bit 1 | R    | REI[9]   | X       |
| Bit 0 | R    | REI[8]   | X       |

These registers report the number of remote error indications (REI) detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated registers in this set contain invalid data.

**REI[10:0]:**

The REI[10:0] bits report the number of tributary path remote error indications that have been detected since the last time the REI registers were polled. The REI registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger registers. The write access transfers the internally accumulated error count to the REI registers within 10  $\mu$ s and resets the internal counter simultaneously to begin a new cycle of error accumulation.

**Register 178H, 278H, 378H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, COPSL  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | COPSL7I  | 0       |
| Bit 5 | R    | COPSL6I  | 0       |
| Bit 4 | R    | COPSL5I  | 0       |
| Bit 3 | R    | COPSL4I  | 0       |
| Bit 2 | R    | COPSL3I  | 0       |
| Bit 1 | R    | COPSL2I  | 0       |
| Bit 0 | R    | COPSL1I  | 0       |

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**COPSL1I-COPSL7I:**

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated COPSLxI bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSLxI bit is set high when a change of PSL event on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSLxI remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

**Register 179H, 279H, 379H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLM  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLM7I   | 0       |
| Bit 5 | R    | PSLM6I   | 0       |
| Bit 4 | R    | PSLM5I   | 0       |
| Bit 3 | R    | PSLM4I   | 0       |
| Bit 2 | R    | PSLM3I   | 0       |
| Bit 1 | R    | PSLM2I   | 0       |
| Bit 0 | R    | PSLM1I   | 0       |

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**PSLM1I-PSLM7I:**

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated PSLMxI bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLMxI bit is set high when a change of PSL matched state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLMxI remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

**Register 17AH, 27AH, 37AH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLU  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLU7I   | 0       |
| Bit 5 | R    | PSLU6I   | 0       |
| Bit 4 | R    | PSLU5I   | 0       |
| Bit 3 | R    | PSLU4I   | 0       |
| Bit 2 | R    | PSLU3I   | 0       |
| Bit 1 | R    | PSLU2I   | 0       |
| Bit 0 | R    | PSLU1I   | 0       |

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**PSLU1I-PSLU7I:**

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated PSLUxI bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLUxI bit is set high when a change of PSL unstable state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLUxI remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

**Register 17BH, 27BH, 37BH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RDI  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RDI7I    | 0       |
| Bit 5 | R    | RDI6I    | 0       |
| Bit 4 | R    | RDI5I    | 0       |
| Bit 3 | R    | RDI4I    | 0       |
| Bit 2 | R    | RDI3I    | 0       |
| Bit 1 | R    | RDI2I    | 0       |
| Bit 0 | R    | RDI1I    | 0       |

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**RDI1I-RDI7I:**

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated RDI<sub>xl</sub> bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI<sub>xl</sub> bit is set high when a change of RDI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI<sub>xl</sub> remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

**Register 17CH, 27CH, 37CH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RFI  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RFI7I    | 0       |
| Bit 5 | R    | RFI6I    | 0       |
| Bit 4 | R    | RFI5I    | 0       |
| Bit 3 | R    | RFI4I    | 0       |
| Bit 2 | R    | RFI3I    | 0       |
| Bit 1 | R    | RFI2I    | 0       |
| Bit 0 | R    | RFI1I    | 0       |

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**RFI1I-RFI7I:**

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated RFIxI bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFIxI bit is set high when a change of RFI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFIxI remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.



**Register 17DH, 27DH, 37DH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | IBER7    | 0       |
| Bit 5 | R/W  | IBER6    | 0       |
| Bit 4 | R/W  | IBER5    | 0       |
| Bit 3 | R/W  | IBER4    | 0       |
| Bit 2 | R/W  | IBER3    | 0       |
| Bit 1 | R/W  | IBER2    | 0       |
| Bit 0 | R/W  | IBER1    | 0       |

This register enables the inband error reporting mode for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**IBER1-IBER7:**

The IBER1 to IBER7 bits control in band error reporting for tributary TU #2 in TUG2 #1 to TUG2 #7, respectively. Setting an IBERx bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #2 of the corresponding TUG2. When an IBERx bit is low, in band error reporting is disabled and the V5 byte of tributary TU #2 of the corresponding TUG2 is not modified.

**Register 17EH, 27EH, 37EH: TU #2 in TUG2 #1 to TUG2 #7, Controllable Output Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | COUT7    | 0       |
| Bit 5 | R/W  | COUT6    | 0       |
| Bit 4 | R/W  | COUT5    | 0       |
| Bit 3 | R/W  | COUT4    | 0       |
| Bit 2 | R/W  | COUT3    | 0       |
| Bit 1 | R/W  | COUT2    | 0       |
| Bit 0 | R/W  | COUT1    | 0       |

This register controls the COUT output for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**COUT1-COUT7:**

The COUT1 to COUT7 bits control the COUT output for tributary TU #2 in TUG2 #1 to TUG2 #7, respectively. Setting a COUTx bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #2 of the corresponding TUG2. When an COUTx bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #2 of the corresponding TUG2.

**Register 180H, 188H, 190H, 198H, 1A0H, 1A8H, 1B0H:  
Register 280H, 288H, 290H, 298H, 2A0H, 2A8H, 2B0H:  
Register 380H, 388H, 390H, 398H, 3A0H, 3A8H, 3B0H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | BLKBIP    | 0       |
| Bit 4 | R/W  | PSLUE     | 0       |
| Bit 3 | R/W  | PSLME     | 0       |
| Bit 2 | R/W  | COPSLE    | 0       |
| Bit 1 | R/W  | RFIE      | 0       |
| Bit 0 | R/W  | RDIE      | 0       |

This set of registers configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

#### RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

#### RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set

low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

#### COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #3 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

#### PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #3 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

#### PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #3 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

#### BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #3 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 181H, 189H, 191H, 199H, 1A1H, 1A9H, 1B1H:  
Register 281H, 289H, 291H, 299H, 2A1H, 2A9H, 2B1H:  
Register 381H, 389H, 391H, 399H, 3A1H, 3A9H, 3B1H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status**

| Bit   | Type | Function      | Default |
|-------|------|---------------|---------|
| Bit 7 | R/W  | RDIZ7EN       | 0       |
| Bit 6 | R/W  | TUPTE         | 0       |
| Bit 5 | R/W  | PDIVEN        | 0       |
| Bit 4 | R    | PSLUV         | X       |
| Bit 3 | R    | PSLMV         | X       |
| Bit 2 | R    | ERDIV[2]      | X       |
| Bit 1 | R    | ERDIV[1]/RFIV | X       |
| Bit 0 | R    | ERDIV[0]/RDIV | X       |

This set of registers reports alarm status and configures TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

#### RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

#### RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers

(addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

#### ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

#### PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #3 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

#### PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #3 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

#### PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #3 in the corresponding TUG2. The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] input for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

#### TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #3 in the corresponding TUG2. TUPTE is set high if tributary

TU #3 is to be terminated in the network element containing this TUPP+622 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #3 is part of the through traffic in the network element containing this TUPP+622 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

**RDIZ7EN:**

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #3 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.



**Register 182H, 18AH, 192H, 19AH, 1A2H, 1AAH, 1B2H:  
Register 282H, 28AH, 292H, 29AH, 2A2H, 2AAH, 2B2H:  
Register 382H, 38AH, 392H, 39AH, 3A2H, 3AAH, 3B2H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Expected Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R/W  | EPSL[2]  | 0       |
| Bit 1 | R/W  | EPSL[1]  | 0       |
| Bit 0 | R/W  | EPSL[0]  | 0       |

This set of registers configures the expected the path signal label of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

#### EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #3 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

**Register 183H, 18BH, 193H, 19BH, 1A3H, 1ABH, 1B3H:  
Register 283H, 28BH, 293H, 29BH, 2A3H, 2ABH, 2B3H:  
Register 383H, 38BH, 393H, 39BH, 3A3H, 3ABH, 3B3H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | APSL[2]  | 0       |
| Bit 1 | R    | APSL[1]  | 0       |
| Bit 0 | R    | APSL[0]  | 0       |

This set of registers reports the accepted the path signal label of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

#### APSL[2:0]:

The APSL[2:0] bits report the accepted path signal label of tributary TU #3 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

**Register 184H, 18CH, 194H, 19CH, 1A4H, 1ACH, 1B4H:  
Register 284H, 28CH, 294H, 29CH, 2A4H, 2ACH, 2B4H:  
Register 384H, 38CH, 394H, 39CH, 3A4H, 3ACH, 3B4H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BIP[7]   | X       |
| Bit 6 | R    | BIP[6]   | X       |
| Bit 5 | R    | BIP[5]   | X       |
| Bit 4 | R    | BIP[4]   | X       |
| Bit 3 | R    | BIP[3]   | X       |
| Bit 2 | R    | BIP[2]   | X       |
| Bit 1 | R    | BIP[1]   | X       |
| Bit 0 | R    | BIP[0]   | X       |

**Register 185H, 18DH, 195H, 19DH, 1A5H, 1ADH, 1B5H:  
Register 285H, 28DH, 295H, 29DH, 2A5H, 2ADH, 2B5H:  
Register 385H, 38DH, 395H, 39DH, 3A5H, 3ADH, 3B5H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | BIP[10]  | X       |
| Bit 1 | R    | BIP[9]   | X       |
| Bit 0 | R    | BIP[8]   | X       |

These registers report the number of block interleave parity (BIP-2) errors detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the data in the associated registers are invalid. These registers do not saturate.

**BIP[10:0]:**

The BIP[10:0] bits report the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10  $\mu$ s and resets the internal counter simultaneously to begin a new cycle of error accumulation.

**Register 186H, 18EH, 196H, 19EH, 1A6H, 1AEH, 1B6H:  
Register 286H, 28EH, 296H, 29EH, 2A6H, 2AEH, 2B6H:  
Register 386H, 38EH, 396H, 39EH, 3A6H, 3AEH, 3B6H:  
TU #3 in TUG2 #1 to TUG2 #7, REI Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | REI[7]   | X       |
| Bit 6 | R    | REI[6]   | X       |
| Bit 5 | R    | REI[5]   | X       |
| Bit 4 | R    | REI[4]   | X       |
| Bit 3 | R    | REI[3]   | X       |
| Bit 2 | R    | REI[2]   | X       |
| Bit 1 | R    | REI[1]   | X       |
| Bit 0 | R    | REI[0]   | X       |

**Register 187H, 18FH, 197H, 19FH, 1A7H, 1AFH, 1B7H:  
Register 287H, 28FH, 297H, 29FH, 2A7H, 2AFH, 2B7H:  
Register 387H, 38FH, 397H, 39FH, 3A7H, 3AFH, 3B7H:  
RTOP, TU #3 in TUG2 #1 to TUG2 #7, REI Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | REI[10]  | X       |
| Bit 1 | R    | REI[9]   | X       |
| Bit 0 | R    | REI[8]   | X       |

These registers report the number of remote error indications (REI) detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated registers in this set contain invalid data.

**REI[10:0]:**

The REI[10:0] bits report the number of tributary path remote error indications that have been detected since the last time the REI registers were polled. The REI registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the REI registers within 10  $\mu$ s and resets the internal counter simultaneously to begin a new cycle of error accumulation.

**Register 1B8H, 2B8H, 3B8H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, COPSL  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Reserved | X       |
| Bit 6 | R    | COPSL7I  | 0       |
| Bit 5 | R    | COPSL6I  | 0       |
| Bit 4 | R    | COPSL5I  | 0       |
| Bit 3 | R    | COPSL4I  | 0       |
| Bit 2 | R    | COPSL3I  | 0       |
| Bit 1 | R    | COPSL2I  | 0       |
| Bit 0 | R    | COPSL1I  | 0       |

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

**COPSL1I-COPSL7I:**

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated COPSLxI bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSLxI bit is set high when a change of PSL event on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSLxI remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

**Reserved:**

The Reserved bits must be written with a logic 0 for proper operation of the TUPP+622.

**Register 1B9H, 2B9H, 3B9H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLM  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLM7I   | 0       |
| Bit 5 | R    | PSLM6I   | 0       |
| Bit 4 | R    | PSLM5I   | 0       |
| Bit 3 | R    | PSLM4I   | 0       |
| Bit 2 | R    | PSLM3I   | 0       |
| Bit 1 | R    | PSLM2I   | 0       |
| Bit 0 | R    | PSLM1I   | 0       |

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

**PSLM1I-PSLM7I:**

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated PSLMxI bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLMxI bit is set high when a change of PSL matched state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLMxI remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.



**Register 1BAH, 2BAH, 3BAH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLU  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLU7I   | 0       |
| Bit 5 | R    | PSLU6I   | 0       |
| Bit 4 | R    | PSLU5I   | 0       |
| Bit 3 | R    | PSLU4I   | 0       |
| Bit 2 | R    | PSLU3I   | 0       |
| Bit 1 | R    | PSLU2I   | 0       |
| Bit 0 | R    | PSLU1I   | 0       |

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

**PSLU1I-PSLU7I:**

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated PSLUxI bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLUxI bit is set high when a change of PSL unstable state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLUxI remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

**Register 1BBH, 2BBH, 3BBH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RDI  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RDI7I    | 0       |
| Bit 5 | R    | RDI6I    | 0       |
| Bit 4 | R    | RDI5I    | 0       |
| Bit 3 | R    | RDI4I    | 0       |
| Bit 2 | R    | RDI3I    | 0       |
| Bit 1 | R    | RDI2I    | 0       |
| Bit 0 | R    | RDI1I    | 0       |

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

**RDI1I-RDI7I:**

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated RDIxI bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDIxI bit is set high when a change of RDI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDIxI remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

**Register 1BCH, 2BCH, 3BCH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RFI  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RFI7I    | 0       |
| Bit 5 | R    | RFI6I    | 0       |
| Bit 4 | R    | RFI5I    | 0       |
| Bit 3 | R    | RFI4I    | 0       |
| Bit 2 | R    | RFI3I    | 0       |
| Bit 1 | R    | RFI2I    | 0       |
| Bit 0 | R    | RFI1I    | 0       |

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

**RFI1I-RFI7I:**

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated RFI<sub>x</sub>I bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI<sub>x</sub>I bit is set high when a change of RFI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI<sub>x</sub>I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

**Register 1BDH, 2BDH, 3BDH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | IBER7    | 0       |
| Bit 5 | R/W  | IBER6    | 0       |
| Bit 4 | R/W  | IBER5    | 0       |
| Bit 3 | R/W  | IBER4    | 0       |
| Bit 2 | R/W  | IBER3    | 0       |
| Bit 1 | R/W  | IBER2    | 0       |
| Bit 0 | R/W  | IBER1    | 0       |

This register enables the inband error reporting mode for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

**IBER1-IBER7:**

The IBER1 to IBER7 bits control in band error reporting for tributary TU #3 in TUG2 #1 to TUG2 #7, respectively. Setting an IBERx bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #3 of the corresponding TUG2. When an IBERx bit is low, in band error reporting is disabled and the V5 byte of tributary TU #3 of the corresponding TUG2 is not modified.

**Register 1BEH, 2BEH, 3BEH: RTOP, TU #3 in TUG2 #1 to TUG2 #7,  
Controllable Output Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | COUT7    | 0       |
| Bit 5 | R/W  | COUT6    | 0       |
| Bit 4 | R/W  | COUT5    | 0       |
| Bit 3 | R/W  | COUT4    | 0       |
| Bit 2 | R/W  | COUT3    | 0       |
| Bit 1 | R/W  | COUT2    | 0       |
| Bit 0 | R/W  | COUT1    | 0       |

This register controls the COUT output for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

**COUT1-COUT7:**

The COUT1 to COUT7 bits control the COUT output for tributary TU #3 in TUG2 #1 to TUG2 #7, respectively. Setting a COUTx bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #3 of the corresponding TUG2. When an COUTx bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #3 of the corresponding TUG2.

**Register 1C0H, 1C8H, 1D0H, 1D8H, 1E0H, 1E8H, 1F0H:  
Register 2C0H, 2C8H, 2D0H, 2D8H, 2E0H, 2E8H, 2F0H:  
Register 3C0H, 3C8H, 3D0H, 3D8H, 3E0H, 3E8H, 3F0H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | BLKBIP    | 0       |
| Bit 4 | R/W  | PSLUE     | 0       |
| Bit 3 | R/W  | PSLME     | 0       |
| Bit 2 | R/W  | COPSLE    | 0       |
| Bit 1 | R/W  | RFIE      | 0       |
| Bit 0 | R/W  | RDIE      | 0       |

This set of registers configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

#### RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #4 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RDIV bit when RDIE is set high. Interrupts due to RDIV status change are masked when RDIE is set low.

When RDIZ7EN is set high, an interrupt is generated upon assertion or negation events of the ERDIV[2:0] bits when RDIE is set high. Interrupts due to ERDIV[2:0] status change are masked when RDIE is set low.

#### COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #4 in the corresponding TUG2. When COPSLE is set high, an

interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

### PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #4 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

### PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #4 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

### BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #4 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 1C1H, 1C9H, 1D1H, 1D9H, 1E1H, 1E9H, 1F1H:  
Register 2C1H, 2C9H, 2D1H, 2D9H, 2E1H, 2E9H, 2F1H:  
Register 3C1H, 3C9H, 3D1H, 3D9H, 3E1H, 3E9H, 3F1H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status**

| Bit   | Type | Function      | Default |
|-------|------|---------------|---------|
| Bit 7 | R/W  | RDIZ7EN       | 0       |
| Bit 6 | R/W  | TUPTE         | 0       |
| Bit 5 | R/W  | PDIVEN        | 0       |
| Bit 4 | R    | PSLUV         | X       |
| Bit 3 | R    | PSLMV         | X       |
| Bit 2 | R    | ERDIV[2]      | X       |
| Bit 1 | R    | ERDIV[1]/RFIV | X       |
| Bit 0 | R    | ERDIV[0]/RDIV | X       |

This set of registers configures and reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

#### RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

#### RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers



(addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

#### ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

#### PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #4 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

#### PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #4 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

#### PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #4 in the corresponding TUG2. The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] input for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

#### TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #4 in the corresponding TUG2. TUPTE is set high if tributary

TU #4 is to be terminated in the network element containing this TUPP+622 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #4 is part of the through traffic in the network element containing this TUPP+622 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

**RDIZ7EN:**

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #4 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

**Register 1C2H, 1CAH, 1D2H, 1DAH, 1E2H, 1EAH, 1F2H:  
Register 2C2H, 2CAH, 2D2H, 2DAH, 2E2H, 2EAH, 2F2H:  
Register 3C2H, 3CAH, 3D2H, 3DAH, 3E2H, 3EAH, 3F2H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Expected Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R/W  | EPSL[2]  | 0       |
| Bit 1 | R/W  | EPSL[1]  | 0       |
| Bit 0 | R/W  | EPSL[0]  | 0       |

This set of registers configures the expected path signal label of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

#### EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #4 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

**Register 1C3H, 1CBH, 1D3H, 1DBH, 1E3H, 1EBH, 1F3H:  
Register 2C3H, 2CBH, 2D3H, 2DBH, 2E3H, 2EBH, 2F3H:  
Register 3C3H, 3CBH, 3D3H, 3DBH, 3E3H, 3EBH, 3F3H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Path Signal Label**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | APSL[2]  | 0       |
| Bit 1 | R    | APSL[1]  | 0       |
| Bit 0 | R    | APSL[0]  | 0       |

This set of register reports the accepted path signal label of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

#### APSL[2:0]:

The APSL[2:0] bits report the accepted path signal label of tributary TU #4 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

**Register 1C4H, 1CCH, 1D4H, 1DCH, 1E4H, 1ECH, 1F4H:  
Register 2C4H, 2CCH, 2D4H, 2DCH, 2E4H, 2ECH, 2F4H:  
Register 3C4H, 3CCH, 3D4H, 3DCH, 3E4H, 3ECH, 3F4H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BIP[7]   | X       |
| Bit 6 | R    | BIP[6]   | X       |
| Bit 5 | R    | BIP[5]   | X       |
| Bit 4 | R    | BIP[4]   | X       |
| Bit 3 | R    | BIP[3]   | X       |
| Bit 2 | R    | BIP[2]   | X       |
| Bit 1 | R    | BIP[1]   | X       |
| Bit 0 | R    | BIP[0]   | X       |

**Register 1C5H, 1CDH, 1D5H, 1DDH, 1E5H, 1EDH, 1F5H:  
Register 2C5H, 2CDH, 2D5H, 2DDH, 2E5H, 2EDH, 2F5H:  
Register 3C5H, 3CDH, 3D5H, 3DDH, 3E5H, 3EDH, 3F5H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | BIP[10]  | X       |
| Bit 1 | R    | BIP[9]   | X       |
| Bit 0 | R    | BIP[8]   | X       |

These registers report the number of block interleave parity (BIP-2) errors detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated registers in this set contain invalid data. These registers do not saturate.

**BIP[10:0]:**

The BIP[10:0] bits report the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10  $\mu$ s and resets the internal counter simultaneously to begin a new cycle of error accumulation.

**Register 1C6H, 1CEH, 1D6H, 1DEH, 1E6H, 1EEH, 1F6H:  
Register 2C6H, 2CEH, 2D6H, 2DEH, 2E6H, 2EEH, 2F6H:  
Register 3C6H, 3CEH, 3D6H, 3DEH, 3E6H, 3EEH, 3F6H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, REI Error Count LSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | REI[7]   | X       |
| Bit 6 | R    | REI[6]   | X       |
| Bit 5 | R    | REI[5]   | X       |
| Bit 4 | R    | REI[4]   | X       |
| Bit 3 | R    | REI[3]   | X       |
| Bit 2 | R    | REI[2]   | X       |
| Bit 1 | R    | REI[1]   | X       |
| Bit 0 | R    | REI[0]   | X       |

**Register 1C7H, 1CFH, 1D7H, 1DFH, 1E7H, 1EFH, 1F7H:  
Register 2C7H, 2CFH, 2D7H, 2DFH, 2E7H, 2EFH, 2F7H:  
Register 3C7H, 3CFH, 3D7H, 3DFH, 3E7H, 3EFH, 3F7H:  
RTOP, TU #4 in TUG2 #1 to TUG2 #7, REI Error Count MSB**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | R    | REI[10]  | X       |
| Bit 1 | R    | REI[9]   | X       |
| Bit 0 | R    | REI[8]   | X       |

These registers report the number of remote error indications (REI) detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated registers in this set contain invalid data.

**REI[10:0]:**

The REI[10:0] bits report the number of tributary path remote error indications that have been detected since the last time the REI registers were polled. The REI registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the REI registers within 10  $\mu$ s and resets the internal counter simultaneously to begin a new cycle of error accumulation.



**Register 1F8H, 2F8H, 3F8H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, COPSL  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | 0       |
| Bit 6 | R    | COPSL7I  | 0       |
| Bit 5 | R    | COPSL6I  | 0       |
| Bit 4 | R    | COPSL5I  | 0       |
| Bit 3 | R    | COPSL4I  | 0       |
| Bit 2 | R    | COPSL3I  | 0       |
| Bit 1 | R    | COPSL2I  | 0       |
| Bit 0 | R    | COPSL1I  | 0       |

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

**COPSL1I-COPSL7I:**

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated COPSLxI bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSLxI bit is set high when a change of PSL event on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSLxI remains valid when interrupts are not enabled (COPSLxI set low) and may be polled to detect change of path signal label events.

**Register 1F9H, 2F9H, 3F9H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLM  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLM7I   | 0       |
| Bit 5 | R    | PSLM6I   | 0       |
| Bit 4 | R    | PSLM5I   | 0       |
| Bit 3 | R    | PSLM4I   | 0       |
| Bit 2 | R    | PSLM3I   | 0       |
| Bit 1 | R    | PSLM2I   | 0       |
| Bit 0 | R    | PSLM1I   | 0       |

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

**PSLM1I-PSLM7I:**

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated PSLMxI bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLMxI bit is set high when a change of PSL matched state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLMxI remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

**Register 1FAH, 2FAH, 3FAH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLU  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | PSLU7I   | 0       |
| Bit 5 | R    | PSLU6I   | 0       |
| Bit 4 | R    | PSLU5I   | 0       |
| Bit 3 | R    | PSLU4I   | 0       |
| Bit 2 | R    | PSLU3I   | 0       |
| Bit 1 | R    | PSLU2I   | 0       |
| Bit 0 | R    | PSLU1I   | 0       |

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

**PSLU1I-PSLU7I:**

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated PSLUxI bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLUxI bit is set high when a change of PSL unstable state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLUxI remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

**Register 1FBH, 2FBH, 3FBH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RDI  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RDI7I    | 0       |
| Bit 5 | R    | RDI6I    | 0       |
| Bit 4 | R    | RDI5I    | 0       |
| Bit 3 | R    | RDI4I    | 0       |
| Bit 2 | R    | RDI3I    | 0       |
| Bit 1 | R    | RDI2I    | 0       |
| Bit 0 | R    | RDI1I    | 0       |

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

**RDI1I-RDI7I:**

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated RDIxI bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDIxI bit is set high when a change of RDI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDIxI remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

**Register 1FCH, 2FCH, 3FCH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RFI  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | RFI7I    | 0       |
| Bit 5 | R    | RFI6I    | 0       |
| Bit 4 | R    | RFI5I    | 0       |
| Bit 3 | R    | RFI4I    | 0       |
| Bit 2 | R    | RFI3I    | 0       |
| Bit 1 | R    | RFI2I    | 0       |
| Bit 0 | R    | RFI1I    | 0       |

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

**RFI1I-RFI7I:**

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated RFIxI bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFIxI bit is set high when a change of RFI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFIxI remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

**Register 1FDH, 2FDH, 3FDH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | IBER7    | 0       |
| Bit 5 | R/W  | IBER6    | 0       |
| Bit 4 | R/W  | IBER5    | 0       |
| Bit 3 | R/W  | IBER4    | 0       |
| Bit 2 | R/W  | IBER3    | 0       |
| Bit 1 | R/W  | IBER2    | 0       |
| Bit 0 | R/W  | IBER1    | 0       |

This register enables the inband error reporting mode for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

**IBER1-IBER7:**

The IBER1 to IBER7 bits control in band error reporting for tributary TU #4 in TUG2 #1 to TUG2 #7, respectively. Setting an IBERx bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #4 of the corresponding TUG2. When an IBERx bit is low, in band error reporting is disabled and the V5 byte of tributary TU #4 of the corresponding TUG2 is not modified.

**Register 1FEH, 2FEH, 3FEH: RTOP, TU #4 in TUG2 #1 to TUG2 #7,  
Controllable Output Configuration**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | x       |
| Bit 6 | R/W  | COUT7    | 0       |
| Bit 5 | R/W  | COUT6    | 0       |
| Bit 4 | R/W  | COUT5    | 0       |
| Bit 3 | R/W  | COUT4    | 0       |
| Bit 2 | R/W  | COUT3    | 0       |
| Bit 1 | R/W  | COUT2    | 0       |
| Bit 0 | R/W  | COUT1    | 0       |

This register controls the COUT output for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

**COUT1-COUT7:**

The COUT1 to COUT7 bits control the COUT output for tributary TU #4 in TUG2 #1 to TUG2 #7, respectively. Setting a COUTx bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #4 of the corresponding TUG2. When an COUTx bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #4 of the corresponding TUG2.

**Register 1FFH, 2FFH, 3FFH: RTOP Status**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | Reserved | 0       |
| Bit 6 | R/W  | Reserved | 0       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 |      | Unused   | X       |
| Bit 1 | R/W  | BLKREI   | 0       |
| Bit 0 | R    | BUSY     | X       |

This register configures and reports the status of the various internal operations inside RTOP.

**BUSY:**

The BUSY bit indicates the status of the transfer of BIP and REI counts from the counters to the holding registers. BUSY is set high when the STP Input Signal Activity Monitor #1, Accumulation Trigger register is being written. BUSY is set low when all the counters values have been transferred to holding registers. The elapsed time shall be less than 10  $\mu$ s.

**BLKREI:**

The block REI accumulation control bit selects between counting of REIs in the incoming TU3 stream on a block or bit basis. When BLKREI is set high, REI count codes in the range of 1 to 8 are accumulated on a block basis as a single REI event. All other codes are counted zero events. When BLKREI is set low, REI count codes in the range of 1 to 8 are accumulated on a bit basis as a up to 8 REI events. All other codes are counted zero events.

**Reserved:**

The Reserved bits must be written with a logic 0 for proper operation of the TUPP+622.



## **11.4 RTTB #1, RTTB #2 and RTTB #3 Registers**

### **Register 400H, 440H, 480H: RTTB, TU3 or TU #1 in TUG2 #1, Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | CONFIG[1] | 1       |
| Bit 6 | R/W  | CONFIG[0] | 1       |
| Bit 5 | R/W  | NOSYNC    | 0       |
| Bit 4 | R/W  | LEN16     | 0       |
| Bit 3 | R    | TIMV      | X       |
| Bit 2 | R/W  | TIME      | 0       |
| Bit 1 | R    | TIUV      | X       |
| Bit 0 | R/W  | TIUE      | 0       |

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the RTTB. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

#### **TIUE:**

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #1 in TUG2 #1 or TU3. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

#### **TIUV:**

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #1 in TUG2 #1 or TU3.

#### **TIME:**

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #1 in TUG2 #1 or TU3. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched

identifier. Interrupts due to TIM status change are masked when TIME is set low.

#### TIMV:

The TIUV bit indicates the trail trace identifier mismatch status of tributary TU #1 in TUG2 #1 or TU3.

#### LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #1 in TUG2 #1 or TU3. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

#### NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #1 in TUG2 #1 or TU3. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 401H-406H, 441H-446H, 481H-486H: RTTB, TU #1 in TUG2 #2 to  
TUG2 #7, Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R/W  | CONFIG[1] | 1       |
| Bit 6 | R/W  | CONFIG[0] | 1       |
| Bit 5 | R/W  | NOSYNC    | 0       |
| Bit 4 | R/W  | LEN16     | 0       |
| Bit 3 | R    | TIMV      | X       |
| Bit 2 | R/W  | TIME      | 0       |
| Bit 1 | R    | TIUV      | X       |
| Bit 0 | R/W  | TIUE      | 0       |

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

**TIUE:**

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #1 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

**TIUV:**

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #1 in the corresponding TUG2.

**TIME:**

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #1 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

**TIMV:**

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #1 in the corresponding TUG2.

**LEN16:**

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #1 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

**NOSYNC:**

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #1 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

**CONFIG[1:0]:**

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 408H-40EH, 448H-44EH, 488H-48EH: RTTB, TU #2 in TUG2 #1 to  
TUG2 #7, Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | NOSYNC    | 0       |
| Bit 4 | R/W  | LEN16     | 0       |
| Bit 3 | R    | TIMV      | X       |
| Bit 2 | R/W  | TIME      | 0       |
| Bit 1 | R    | TIUV      | X       |
| Bit 0 | R/W  | TIUE      | 0       |

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

**TIUE:**

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #2 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

**TIUV:**

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #2 in the corresponding TUG2.

**TIME:**

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #2 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a

matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

#### TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #2 in the corresponding TUG2.

#### LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #2 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

#### NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #2 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 410H-416H, 450H-456H, 490H-496H: RTTB, TU #3 in TUG2 #1 to  
TUG2 #7, Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | NOSYNC    | 0       |
| Bit 4 | R/W  | LEN16     | 0       |
| Bit 3 | R    | TIMV      | X       |
| Bit 2 | R/W  | TIME      | 0       |
| Bit 1 | R    | TIUV      | X       |
| Bit 0 | R/W  | TIUE      | 0       |

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

**TIUE:**

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #3 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

**TIUV:**

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #3 in the corresponding TUG2.

**TIME:**

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #3 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a

matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

#### TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #3 in the corresponding TUG2.

#### LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #3 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

#### NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #3 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |



**Register 418H-41EH, 458H-45EH, 498H-49EH: RTTB, TU #4 in TUG2 #1 to  
TUG2 #7, Configuration and Status**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | R    | CONFIG[1] | 1       |
| Bit 6 | R    | CONFIG[0] | 1       |
| Bit 5 | R/W  | NOSYNC    | 0       |
| Bit 4 | R/W  | LEN16     | 0       |
| Bit 3 | R    | TIMV      | X       |
| Bit 2 | R/W  | TIME      | 0       |
| Bit 1 | R    | TIUV      | X       |
| Bit 0 | R/W  | TIUE      | 0       |

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or, TU12 (VT2) mode, the associated register in this set has no effect.

**TIUE:**

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #4 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

**TIUV:**

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #4 in the corresponding TUG2.

**TIME:**

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #4 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a

matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

#### TIMV:

The TIUV bit indicates the trail trace identifier mismatch status of tributary TU #4 in the corresponding TUG2.

#### LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #4 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

#### NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #4 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

#### CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

| CONFIG[1] | CONFIG[0] | Configuration | Active TU (VT) |
|-----------|-----------|---------------|----------------|
| 0         | 0         | TU2 (VT6)     | #1             |
| 0         | 1         | VT3           | #1, #2         |
| 1         | 0         | TU12 (VT2)    | #1, #2, #3     |
| 1         | 1         | TU11 (VT1.5)  | #1, #2, #3, #4 |

**Register 420H, 460H, 4A0H: RTTB, TU3 or TU #1 in TUG2 #1 to TUG2 #7,  
TIM Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIM7I    | 0       |
| Bit 5 | R    | TIM6I    | 0       |
| Bit 4 | R    | TIM5I    | 0       |
| Bit 3 | R    | TIM4I    | 0       |
| Bit 2 | R    | TIM3I    | 0       |
| Bit 1 | R    | TIM2I    | 0       |
| Bit 0 | R    | TIM1I    | 0       |

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 trail trace identifier mismatch interrupts.

**TIM1I:**

The TIM1I bit identifies the source of trail trace identifier mismatch interrupts. In TU3 mode, The TIM1I bit reports and acknowledges TIM interrupt of the TU3 trail trace identifier. Out of TU3 mode, TIM1I bit reports and acknowledges TIM interrupt of TU #1 in TUG2 #1. Interrupts are generated upon change of identifier mismatch state. The TIM1I bit is set high when a trail trace identifier mismatch event and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. the TIM1I bit remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

**TIM2I-TIM7I:**

The TIM2I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. TIM2I to TIM7I bits report and acknowledge TIM interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIMxI bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #1 in TUG2 #x) occurs

and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIMxl remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

**Register 421H, 461H, 4A1H: RTTB, TU #2 in TUG2 #1 to TUG2 #7, TIM  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIM7I    | 0       |
| Bit 5 | R    | TIM6I    | 0       |
| Bit 4 | R    | TIM5I    | 0       |
| Bit 3 | R    | TIM4I    | 0       |
| Bit 2 | R    | TIM3I    | 0       |
| Bit 1 | R    | TIM2I    | 0       |
| Bit 0 | R    | TIM1I    | 0       |

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**TIM1I-TIM7I:**

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated TIMxI bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIMxI bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIMxI remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

**Register 422H, 462H, 4A2H: RTTB, TU #3 in TUG2 #1 to TUG2 #7, TIM  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIM7I    | 0       |
| Bit 5 | R    | TIM6I    | 0       |
| Bit 4 | R    | TIM5I    | 0       |
| Bit 3 | R    | TIM4I    | 0       |
| Bit 2 | R    | TIM3I    | 0       |
| Bit 1 | R    | TIM2I    | 0       |
| Bit 0 | R    | TIM1I    | 0       |

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

**TIM1I-TIM7I:**

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated TIMxI bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIMxI bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIMxI remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

**Register 423H, 463H, 4A3H: RTTB, TU #4 in TUG2 #1 to TUG2 #7, TIM  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIM7I    | 0       |
| Bit 5 | R    | TIM6I    | 0       |
| Bit 4 | R    | TIM5I    | 0       |
| Bit 3 | R    | TIM4I    | 0       |
| Bit 2 | R    | TIM3I    | 0       |
| Bit 1 | R    | TIM2I    | 0       |
| Bit 0 | R    | TIM1I    | 0       |

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

**TIM1I-TIM7I:**

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated TIMxI bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIMxI bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIMxI remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

**Register 424H, 464H, 4A4H: RTTB, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIU Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIU7I    | 0       |
| Bit 5 | R    | TIU6I    | 0       |
| Bit 4 | R    | TIU5I    | 0       |
| Bit 3 | R    | TIU4I    | 0       |
| Bit 2 | R    | TIU3I    | 0       |
| Bit 1 | R    | TIU2I    | 0       |
| Bit 0 | R    | TIU1I    | 0       |

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 trail trace identifier unstable interrupts.

**TIU1I:**

The TIU1I bit identifies the source of trail trace identifier unstable interrupts. In TU3 mode, The TIU1I bit reports and acknowledges TIU interrupt of the TU3 trail trace identifier. Out of TU3 mode, TIU1I bit reports and acknowledges TIU interrupt of TU #1 in TUG2 #1. Interrupts are generated upon change of identifier unstable state. The TIU1I bit is set high when a trail trace identifier unstable event and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. the TIU1I bit remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

**TIU2I-TIU7I:**

The TIU2I to TIU7I bits identify the source of trail trace identifier unstable interrupts. TIU2I to TIU7I bits report and acknowledge TIU interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIUxI bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #1 in TUG2 #x ) occurs and



are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIUxl remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

**Register 425H, 465H, 4A5H: RTTB, TU #2 in TUG2 #1 to TUG2 #7, TIU  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIU7I    | 0       |
| Bit 5 | R    | TIU6I    | 0       |
| Bit 4 | R    | TIU5I    | 0       |
| Bit 3 | R    | TIU4I    | 0       |
| Bit 2 | R    | TIU3I    | 0       |
| Bit 1 | R    | TIU2I    | 0       |
| Bit 0 | R    | TIU1I    | 0       |

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

**TIU1I-TIU7I:**

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated TIUxI bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIUxI bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #2 in TUG2 #x ) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIUxI remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

**Register 426H, 466H, 4A6H: RTTB, TU #3 in TUG2 #1 to TUG2 #7, TIU  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIU7I    | 0       |
| Bit 5 | R    | TIU6I    | 0       |
| Bit 4 | R    | TIU5I    | 0       |
| Bit 3 | R    | TIU4I    | 0       |
| Bit 2 | R    | TIU3I    | 0       |
| Bit 1 | R    | TIU2I    | 0       |
| Bit 0 | R    | TIU1I    | 0       |

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

**TIU1I-TIU7I:**

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated TIUxI bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIUxI bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #3 in TUG2 #x ) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIUxI remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

**Register 427H, 467H, 4A7H: RTTB, TU #4 in TUG2 #1 to TUG2 #7, TIU  
Interrupt**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 | R    | TIU7I    | 0       |
| Bit 5 | R    | TIU6I    | 0       |
| Bit 4 | R    | TIU5I    | 0       |
| Bit 3 | R    | TIU4I    | 0       |
| Bit 2 | R    | TIU3I    | 0       |
| Bit 1 | R    | TIU2I    | 0       |
| Bit 0 | R    | TIU1I    | 0       |

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

**TIU1I-TIU7I:**

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated TIMxI bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIUxI bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #4 in TUG2 #x ) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIUxI remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

**Register 428H, 468H, 4A8H: RTTB, TIU Threshold**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | TIU64[3] | 0       |
| Bit 6 | R/W  | TIU64[2] | 1       |
| Bit 5 | R/W  | TIU64[1] | 1       |
| Bit 4 | R/W  | TIU64[0] | 1       |
| Bit 3 | R/W  | TIU16[3] | 0       |
| Bit 2 | R/W  | TIU16[2] | 1       |
| Bit 1 | R/W  | TIU16[1] | 1       |
| Bit 0 | R/W  | TIU16[0] | 1       |

This register contains threshold for declaration of the trail trace identifier unstable alarm (TIU) for 16-byte and 64-byte tributary path trace messages.

**TIU16[3:0]:**

The 16-byte message trail trace identifier unstable threshold bits (TIU16[3:0]) controls level in the unstable counter at which to declare TIU. When ALGO2 is set low, each time a received message differs from the previous message, the unstable counter is incremented. When the count exceeds TIU16, the TIU alarm is declared. When ALGO2 is set high, a message that differs from the previous initiates the unstable counter to count once per message. When the count exceeds TIU16, the TIU alarm is declared. TIU is negated and the unstable counter cleared when a consistent message is repeated three or five times, as controlled by the PER5 bit, to become the accepted message.

**TIU64[3:0]:**

The 64-byte message trail trace identifier unstable threshold bits (TIU64[3:0]) controls level in the unstable counter at which to declare TIU. When ALGO2 is set low, each time a received message differs from the previous message, the unstable counter is incremented. When the count exceeds TIU64, the TIU alarm is declared. When ALGO2 is set high, a message that differs from the previous initiates the unstable counter to count once per message. When the count exceeds TIU64, the TIU alarm is declared. TIU is negated and the

unstable counter cleared when a consistent message is repeated three or five times, as controlled by the PER5 bit, to become the accepted message.

**Register 429H, 469H, 4A9H: RTTB, Indirect Tributary Select**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | CPAGE    | 0       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 | R/W  | TUG2[2]  | 0       |
| Bit 3 | R/W  | TUG2[1]  | 0       |
| Bit 2 | R/W  | TUG2[0]  | 0       |
| Bit 1 | R/W  | TU[1]    | 0       |
| Bit 0 | R/W  | TU[0]    | 0       |

This register contains the identity of the tributary buffer to be accessed in an indirect read or write operation.

**TU[1:0]:**

The tributary unit address bits (TU[1:0]) identifies the tributary within the tributary unit group which is identified by the TUG2[2:0] bits. The combination of TUG2[2:0] and TU[1:0] identifies the tributary buffer to be accessed indirectly.

**TUG2[2:0]:**

The tributary unit group address bits (TUG2[2:0]) identifies the tributary unit group. The combination of TUG2[2:0] and TU[1:0] identifies the tributary buffer to be accessed indirectly.

**CPAGE:**

The capture page control bit (CPAGE) selects between accessing the capture page and the expected page of the tributary buffer. When CPAGE is set high, the indirect register access is targeted at the capture page. Reading from the capture page returns the most recent tributary path trace message received from the incoming stream. No de-bouncing is provided. When CPAGE is set low, the indirect register access is targeted at the expected page. An expected

trace message can be provisioned by writing to the expected page. Both the capture and expected pages may be read from or written to.



**Register 42AH, 46AH, 4AAH: RTTB, Indirect Address Select**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | BUSY     | 0       |
| Bit 6 | R/W  | RWB      | 0       |
| Bit 5 | R/W  | A[5]     | 0       |
| Bit 4 | R/W  | A[4]     | 0       |
| Bit 3 | R/W  | A[3]     | 0       |
| Bit 2 | R/W  | A[2]     | 0       |
| Bit 1 | R/W  | A[1]     | 0       |
| Bit 0 | R/W  | A[0]     | 0       |

This register provides the byte address within the tributary buffer addressed by the Indirect Tributary Select register. Writing to this register triggers an indirect register access..

**A[5:0]:**

The indirect address bits (A[5:0]) index into the receive and expected pages of the tributary buffers.

**RWB:**

The indirect access control bit (RWB) selects between a read and write operation into the tributary buffers. Writing a logic zero to RWB triggers an indirect write operation. The tributary buffer is selected by the TUG2[2:0] and TU[1:0] bits in the Indirect Tributary register. Selection between the capture page and the expected page is controlled by the CPAGE bit also in the Indirect Tributary register. Bytes within the tributary buffer are indexed by A[5:0]. Data to be written is taken from D[7:0] of the Indirect Data register. Writing a logic one to RWB triggers an indirect read operation. Tributary buffer, page, and byte addressing is the same as in an indirect write operation. The data read can be found in D[7:0] of the Indirect Data register.

**BUSY:**

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written to trigger an indirect access and will stay high until the access is complete. At which point, BUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence.

**Register 42BH, 46BH, 4ABH: RTTB, Indirect Data Select**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W  | D[7]     | 0       |
| Bit 6 | R/W  | D[6]     | 0       |
| Bit 5 | R/W  | D[5]     | 0       |
| Bit 4 | R/W  | D[4]     | 0       |
| Bit 3 | R/W  | D[3]     | 0       |
| Bit 2 | R/W  | D[2]     | 0       |
| Bit 1 | R/W  | D[1]     | 0       |
| Bit 0 | R/W  | D[0]     | 0       |

This register contains the data read from a tributary buffer after an indirect read operation or the data to be inserted into a tributary buffer in an indirect write operation.

**D[7:0]:**

The indirect data bits (D[7:0]) reports the data read from a tributary buffer after an indirect read operation has complete. Data to be written to a tributary buffer in an indirect write operation must be set up in this register before triggering the write. Data in this register reflects the value written until the completion of a subsequent indirect read operation.

## 12 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs when the MBEB input is negated (high), causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TUPP+622. Test mode registers (as opposed to normal mode registers) are selected when A[13] is high.

Test mode registers may also be used for board testing. When all of the tributary payload processors within the TUPP+622 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

**Table 3 - Test Mode Register Memory Map**

| STP #1      | STP #2      | STP #3      | STP #4      | Register                |
|-------------|-------------|-------------|-------------|-------------------------|
| 0000H-07FFH | 0800H-0FFFH | 1000H-17FFH | 1800H-1FFFH | Normal Mode Registers   |
| 2000H       |             |             |             | Master Test Register    |
| 2001H       |             |             |             | STP Select Register     |
| 2002H       | 2802H       | 3002H       | 3802H       | I/O Test register 1     |
| 2003H       | 2803H       | 3003H       | 3803H       | I/O Test register 2     |
| 2004H       | 2804H       | 3004H       | 3804H       | I/O Test register 3     |
| 2005H       | 2805H       | 3005H       | 3805H       | I/O Test register 4     |
| 2006H       | 2806H       | 3006H       | 3806H       | I/O Test register 5     |
| 2006H-201FH | 2806H-281FH | 3006H-301FH | 3806H-381FH | Reserved                |
| 2020H       | 2820H       | 3020H       | 3820H       | VTPP #1 Test Register 0 |
| 2021H       | 2821H       | 3021H       | 3821H       | VTPP #1 Test Register 2 |
| 2022H       | 2822H       | 3022H       | 3822H       | VTPP #1 Test Register 4 |

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| STP #1          | STP #2          | STP #3          | STP #4          | Register                |
|-----------------|-----------------|-----------------|-----------------|-------------------------|
| 2023H-<br>203FH | 2823H-<br>283FH | 3023H-<br>303FH | 3823H-<br>383FH | Reserved                |
| 20A0H           | 28A0H           | 30A0H           | 38A0H           | VTPP #1 Test Register 1 |
| 20A1H           | 28A1H           | 30A1H           | 38A1H           | VTPP #1 Test Register 3 |
| 20A2H           | 28A2H           | 30A2H           | 38A2H           | VTPP #1 Test Register 5 |
| 20A3H-<br>20BFH | 28A3H-<br>28BFH | 30A3H-<br>30BFH | 38A3H-<br>38BFH | Reserved                |
| 2040H           | 2840H           | 3040H           | 3840H           | VTPP #2 Test Register 0 |
| 2041H           | 2841H           | 3041H           | 3841H           | VTPP #2 Test Register 2 |
| 2042H           | 2842H           | 3042H           | 3842H           | VTPP #2 Test Register 4 |
| 2043H-<br>205FH | 2843H-<br>285FH | 3043H-<br>305FH | 3843H-<br>385FH | Reserved                |
| 20C0H           | 28C0H           | 30C0H           | 38C0H           | VTPP #2 Test Register 1 |
| 20C1H           | 28C1H           | 30C1H           | 38C1H           | VTPP #2 Test Register 3 |
| 20C2H           | 28C2H           | 30C2H           | 38C2H           | VTPP #2 Test Register 5 |
| 20C3H-<br>20DFH | 28C3H-<br>28DFH | 30C3H-<br>30DFH | 38C3H-<br>38DFH | Reserved                |
| 2060H           | 2860H           | 3060H           | 3860H           | VTPP #3 Test Register 0 |
| 2061H           | 2861H           | 3061H           | 3861H           | VTPP #3 Test Register 2 |
| 2062H           | 2862H           | 3062H           | 3862H           | VTPP #3 Test Register 4 |
| 2063H-<br>207FH | 2863H-<br>287FH | 3063H-<br>307FH | 3863H-<br>387FH | Reserved                |
| 20E0H           | 28E0H           | 30E0H           | 38E0H           | VTPP #3 Test Register 1 |
| 20E1H           | 28E1H           | 30E1H           | 38E1H           | VTPP #3 Test Register 3 |
| 20E2H           | 28E2H           | 30E2H           | 38E2H           | VTPP #3 Test Register 5 |
| 20E3H-<br>20FFH | 28E3H-<br>28FFH | 30E3H-<br>30FFH | 38E3H-<br>38FFH | Reserved                |

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| <b>STP #1</b>    | <b>STP #2</b>    | <b>STP #3</b>    | <b>STP #4</b>    | <b>Register</b>              |
|------------------|------------------|------------------|------------------|------------------------------|
| 2100H            | 2900H            | 3100H            | 3900H            | RTOP #1 Test Register 0      |
| 2101H            | 2901H            | 3101H            | 3901H            | RTOP #1 Test Register 1      |
| 2102H            | 2902H            | 3102H            | 3902H            | RTOP #1 Test Register 2      |
| 2103H            | 2903H            | 3103H            | 3903H            | RTOP #1 Test Register 3      |
| 2104H            | 2904H            | 3104H            | 3904H            | RTOP #1 Test Register 4      |
| 2105H            | 2905H            | 3105H            | 3905H            | RTOP #1 Test Register 5      |
| 2106H            | 2906H            | 3106H            | 3906H            | RTOP #1 Test Register 6      |
| 2107H            | 2907H            | 3107H            | 3907H            | RTOP #1 Test Register 7      |
| 2108H            | 2908H            | 3108H            | 3908H            | RTOP #1 Test Register 8      |
| 2109H            | 2909H            | 3109H            | 3909H            | RTOP #1 Test Register 9      |
| 210AH            | 290AH            | 310AH            | 390AH            | RTOP #1 Test Register 10     |
| 210BH            | 290BH            | 310BH            | 390BH            | RTOP #1 Test Register 11     |
| 210CH            | 290CH            | 310CH            | 390CH            | RTOP #1 Test Register 12     |
| 210DH            | 290DH            | 310DH            | 390DH            | RTOP #1 Test Register 13     |
| 210EH            | 290EH            | 310EH            | 390EH            | RTOP #1 Test Register 14     |
| 210FH            | 290FH            | 310FH            | 390FH            | RTOP #1 Test Register 15     |
| 2110H-<br>21FFH  | 2910H-<br>29FFH  | 3110H-<br>31FFH  | 3910H-<br>39FFH  | Reserved                     |
| 2200H –<br>220FH | 2A00H -<br>2A0FH | 3200H -<br>320FH | 3A00H -<br>3A0FH | RTOP #2 Test Register 0 - 15 |
| 2210H-<br>22FFH  | 2A10H-<br>2AFFH  | 3210H-<br>32FFH  | 3A10H-<br>3AFFH  | Reserved                     |
| 2300H –<br>230FH | 2B00H -<br>2B0FH | 3300H -<br>330FH | 3B00H -<br>3B0FH | RTOP #3 Test Register 0 - 15 |
| 2310H-<br>23FFH  | 2B10H-<br>2BFFH  | 3310H-<br>33FFH  | 3B10H-<br>3BFFH  | Reserved                     |
| 2400H            | 2C00H            | 3400H            | 3C00H            | RTTB #1 Test Register 0      |

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| STP #1           | STP #2           | STP #3           | STP #4           | Register                    |
|------------------|------------------|------------------|------------------|-----------------------------|
| 2401H            | 2C01H            | 3401H            | 3C01H            | RTTB #1 Test Register 1     |
| 2402H            | 2C02H            | 3402H            | 3C02H            | RTTB #1 Test Register 2     |
| 2403H            | 2C03H            | 3403H            | 3C03H            | RTTB #1 Test Register 3     |
| 2404H-<br>243FH  | 2C04H-<br>2C3FH  | 3404H-<br>343FH  | 3C04H-<br>3C3FH  | Reserved                    |
| 2440H -<br>2443H | 2C40H -<br>2C43H | 3440H -<br>3443H | 3C40H -<br>3C43H | RTTB #2 Test Register 0 - 3 |
| 2444H-<br>247FH  | 2C44H-<br>2C7FH  | 3444H-<br>347FH  | 3C44H-<br>3C7FH  | Reserved                    |
| 2480H -<br>2483H | 2C80H -<br>2C83H | 3480H -<br>3483H | 3C80H -<br>3C83H | RTTB #3 Test Register 0 - 3 |
| 2484H-<br>27FFH  | 2C84H-<br>2FFFH  | 3484H-<br>37FFH  | 3C84H-<br>3FFFH  | Reserved                    |

**Notes on Test Mode Register Bits:**

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.
2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

### Register 2000H: Master Test

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 | W    | PMCTST   | X       |
| Bit 3 | W    | MOTOTST  | X       |
| Bit 2 | R/W  | IOTST    | 0       |
| Bit 1 | W    | HIZDATA  | X       |
| Bit 0 | R/W  | HIZIO    | 0       |

This register is used to enable TUPP+622 test features. All bits, except PMCTST, are reset to zero by a reset of the TUPP+622.

#### HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the TUPP+622. While the HIZIO bit is a logic 1, all output pins of the TUPP+622 except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

#### IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the TUPP+622 for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

#### MOTOTST:

The MOTOTST bit is used to test the decoding of the RDB\_E and WRB\_RWB control signals when MBEB is logic 0.



**PMCTST:**

The PMCTST bit is used to configure the TUPP+622 for PMC's manufacturing tests. When PMCTST is set to logic 1, the TUPP+622 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "OR'ed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

### Register 2001H: STP Select

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 | W    | STPSEL[1] | X       |
| Bit 6 | W    | STPSEL[0] | X       |
| Bit 5 | W    | SSEL[1]   | X       |
| Bit 4 | W    | SSEL[0]   | X       |
| Bit 3 |      | Unused    | X       |
| Bit 2 |      | Unused    | X       |
| Bit 1 |      | Unused    | X       |
| Bit 0 |      | Unused    | X       |

This register is used to select the STM-1 (STS-3) Tributary Processor (STP) and the VTPP, RTOP, RTTB slice when the PMC's manufacturing test mode for the TUPP+622 is enabled.

#### SSEL[1:0]:

The test mode (TSB) slice selection bits (SSEL[1:0]) control CBI access to the VTPP[3:1], RTOP[3:1] and RTTB[3:1] of a selected STP when PMCTST is set high. When SSEL is set to 'b00, the selection among the TSBs in STP #1 - #4 is directly controlled by the address bus (A[13:0]). When SSEL is set to the three higher values, TSB selection is a combination of the address bus, the STPSEL values and the SSEL values. The STP is selected by the STPSEL values. The selection among the VTPP, RTOP and RTTB TSBs is made by setting the address to the address range of VTPP #1, RTOP #1 and RTTB #1, respectively. The choice of TSB slice #1, #2 and #3 is controlled by writing 'b01, 'b10 and 'b11, respectively, to the SSEL[1:0] bits. The SSEL[1:0] bits are cleared by setting CSB to logic 1.

#### STPSEL[1:0]:

The test mode STP selection bits (STPSEL[1:0]) control CBI access to the STP #1, #2, #3 and #4 when PMCTST is set high and the SSEL[1:0] bits are set to 'b01, 'b10 or 'b11. The choice of STP #1, #2, #3 or #4 is controlled by

writing 'b00, 'b01, 'b10 or 'b11 to the STPSEL[1:0] bits, respectively. The STPSEL[1:0] bits are cleared by setting CSB to logic 1.

### **12.1 I/O Test Mode**

In I/O test mode (IOTST in Master Test Register set high), the TUPP+622 allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

**Test Register 2002H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | OD[7]    | X       |
| Bit 6 | W    | OD[6]    | X       |
| Bit 5 | W    | OD[5]    | X       |
| Bit 4 | W    | OD[4]    | X       |
| Bit 3 | W    | OD[3]    | X       |
| Bit 2 | W    | OD[2]    | X       |
| Bit 1 | W    | OD[1]    | X       |
| Bit 0 | W    | OD[0]    | X       |

**Test Register 2003H: (Write in I/O test mode)**

| Bit   | Type | Function   | Default |
|-------|------|------------|---------|
| Bit 7 | W    | ODP[1]     | X       |
| Bit 6 | W    | OTPL[1]    | X       |
| Bit 5 | W    | OTV5[1]    | X       |
| Bit 4 | W    | AIS[1]     | X       |
| Bit 3 | W    | IDLE[1]    | X       |
| Bit 2 | W    | OC1J1V1[1] | X       |
| Bit 1 | W    | OPL[1]     | X       |
| Bit 0 | W    | INTB       | X       |

**Test Register 2004H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | W    | POH[3]   | X       |
| Bit 4 | W    | POH[2]   | X       |
| Bit 3 | W    | POH[1]   | X       |
| Bit 2 | W    | POHFP[3] | X       |
| Bit 1 | W    | POHFP[2] | X       |
| Bit 0 | W    | POHFP[1] | X       |

**Test Register 2005H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | W    | POHEN[3] | X       |
| Bit 4 | W    | POHEN[2] | X       |
| Bit 3 | W    | POHEN[1] | X       |
| Bit 2 |      | Unused   | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 | W    | POHCK    | X       |

**Test Register 2006H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | COUT[1]  | X       |
| Bit 6 | W    | RAD[1]   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | W    | TPOH[1]  | X       |
| Bit 1 | W    | GSCLK[1] | X       |
| Bit 0 | W    | GSCLK[0] | X       |



**Test Register 2802H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | OD[15]   | X       |
| Bit 6 | W    | OD[14]   | X       |
| Bit 5 | W    | OD[13]   | X       |
| Bit 4 | W    | OD[12]   | X       |
| Bit 3 | W    | OD[11]   | X       |
| Bit 2 | W    | OD[10]   | X       |
| Bit 1 | W    | OD[9]    | X       |
| Bit 0 | W    | OD[8]    | X       |

**Test Register 2803H: (Write in I/O test mode)**

| Bit   | Type | Function   | Default |
|-------|------|------------|---------|
| Bit 7 | W    | ODP[2]     | X       |
| Bit 6 | W    | OTPL[2]    | X       |
| Bit 5 | W    | OTV5[2]    | X       |
| Bit 4 | W    | AIS[2]     | X       |
| Bit 3 | W    | IDLE[2]    | X       |
| Bit 2 | W    | OC1J1V1[2] | X       |
| Bit 1 | W    | OPL[2]     | X       |
| Bit 0 |      | Unused     | X       |

**Test Register 2804H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | W    | POH[6]   | X       |
| Bit 4 | W    | POH[5]   | X       |
| Bit 3 | W    | POH[4]   | X       |
| Bit 2 | W    | POHFP[6] | X       |
| Bit 1 | W    | POHFP[5] | X       |
| Bit 0 | W    | POHFP[4] | X       |

**Test Register 2805H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | W    | POHEN[6] | X       |
| Bit 4 | W    | POHEN[5] | X       |
| Bit 3 | W    | POHEN[4] | X       |
| Bit 2 |      | Unused   | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 |      | Unused   | X       |

**Test Register 2806H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | COUT[2]  | X       |
| Bit 6 | W    | RAD[2]   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | W    | TPOH[2]  | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 |      | Unused   | X       |

**Test Register 3002H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | OD[23]   | X       |
| Bit 6 | W    | OD[22]   | X       |
| Bit 5 | W    | OD[21]   | X       |
| Bit 4 | W    | OD[20]   | X       |
| Bit 3 | W    | OD[19]   | X       |
| Bit 2 | W    | OD[18]   | X       |
| Bit 1 | W    | OD[17]   | X       |
| Bit 0 | W    | OD[16]   | X       |

**Test Register 3003H: (Write in I/O test mode)**

| Bit   | Type | Function   | Default |
|-------|------|------------|---------|
| Bit 7 | W    | ODP[3]     | X       |
| Bit 6 | W    | OTPL[3]    | X       |
| Bit 5 | W    | OTV5[3]    | X       |
| Bit 4 | W    | AIS[3]     | X       |
| Bit 3 | W    | IDLE[3]    | X       |
| Bit 2 | W    | OC1J1V1[3] | X       |
| Bit 1 | W    | OPL[3]     | X       |
| Bit 0 |      | Unused     | X       |

**Test Register 3004H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | W    | POH[9]   | X       |
| Bit 4 | W    | POH[8]   | X       |
| Bit 3 | W    | POH[7]   | X       |
| Bit 2 | W    | POHFP[9] | X       |
| Bit 1 | W    | POHFP[8] | X       |
| Bit 0 | W    | POHFP[7] | X       |



**Test Register 3005H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 |      | Unused   | X       |
| Bit 6 |      | Unused   | X       |
| Bit 5 | W    | POHEN[9] | X       |
| Bit 4 | W    | POHEN[8] | X       |
| Bit 3 | W    | POHEN[7] | X       |
| Bit 2 |      | Unused   | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 |      | Unused   | X       |

**Test Register 3006H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | COUT[3]  | X       |
| Bit 6 | W    | RAD[3]   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 |      | TPOH[3]  | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 |      | Unused   | X       |

**Test Register 3802H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | OD[31]   | X       |
| Bit 6 | W    | OD[30]   | X       |
| Bit 5 | W    | OD[29]   | X       |
| Bit 4 | W    | OD[28]   | X       |
| Bit 3 | W    | OD[27]   | X       |
| Bit 2 | W    | OD[26]   | X       |
| Bit 1 | W    | OD[25]   | X       |
| Bit 0 | W    | OD[24]   | X       |

**Test Register 3803H: (Write in I/O test mode)**

| Bit   | Type | Function   | Default |
|-------|------|------------|---------|
| Bit 7 | W    | ODP[4]     | X       |
| Bit 6 | W    | OTPL[4]    | X       |
| Bit 5 | W    | OTV5[4]    | X       |
| Bit 4 | W    | AIS[4]     | X       |
| Bit 3 | W    | IDLE[4]    | X       |
| Bit 2 | W    | OC1J1V1[4] | X       |
| Bit 1 | W    | OPL[4]     | X       |
| Bit 0 |      | Unused     | X       |

**Test Register 3804H: (Write in I/O test mode)**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 |      | Unused    | X       |
| Bit 6 |      | Unused    | X       |
| Bit 5 | W    | POH[12]   | X       |
| Bit 4 | W    | POH[11]   | X       |
| Bit 3 | W    | POH[10]   | X       |
| Bit 2 | W    | POHFP[12] | X       |
| Bit 1 | W    | POHFP[11] | X       |
| Bit 0 | W    | POHFP[10] | X       |

**Test Register 3805H: (Write in I/O test mode)**

| Bit   | Type | Function  | Default |
|-------|------|-----------|---------|
| Bit 7 |      | Unused    | X       |
| Bit 6 |      | Unused    | X       |
| Bit 5 | W    | POHEN[12] | X       |
| Bit 4 | W    | POHEN[11] | X       |
| Bit 3 | W    | POHEN[10] | X       |
| Bit 2 |      | Unused    | X       |
| Bit 1 |      | Unused    | X       |
| Bit 0 |      | Unused    | X       |

**Test Register 3806H: (Write in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | W    | COUT[4]  | X       |
| Bit 6 | W    | RAD[4]   | X       |
| Bit 5 |      | Unused   | X       |
| Bit 4 |      | Unused   | X       |
| Bit 3 |      | Unused   | X       |
| Bit 2 | W    | TPOH[4]  | X       |
| Bit 1 |      | Unused   | X       |
| Bit 0 |      | Unused   | X       |

**Test Register 2002H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | ID[7]    | X       |
| Bit 6 | R    | ID[6]    | X       |
| Bit 5 | R    | ID[5]    | X       |
| Bit 4 | R    | ID[4]    | X       |
| Bit 3 | R    | ID[3]    | X       |
| Bit 2 | R    | ID[2]    | X       |
| Bit 1 | R    | ID[1]    | X       |
| Bit 0 | R    | ID[0]    | X       |



**Test Register 2003H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | IC1J1[1] | X       |
| Bit 5 | R    | IPL[1]   | X       |
| Bit 4 | R    | ITMF[1]  | X       |
| Bit 3 | R    | IDP[1]   | X       |
| Bit 2 | R    | OTMF[1]  | X       |
| Bit 1 | R    | GSCLK_FP | X       |
| Bit 0 | R    | Reserved | X       |

**Test Register 2004H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | HSCLK    | X       |
| Bit 6 | R    | IHSMODEB | X       |
| Bit 5 | R    | OHSMODEB | X       |
| Bit 4 | R    | ITV5[1]  | X       |
| Bit 3 | R    | ITPL[1]  | X       |
| Bit 2 | R    | IAIS[1]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |

**Test Register 2802H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | ID[15]   | X       |
| Bit 6 | R    | ID[14]   | X       |
| Bit 5 | R    | ID[13]   | X       |
| Bit 4 | R    | ID[12]   | X       |
| Bit 3 | R    | ID[11]   | X       |
| Bit 2 | R    | ID[10]   | X       |
| Bit 1 | R    | ID[9]    | X       |
| Bit 0 | R    | ID[8]    | X       |

**Test Register 2803H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | IC1J1[2] | X       |
| Bit 5 | R    | IPL[2]   | X       |
| Bit 4 | R    | ITMF[2]  | X       |
| Bit 3 | R    | IDP[2]   | X       |
| Bit 2 | R    | OTMF[2]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |

**Test Register 2804H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | Reserved | X       |
| Bit 5 | R    | Reserved | X       |
| Bit 4 | R    | ITV5[2]  | X       |
| Bit 3 | R    | ITPL[2]  | X       |
| Bit 2 | R    | IAIS[2]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |

**Test Register 3002H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | ID[23]   | X       |
| Bit 6 | R    | ID[22]   | X       |
| Bit 5 | R    | ID[21]   | X       |
| Bit 4 | R    | ID[20]   | X       |
| Bit 3 | R    | ID[19]   | X       |
| Bit 2 | R    | ID[18]   | X       |
| Bit 1 | R    | ID[17]   | X       |
| Bit 0 | R    | ID[16]   | X       |

**Test Register 3003H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | IC1J1[3] | X       |
| Bit 5 | R    | IPL[3]   | X       |
| Bit 4 | R    | ITMF[3]  | X       |
| Bit 3 | R    | IDP[3]   | X       |
| Bit 2 | R    | OTMF[3]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |

**Test Register 3004H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | Reserved | X       |
| Bit 5 | R    | Reserved | X       |
| Bit 4 | R    | ITV5[3]  | X       |
| Bit 3 | R    | ITPL[3]  | X       |
| Bit 2 | R    | IAIS[3]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |



**Test Register 3802H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | ID[31]   | X       |
| Bit 6 | R    | ID[30]   | X       |
| Bit 5 | R    | ID[29]   | X       |
| Bit 4 | R    | ID[28]   | X       |
| Bit 3 | R    | ID[27]   | X       |
| Bit 2 | R    | ID[26]   | X       |
| Bit 1 | R    | ID[25]   | X       |
| Bit 0 | R    | ID[24]   | X       |

**Test Register 3803H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | IC1J1[4] | X       |
| Bit 5 | R    | IPL[4]   | X       |
| Bit 4 | R    | ITMF[4]  | X       |
| Bit 3 | R    | IDP[4]   | X       |
| Bit 2 | R    | OTMF[4]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |

**Test Register 3804H: (Read in I/O test mode)**

| Bit   | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R    | Reserved | X       |
| Bit 6 | R    | Reserved | X       |
| Bit 5 | R    | Reserved | X       |
| Bit 4 | R    | ITV5[4]  | X       |
| Bit 3 | R    | ITPL[4]  | X       |
| Bit 2 | R    | IAIS[4]  | X       |
| Bit 1 | R    | Reserved | X       |
| Bit 0 | R    | Reserved | X       |

**12.2 JTAG Test Port**

The TUPP+622 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

**Table 4 - Instruction Register (Length – 3 bits)**

| Instructions | Selected Register | Instruction Codes, IR[2:0] |
|--------------|-------------------|----------------------------|
| EXTEST       | Boundary Scan     | 000                        |
| IDCODE       | Identification    | 001                        |
| SAMPLE       | Boundary Scan     | 010                        |
| BYPASS       | Bypass            | 011                        |
| BYPASS       | Bypass            | 100                        |
| STCTEST      | Boundary Scan     | 101                        |
| BYPASS       | Bypass            | 110                        |
| BYPASS       | Bypass            | 111                        |

**Table 5 -Identification Register**

|                                    |           |
|------------------------------------|-----------|
| Length                             | 32 bits   |
| Version number                     | 1H        |
| Part Number                        | 5363H     |
| Manufacturer's identification code | 0CDH      |
| Device identification              | 153630CDH |

**Table 6 Boundary Scan Register (Length – 218 bits)**

| Order # | Pin # | Pin name   | Pin Type      | ID value |
|---------|-------|------------|---------------|----------|
| 0       |       | HIZ        | Output Enable |          |
| 1       | D3    | OC1J1V1[1] | Output        |          |
| 2       | E4    | OPL[1]     | Output        |          |
| 3       | C1    | OD[0]      | Output        |          |
| 4       | D2    | OD[1]      | Output        |          |
| 5       | E3    | OD[2]      | Output        |          |
| 6       | D1    | OD[3]      | Output        |          |
| 7       | E2    | OD[4]      | Output        |          |
| 8       | F3    | OD[5]      | Output        |          |
| 9       | G4    | OD[6]      | Output        |          |
| 10      | E1    | OD[7]      | Output        |          |
| 11      | F2    | ODP[1]     | Output        |          |
| 12      | G3    | OTV5[1]    | Output        |          |
| 13      | H4    | OTPL[1]    | Output        |          |
| 14      | G1    | AIS[1]     | Output        |          |
| 15      | H3    | IDLE[1]    | Output        |          |
| 16      | H2    | TPOH[1]    | Output        |          |
| 17      | J3    | COUT[1]    | Output        |          |
| 18      | J2    | OTMF[1]    | Input         |          |
| 19      | K4    | HSCLK      | Input         |          |

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| Order # | Pin # | Pin name | Pin Type | ID value |
|---------|-------|----------|----------|----------|
| 20      | J1    | GSCLK_FP | Input    |          |
| 21      | K3    | RAD[1]   | Output   |          |
| 22      | K1    | POHFP[1] | Output   |          |
| 23      | L4    | POH[1]   | Output   |          |
| 24      | L3    | POHEN[1] | Output   |          |
| 25      | L2    | POHCK    | Output   |          |
| 26      | L1    | POHFP[2] | Output   |          |
| 27      | M3    | POH[2]   | Output   |          |
| 28      | M2    | POHEN[2] | Output   |          |
| 29      | N1    | POHFP[3] | Output   |          |
| 30      | N3    | GSCLK[0] | Output   |          |
| 31      | N4    | GSCLK[1] | Output   |          |
| 32      | P1    | SCLK     | Input    |          |
| 33      | P2    | POH[3]   | Output   |          |
| 34      | P3    | POHEN[3] | Output   |          |
| 35      | R1    | IC1J1[1] | Input    |          |
| 36      | P4    | IPL[1]   | Input    |          |
| 37      | R2    | ID[0]    | Input    |          |
| 38      | R3    | ID[1]    | Input    |          |
| 39      | T2    | ID[2]    | Input    |          |
| 40      | U1    | ID[3]    | Input    |          |
| 41      | T3    | ID[4]    | Input    |          |
| 42      | T4    | ID[5]    | Input    |          |
| 43      | U3    | ID[6]    | Input    |          |
| 44      | V2    | ID[7]    | Input    |          |
| 45      | W1    | IDP[1]   | Input    |          |
| 46      | U4    | ITMF[1]  | Input    |          |

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INTERFACES**

| Order # | Pin # | Pin name  | Pin Type | ID value |
|---------|-------|-----------|----------|----------|
| 47      | V3    | ITV5[1]   | Input    |          |
| 48      | W2    | ITPL[1]   | Input    |          |
| 49      | Y1    | IAIS[1]   | Input    |          |
| 50      | W3    | IHSMODEB  | Input    |          |
| 51      | Y2    | OHSMODEB  | Input    |          |
| 52      | AA1   | IC1J1[4]  | Input    |          |
| 53      | W4    | IPL[4]    | Input    |          |
| 54      | Y3    | ID[24]    | Input    |          |
| 55      | AA4   | ID[25]    | Input    |          |
| 56      | Y5    | ID[26]    | Input    |          |
| 57      | AC3   | ID[27]    | Input    |          |
| 58      | AB4   | ID[28]    | Input    |          |
| 59      | AA5   | ID[29]    | Input    |          |
| 60      | AC4   | ID[30]    | Input    |          |
| 61      | AB5   | ID[31]    | Input    |          |
| 62      | AA6   | IDP[4]    | Input    |          |
| 63      | AC5   | ITMF[4]   | Input    |          |
| 64      | AB6   | ITV5[4]   | Input    |          |
| 65      | AA7   | ITPL[4]   | Input    |          |
| 66      | Y8    | IAIS[4]   | Input    |          |
| 67      | AC7   | RAD[4]    | Output   |          |
| 68      | AA8   | POHFP[10] | Output   |          |
| 69      | AB8   | POH[10]   | Output   |          |
| 70      | AA9   | POHEN[10] | Output   |          |
| 71      | AB9   | POHFP[11] | Output   |          |
| 72      | Y10   | POH[11]   | Output   |          |
| 73      | AC9   | POHEN[11] | Output   |          |

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INTERFACES**

| Order # | Pin # | Pin name   | Pin Type | ID value |
|---------|-------|------------|----------|----------|
| 74      | AA10  | POHFP[12]  | Output   |          |
| 75      | AC10  | POH[12]    | Output   |          |
| 76      | Y11   | POHEN[12]  | Output   |          |
| 77      | AA11  | OTMF[4]    | Input    |          |
| 78      | AB11  | OC1J1V1[4] | Output   |          |
| 79      | AC11  | OPL[4]     | Output   |          |
| 80      | AA12  | OD[24]     | Output   |          |
| 81      | AB12  | OD[25]     | Output   |          |
| 82      | AC13  | OD[26]     | Output   |          |
| 83      | AA13  | OD[27]     | Output   |          |
| 84      | Y13   | OD[28]     | Output   |          |
| 85      | AC14  | OD[29]     | Output   |          |
| 86      | AB14  | OD[30]     | Output   |          |
| 87      | AA14  | OD[31]     | Output   |          |
| 88      | AC15  | ODP[4]     | Output   |          |
| 89      | Y14   | OTV5[4]    | Output   |          |
| 90      | AB15  | OTPL[4]    | Output   |          |
| 91      | AA15  | AIS[4]     | Output   |          |
| 92      | AB16  | IDLE[4]    | Output   |          |
| 93      | AC17  | TPOH[4]    | Output   |          |
| 94      | AA16  | COUT[4]    | Output   |          |
| 95      | AA17  | IC1J1[3]   | Input    |          |
| 96      | AB18  | IPL[3]     | Input    |          |
| 97      | AC19  | ID[16]     | Input    |          |
| 98      | Y17   | ID[17]     | Input    |          |
| 99      | AA18  | ID[18]     | Input    |          |
| 100     | AB19  | ID[19]     | Input    |          |

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INTERFACES**

| Order # | Pin # | Pin name  | Pin Type | ID value |
|---------|-------|-----------|----------|----------|
| 101     | AC20  | ID[20]    | Input    |          |
| 102     | AA19  | ID[21]    | Input    |          |
| 103     | AB20  | ID[22]    | Input    |          |
| 104     | AC21  | ID[23]    | Input    |          |
| 105     | Y19   | IDP[3]    | Input    |          |
| 106     | AA20  | ITMF[3]   | Input    |          |
| 107     | Y21   | ITV5[3]   | Input    |          |
| 108     | W20   | ITPL[3]   | Input    |          |
| 109     | AA23  | IAIS[3]   | Input    |          |
| 110     | Y22   | POHEN [9] | Output   |          |
| 111     | W21   | POH[9]    | Output   |          |
| 112     | Y23   | POHFP [9] | Output   |          |
| 113     | W22   | POHEN [8] | Output   |          |
| 114     | V21   | POH[8]    | Output   |          |
| 115     | U20   | POHFP [8] | Output   |          |
| 116     | W23   | POHEN [7] | Output   |          |
| 117     | V22   | POH[7]    | Output   |          |
| 118     | U21   | POHFP [7] | Output   |          |
| 119     | T20   | RAD[3]    | Output   |          |
| 120     | U23   | COUT[3]   | Output   |          |
| 121     | T21   | TPOH[3]   | Output   |          |
| 122     | T22   | IDLE[3]   | Output   |          |
| 123     | R21   | AIS[3]    | Output   |          |
| 124     | R22   | OTPL[3]   | Output   |          |
| 125     | P20   | OTV5[3]   | Output   |          |
| 126     | R23   | ODP[3]    | Output   |          |
| 127     | P21   | OD[23]    | Output   |          |



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| Order # | Pin # | Pin name    | Pin Type | ID value |
|---------|-------|-------------|----------|----------|
| 128     | P22   | OD[22]      | Output   |          |
| 129     | P23   | OD[21]      | Output   |          |
| 130     | N20   | OD[20]      | Output   |          |
| 131     | N21   | OD[19]      | Output   |          |
| 132     | N23   | OD[18]      | Output   |          |
| 133     | M21   | OD[17]      | Output   |          |
| 134     | M22   | OD[16]      | Output   |          |
| 135     | L23   | OPL[3]      | Output   |          |
| 136     | L22   | OC1J1V1 [3] | Output   |          |
| 137     | L21   | OTMF[3]     | Input    |          |
| 138     | L20   | COUT[2]     | Output   |          |
| 139     | K23   | TPOH[2]     | Output   |          |
| 140     | K22   | IDLE[2]     | Output   |          |
| 141     | K21   | AIS[2]      | Output   |          |
| 142     | J23   | OTPL[2]     | Output   |          |
| 143     | K20   | OTV5[2]     | Output   |          |
| 144     | J21   | ODP[2]      | Output   |          |
| 145     | H22   | OD[15]      | Output   |          |
| 146     | G23   | OD[14]      | Output   |          |
| 147     | H21   | OD[13]      | Output   |          |
| 148     | G22   | OD[12]      | Output   |          |
| 149     | H20   | OD[11]      | Output   |          |
| 150     | G21   | OD[10]      | Output   |          |
| 151     | F22   | OD[9]       | Output   |          |
| 152     | E23   | OD[8]       | Output   |          |
| 153     | G20   | OPL[2]      | Output   |          |
| 154     | F21   | OC1J1V1 [2] | Output   |          |

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INTERFACES**

| Order # | Pin # | Pin name  | Pin Type | ID value |
|---------|-------|-----------|----------|----------|
| 155     | D23   | OTMF[2]   | Input    |          |
| 156     | E21   | POHEN [6] | Output   |          |
| 157     | D22   | POH[6]    | Output   |          |
| 158     | C23   | POHFP [6] | Output   |          |
| 159     | E20   | POHEN [5] | Output   |          |
| 160     | D21   | POH[5]    | Output   |          |
| 161     | C20   | POHFP [5] | Output   |          |
| 162     | D19   | POHEN [4] | Output   |          |
| 163     | A21   | POH[4]    | Output   |          |
| 164     | B20   | POHFP [4] | Output   |          |
| 165     | C19   | RAD[2]    | Output   |          |
| 166     | A20   | IAIS[2]   | Input    |          |
| 167     | B19   | ITPL[2]   | Input    |          |
| 168     | C18   | ITV5[2]   | Input    |          |
| 169     | C14   | INTB      | Output   |          |
| 170     |       | OENB[7]   | OE       |          |
| 171     | A14   | D[7]      | I/O      |          |
| 172     |       | OENB[6]   | OE       |          |
| 173     | D13   | D[6]      | I/O      |          |
| 174     |       | OENB[5]   | OE       |          |
| 175     | C13   | D[5]      | I/O      |          |
| 176     |       | OENB[4]   | OE       |          |
| 177     | B13   | D[4]      | I/O      |          |
| 178     |       | OENB[3]   | OE       |          |
| 179     | A13   | D[3]      | I/O      |          |
| 180     |       | OENB[2]   | OE       |          |
| 181     | C12   | D[2]      | I/O      |          |

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INTERFACES**

| Order # | Pin # | Pin name | Pin Type | ID value |
|---------|-------|----------|----------|----------|
| 182     |       | OENB[1]  | OE       |          |
| 183     | B12   | D[1]     | I/O      |          |
| 184     |       | OENB[0]  | OE       |          |
| 185     | A11   | D[0]     | I/O      |          |
| 186     | D17   | ITMF[2]  | Input    | 1        |
| 187     | A19   | IDP[2]   | Input    | 0        |
| 188     | B18   | ID[15]   | Input    | 1        |
| 189     | C17   | ID[14]   | Input    | 1        |
| 190     | D16   | ID[13]   | Input    | 0        |
| 191     | A17   | ID[12]   | Input    | 0        |
| 192     | C16   | ID[11]   | Input    | 1        |
| 193     | B16   | ID[10]   | Input    | 1        |
| 194     | C15   | ID[9]    | Input    | 0        |
| 195     | B15   | ID[8]    | Input    | 0        |
| 196     | D14   | IPL[2]   | Input    | 0        |
| 197     | A15   | IC1J1[2] | Input    | 0        |
| 198     | C11   | A[13]    | Input    | 1        |
| 199     | D11   | A[12]    | Input    | 1        |
| 200     | A10   | A[11]    | Input    | 0        |
| 201     | B10   | A[10]    | Input    | 0        |
| 202     | C10   | A[9]     | Input    | 0        |
| 203     | A9    | A[8]     | Input    | 1        |
| 204     | D10   | A[7]     | Input    | 1        |
| 205     | B9    | A[6]     | Input    | 0        |
| 206     | C9    | A[5]     | Input    | 1        |
| 207     | B8    | A[4]     | Input    | 1        |
| 208     | A7    | A[3]     | Input    | 0        |

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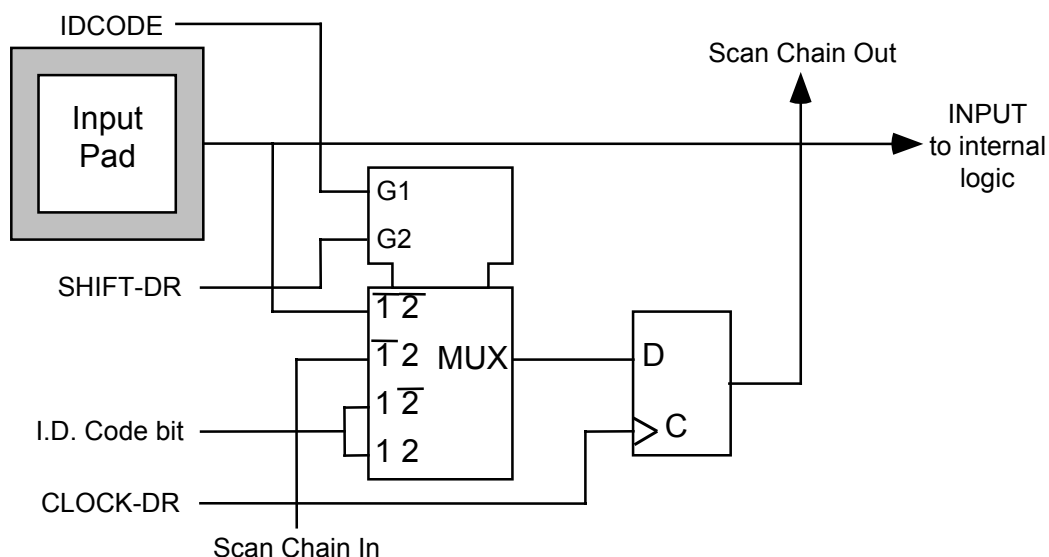
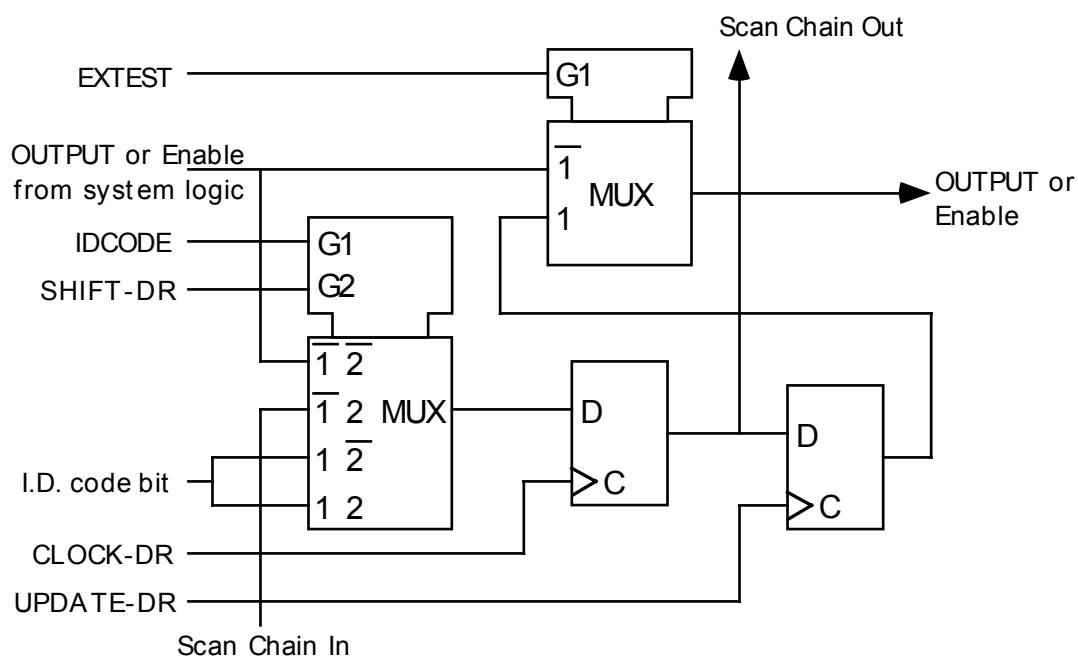
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| Order # | Pin # | Pin name | Pin Type   | ID value |
|---------|-------|----------|------------|----------|
| 209     | C8    | A[2]     | Input      | 0        |
| 210     | B7    | A[1]     | Input      | 1        |
| 211     | D8    | A[0]     | Input      | 0        |
| 212     | C7    | WRB      | Input      | 1        |
| 213     | B6    | RDB      | Input      | 0        |
| 214     | A5    | ALE      | Input      | 1        |
| 215     | D7    | RSTB     | Input      | 0        |
| 216     | C6    | MBEB     | Input      | 0        |
| 217     | A4    | CSB      | Input      | 0        |
|         | C5    | TCK      | TAP Clock  |          |
|         | B4    | TDI      | TAP Input  |          |
|         | A3    | TDO      | TAP Output |          |
|         | D5    | TRSTB    | TAP Input  |          |
|         | C4    | TMS      | TAP Input  |          |

**Notes :**

1. CSB is the first bit of the scan chain (closest to TDI).
2. OENB[n] sets the corresponding D[n] pin to an output when set low.

In the diagram of boundary scan cells, CLOCK-DR is connected to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

**Figure 7 - Input Observation Cell (Input, Clock Input)**

**Figure 8 - Output Cell (Output, Clock Output, Output Enable)**


The diagram illustrates the internal logic of an I/O cell and its connection to an OUT\_CELL. It features two main blocks: an IO\_CELL and an OUT\_CELL. The IO\_CELL has three inputs: 'Scan Chain In' at the bottom, 'INPUT to internal logic' on the left, and 'OUTPUT from internal logic' on the left. It has two outputs: 'Scan Chain Out' at the top and a signal to the OUT\_CELL on the right. The OUT\_CELL has one input: 'OUTPUT ENABLE from internal logic (0 = drive)' on the left. It has one output: 'Scan Chain Out' at the top. A feedback loop is shown where the output of the OUT\_CELL is inverted and fed back into the IO\_CELL. An I/O PAD is connected to the output of the IO\_CELL.

## **13 OPERATION**

### **13.1 Configuration Options**

The TUPP+622 consists of four independent STM-1 (STS-3) tributary processors (STP), each having the equivalent functionality of a TUPP-PLUS (PM5362) device. STP #1, #2, #3 and #4 process the STM-1 #1, #2, #3 and #4 streams, respectively. Each STP consists of three sets of tributary payload processor (VTPP), tributary path overhead processor (RTOP) and tributary trace buffer (RTTB). Each VTPP, RTOP and RTTB set deals with the portion of the SONET frame that corresponds to an STS-1 SPE. Equivalently, each VTPP, RTOP and RTTB set deals with the portion of the SDH frame that corresponds to a VC3 together with the 2 columns of fixed stuff that are added when mapping a VC3 into an AU3. By coordinating the operation of the three VTPPs, RTOPs and RTTBs in an STP, they can process the portion of an SDH frame that corresponds to a VC4. The coordination that may be required between the three VTPPs relates to the J1 byte marker and the encoding of the tributary multiframe into the H4 byte. When processing a VC4 that carries three TUG3s, the alignment provided by the J1 byte marker and the H4 byte of the VC4 must be distributed to all VTPPs, RTOPs and RTTBs in an STP. When processing STS-1 SPEs, or equivalently, VC3s carried within AU3s, each VTPP, RTOP and RTTB set receives its own J1 byte marker and H4 byte. Coordination is accomplished as follows: The tributary multiframe alignment that is detected by VTPP #1 is distributed to the two other VTPPs which do not receive valid H4 bytes. In addition, the input demultiplexer will stretch the pulse captured on the IC1J1 input for the corresponding STM-1 stream that marks the VC4 J1 byte so that it marks the next two bytes. During the demultiplexing process this effectively feeds a "J1" marker to the two "slaved" VTPPs.

The modes of operation of the TUPP+622 are summarized as follows:

**STS-1 Mode:** This is default. Each STS-1 in an STM-1 stream is assumed to carry seven VT groups, each of which can be independently configured to carry VT1.5s, VT2s, VT3s, or VT6s. The associated IC1J1 input is expected to mark the J1 byte of each STS-1 SPE and each VTPP detects the tributary multiframe encoded in the unique H4 byte that it receives.

**AU3 Mode:** This is also the default, as it corresponds exactly to STS-1 mode, except for nomenclature. Each AU3 in an STM-1 stream is assumed to carry

seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of a VT3 is allowed but there is no SDH nomenclature to describe this.) The associated IC1J1 input is expected to mark the J1 byte of each VC3 and each VTPP detects the tributary multiframe encoded in the unique H4 byte that it receives.

**AU4 Mode:** This mode is enabled when the ICONCAT and OCONCAT bits of an STP are set high. In AU4 mode, individual VTPPs in an STP must be configured in either TUG3 mode or TU3 mode. The associated IC1J1 input is expected to mark the J1 byte of the VC4. This J1 marker is stretched to provide a "J1" marker to each VTPP. VTPP #2 and VTPP#3 are slaved to the tributary multiframe indication provided by VTPP #1 as it is the only one that receives a valid H4 byte.

**TUG3 Mode:** This mode is enabled when the TUG3 bit is set high in a VTPP. In addition, the ICONCAT and OCONCAT bits of the STP must be set high. The TUG3 processed by the VTPP is assumed to carry seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of a VT3 is allowed but there is no SDH nomenclature to describe this.) When an STP in the TUPP+622 is in AU4 mode, each VTPP can be independently configured in TUG3 or TU3 mode.

**TU3 Mode:** This mode is enabled when the TU3 bit is set high in a VTPP. In addition the ICONCAT and OCONCAT bits of the STP must be set high. The TUG3 processed by the VTPP is assumed to carry a TU3. When an STP in the TUPP+622 is in AU4 mode, each VTPP can be independently configured in TUG3 or TU3 mode.

For figures in the operation and functional timing sections, transport overhead and path overhead bytes are shown for notational convenience only. In the incoming direction, except for the H4 byte, ID[7:0] (ID[15:8], ID[23:16], ID[31:24]) does not need to contain valid transport and STS/AU path overhead byte values. The H4 byte must be valid only if H4 framing is enabled (ITMFEN=0). Otherwise, it too may be invalid. However, the incoming parity must match the data supplied at all times. In the outgoing direction, TUPP+622 places valid framing, STS/AU pointer bytes and all-zeros data on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]) for transport overhead bytes. It generates all zero bytes for the STS/AU path overhead except for the H4 byte which contains leading ones and an incrementing two bit pattern. The fixed stuff bytes in the tributary mapping to the synchronous payload envelope (virtual container) are also generated as all zero

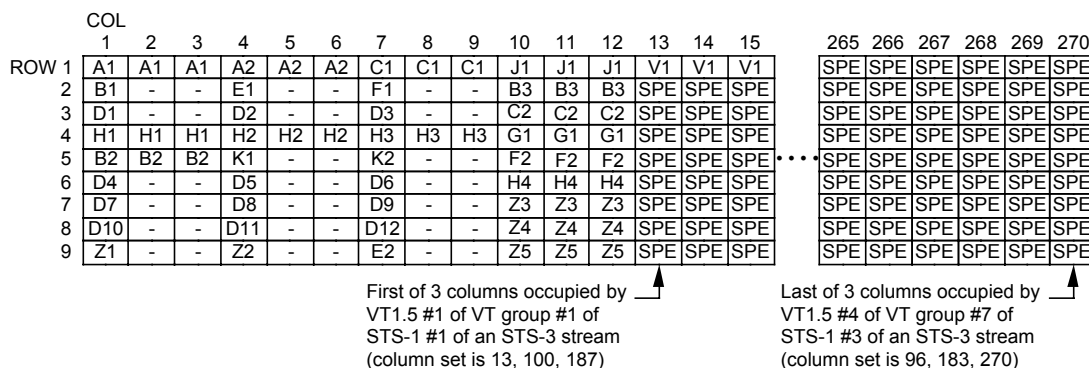


bytes. The outgoing parity reflects the data on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]) at all times.

## 13.2 STS-1 Mode

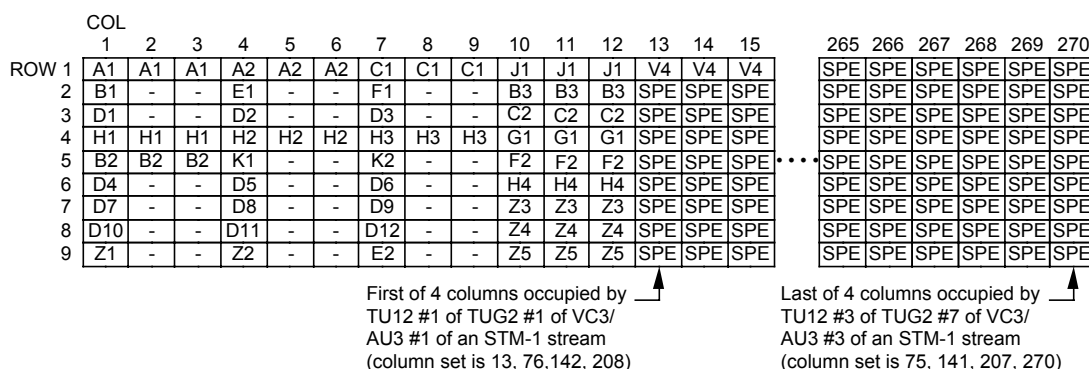
An example of the placement of tributaries assumed in STS-1 mode is illustrated in Figure 11. For simplicity, this figure shows the frame on the OD[7:0] bus when the STM-1 (STS-3) interface mode is enabled. In this case the outgoing STS-1 SPEs are locked to an active offset of 522 with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the first frame of the tributary multiframe when the V1 bytes are present. This example illustrates a VT structured STS-1 SPE where all VT groups are configured to carry VT1.5s.

**Figure 11 - SONET STS-3 Carrying VT1.5 Within STS-1**



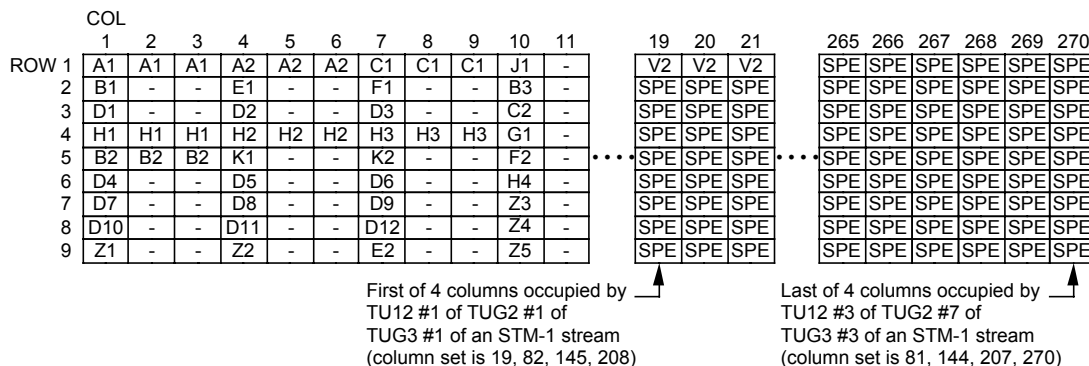
## 13.3 AU3 Mode

An example of the placement of tributaries assumed in AU3 mode is illustrated in Figure 12. For simplicity, this figure shows the frame on the OD[7:0] bus when the STM-1 (STS-3) interface mode is enabled. In this case the outgoing VC3s are locked to an active offset of 522 with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the last frame of the tributary multiframe when the V4 bytes are present. This example illustrates the case where the VC3s carry TUG2s and all TUG2s are configured to carry TU12s.

**Figure 12 - SDH STM-1 Carrying TU12 Within VC3/AU3**


### 13.4 AU4 Mode

An example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 13. For simplicity, this figure shows the frame on the OD[7:0] bus when the STM-1 (STS-3) interface mode is enabled. In this case the outgoing VC4 is locked to an active offset of 522 with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the second frame of the tributary multiframe when the V2 bytes are present. This example illustrates a case where the VC4 carries TUG3s, all TUG3s carry TUG2s, and all TUG2s are configured to carry TU12s.

**Figure 13 - SDH STM-1 Carrying TU12 Within TUG3/AU4**


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Another example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 14. For simplicity, this figure shows the frame on the OD[7:0] bus when the STM-1 (STS-3) interface mode is enabled. In this case the outgoing VC4 is locked to an active offset of 522 with respect to the outgoing transport envelope frame. This example illustrates the case where the VC4 carries TUG3s that are all configured to carry TU3s.

**Figure 14 - SDH STM-1 Carrying TU3 Within TUG3**

| ROW | COL |    |    |     |    |    |     |    |    |    |    |    |    |    |    |     |     |     |     |     |     |
|-----|-----|----|----|-----|----|----|-----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|
|     | 1   | 2  | 3  | 4   | 5  | 6  | 7   | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16  | 17  | 18  | 268 | 269 | 270 |
| 1   | A1  | A1 | A1 | A2  | A2 | A2 | C1  | C1 | C1 | J1 | -  | -  | H1 | H1 | H1 | POH | POH | POH | SPE | SPE | SPE |
| 2   | B1  | -  | -  | E1  | -  | -  | F1  | -  | -  | B3 | -  | -  | H2 | H2 | H2 | POH | POH | POH | SPE | SPE | SPE |
| 3   | D1  | -  | -  | D2  | -  | -  | D3  | -  | -  | C2 | -  | -  | H3 | H3 | H3 | POH | POH | POH | SPE | SPE | SPE |
| 4   | H1  | H1 | H1 | H2  | H2 | H2 | H3  | H3 | H3 | G1 | -  | -  | -  | -  | -  | POH | POH | POH | SPE | SPE | SPE |
| 5   | B2  | B2 | B2 | K1  | -  | -  | K2  | -  | -  | F2 | -  | -  | -  | -  | -  | POH | POH | POH | SPE | SPE | SPE |
| 6   | D4  | -  | -  | D5  | -  | -  | D6  | -  | -  | H4 | -  | -  | -  | -  | -  | POH | POH | POH | SPE | SPE | SPE |
| 7   | D7  | -  | -  | D8  | -  | -  | D9  | -  | -  | Z3 | -  | -  | -  | -  | -  | POH | POH | POH | SPE | SPE | SPE |
| 8   | D10 | -  | -  | D11 | -  | -  | D12 | -  | -  | Z4 | -  | -  | -  | -  | -  | POH | POH | POH | SPE | SPE | SPE |
| 9   | Z1  | -  | -  | Z2  | -  | -  | E2  | -  | -  | Z5 | -  | -  | -  | -  | -  | POH | POH | POH | SPE | SPE | SPE |

First of 86 columns occupied by TU3 carried in TUG3 #1 of an STM-1 stream

Last of 86 columns occupied by TU3 carried in TUG3 #3 of an STM-1 stream

Yet another example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 15. For simplicity, this figure shows the frame on the OD[7:0] bus when the STM-1 (STS-3) interface mode is enabled. In this case the outgoing VC4 is locked to an active offset of 522 with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the last frame of the tributary multiframe when the V4 bytes are present. This example illustrates a complex case where the VC4 carries TUG3s and where TUG3 #1 carries a TU3, TUG3 #2 carries TUG2s that are all configured to carry TU11s, and TUG3 #3 carries TUG2s that are all configured to carry TU12s.

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**Figure 15 - SDH STM-1 Carrying Mix Of TU11, TU12, TU3 Within TUG3/AU4**

| ROW | COL |    |    |     |    |    |     |    |    |    |    |    |    |    |    |     |    |    |     |     |     | 268 | 269 | 270 |
|-----|-----|----|----|-----|----|----|-----|----|----|----|----|----|----|----|----|-----|----|----|-----|-----|-----|-----|-----|-----|
|     | 1   | 2  | 3  | 4   | 5  | 6  | 7   | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16  | 17 | 18 | 19  | 20  | 21  |     |     |     |
| 1   | A1  | A1 | A1 | A2  | A2 | A2 | C1  | C1 | C1 | J1 | -  | -  | H1 | H1 | H1 | POH | -  | -  | SPE | V4  | V4  | SPE | SPE | SPE |
| 2   | B1  | -  | -  | E1  | -  | -  | F1  | -  | -  | B3 | -  | -  | H2 | H2 | H2 | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 3   | D1  | -  | -  | D2  | -  | -  | D3  | -  | -  | C2 | -  | -  | H3 | H3 | H3 | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 4   | H1  | H1 | H1 | H2  | H2 | H2 | H3  | H3 | H3 | G1 | -  | -  | -  | -  | -  | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 5   | B2  | B2 | B2 | K1  | -  | -  | K2  | -  | -  | F2 | -  | -  | -  | -  | -  | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 6   | D4  | -  | -  | D5  | -  | -  | D6  | -  | -  | H4 | -  | -  | -  | -  | -  | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 7   | D7  | -  | -  | D8  | -  | -  | D9  | -  | -  | Z3 | -  | -  | -  | -  | -  | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 8   | D10 | -  | -  | D11 | -  | -  | D12 | -  | -  | Z4 | -  | -  | -  | -  | -  | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |
| 9   | Z1  | -  | -  | Z2  | -  | -  | E2  | -  | -  | Z5 | -  | -  | -  | -  | -  | POH | -  | -  | SPE | SPE | SPE | SPE | SPE | SPE |

First of 86 columns occupied by TU3 carried in TUG3 #1 of an STM-1 stream  
 First of 3 columns occupied by TU11 #1 of TUG2 #1 of TUG3 #2 of an STM-1 stream (column set is 20, 104, 188)  
 Last of 4 columns occupied by TU12 #3 of TUG2 #7 of TUG3 #3 of an STM-1 stream (column set is 81, 144, 207, 270)

In Figure 15 above, the H1 to H3 byte in column 13 form the TU3 offset pointer. The H1 to H3 bytes in columns 14 and 15 are null pointer indications (NPI) for TUG3 #2 and #3.

### 13.5 Bypass Options

The three tributary payload processors (VTPP) in each of the four STM-1 (STS-3) tributary processors (STP) in the TUPP+622 may be individually disabled or bypassed using the corresponding TUGEN or TUGBYP register bits, respectively. This enables the TUPP+622 to support STS-1/AU3/TUG3 level bypass operation. Incoming data destined to a disabled or bypassed processor is re-transmitted unchanged to the outgoing data after some delay. The amount of delay is fixed when the 19.44 MHz STM-1 interface mode for both the incoming and outgoing interfaces are selected. When either or both incoming and outgoing interfaces are set to the 77.76 MHz STM-4 interface mode, the amount of delay is also dependent on the relative phase of the corresponding incoming frame pulse (IC1J1) and the GSCLK frame pulse (GSCLK\_FP). Figure 26 and Figure 27 show the functional timing of possible bypass delays for the STM-1 (STS-3) and the STM-4 (STS-12) interface modes, respectively.

For STM-1 (AU4) bypass operation, all three tributary payload processors (VTPP) of the corresponding STM-1 (STS-3) tributary processor (STP) must be bypassed by setting the TUGEN and TUGBYP bits high. Tributary performance monitoring of the STM-1 (AU4) stream remains active in this bypass configuration.

For STM-4-4c bypass, all three tributary payload processors (VTPP) in each of the four STM-1 (STS-3) tributary processors (STP) must be disabled by setting the TUGEN bits low. Tributary performance monitoring of the STM-4-4c stream is not required and is disabled in this bypass configuration.

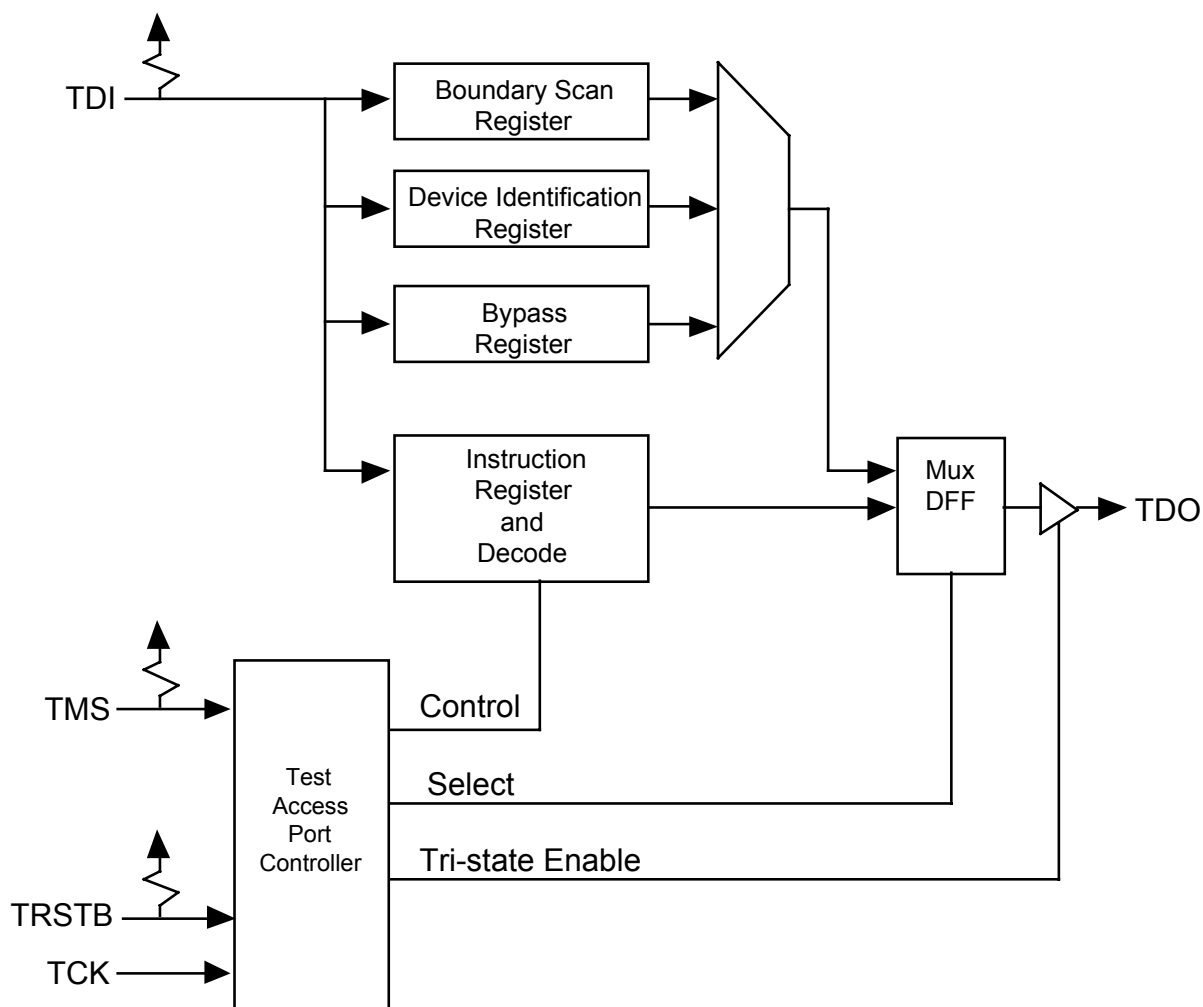
### **13.6 Power Sequencing**

Due to ESD protection structures in the pads, it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, it is possible to damage these ESD protection devices or trigger latch-up. The recommended power supply sequencing is as follows:

1. To prevent damage to the ESD protection on the device inputs, the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDD/VDDI power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification (20 mA).
2. Power supply to the core (VDDI) must be applied after VDD have been applied or they must be current limited to the maximum latch-up current specification (100 mA).
3. Power down the device in the reverse sequence. Use the above current limiting technique for the VDDI power supply. Small offsets in VDD and VDDI discharge times will not damage the device.

### **13.7 JTAG Support**

The TUPP+622 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO, used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

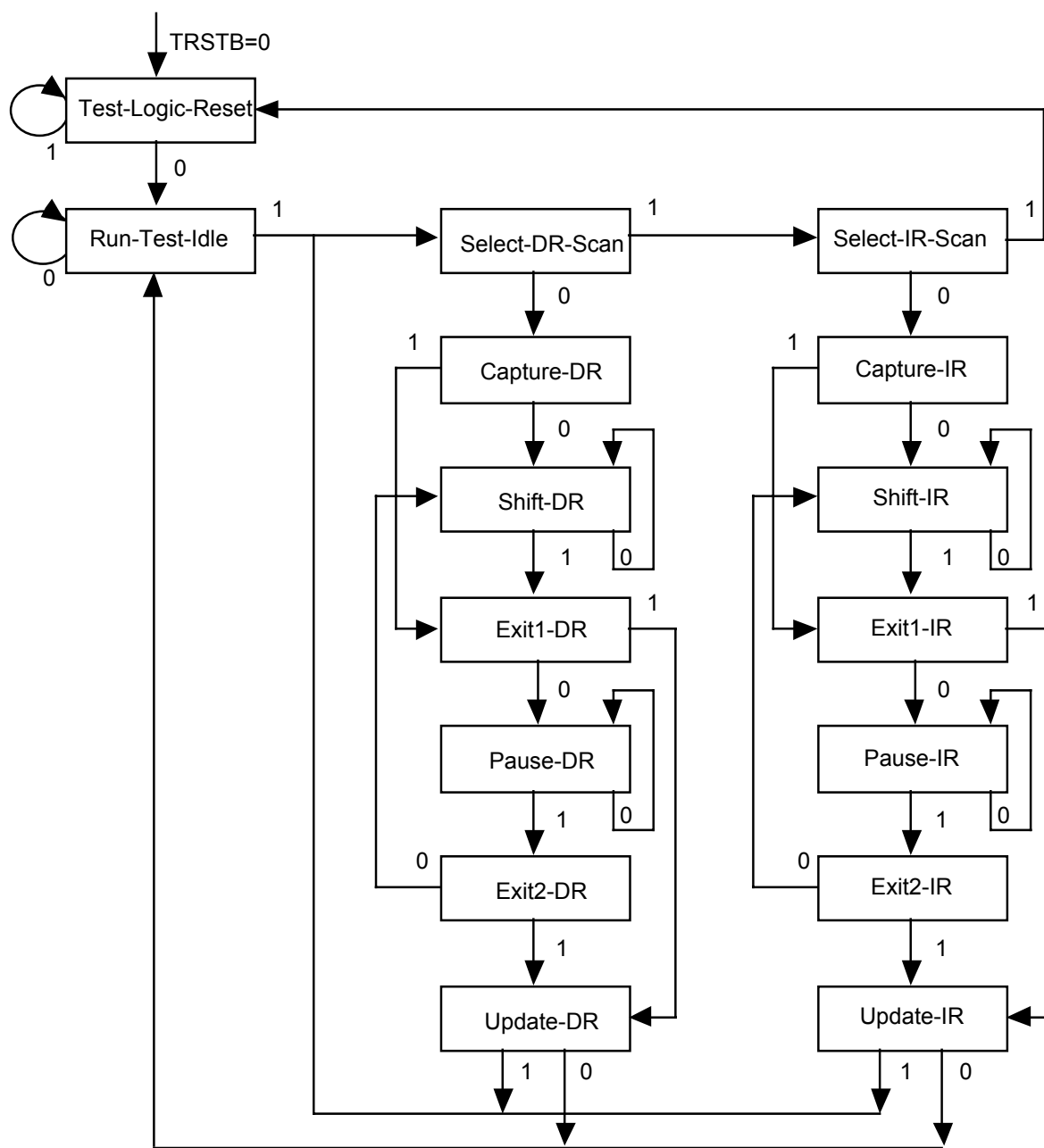
**Figure 16 - Boundary Scan Architecture**


The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

### 13.7.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

**Figure 17 - TAP Controller Finite State Machine**

All transitions dependent on input TMS



**Test-Logic-Reset:**

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

**Run-Test-Idle:**

The run test/idle state is used to execute tests.

**Capture-DR:**

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

**Shift-DR:**

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

**Update-DR:**

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

**Capture-IR:**

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

**Shift-IR:**

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

**Update-IR:**

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

The TDO output is enabled during states Shift-DR and Shift-IR. Otherwise, it is tri-stated.

**13.7.2 Boundary Scan Instructions**

The following is a description of the standard instructions. Each instruction selects an serial test data register path between input, TDI, and output, TDO.

**BYPASS**

The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

**EXTEST**

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input TDI and output TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

## SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

## IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

## STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out on output TDO using the Shift-DR state.

## **14 FUNCTIONAL TIMING**

The timing of the TUPP+622 STM-1 input signals is illustrated in Figure 18 where  $n$  is {1, 2, 3, 4}. This diagram shows a simple STS-3 case that outlines the function of the various input signals associated with each of the four input buses when the TUPP+622 is in STM-1 (STS-3) input interface mode (IHSMODEB set high). Data on ID[7:0] (ID[15:8], ID[23:16], ID[31:24]) is sampled on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the IPL[1] (IPL[2], IPL[3], IPL[4]) signal being set high. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal pulses high while IPL[1] (IPL[2], IPL[3], IPL[4]) is low to mark the position of the first C1 byte in the STS-3 transport envelope. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal is set high for three SCLK periods while IPL[1] (IPL[2], IPL[3], IPL[4]) is also set high to mark the J1 bytes of each STS-1 SPE. The ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) signal is selectable to mark the third byte after J1 of the first tributary in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) is shown to be marking the last H4 byte of the tributary multiframe in STS-1 #1 and STS-1 #3. The H4 byte in STS-1 #2, as shown, is not last in the tributary multiframe. In this simple example, all STS-1 SPEs are aligned to the STS-3 transport envelope such that the J1 bytes directly follow the C1 bytes and no STS-1 pointer justification events are occurring. Other alignments are possible. The four input buses can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the input buses may be different. However, the transport frame alignments of the four input buses must be identical. That is, the C1 portion of all the IC1J1[4:1] signals must be coincident. This diagram also applies to the AU3 mode as it is equivalent to the STS-1 mode, except for nomenclature.

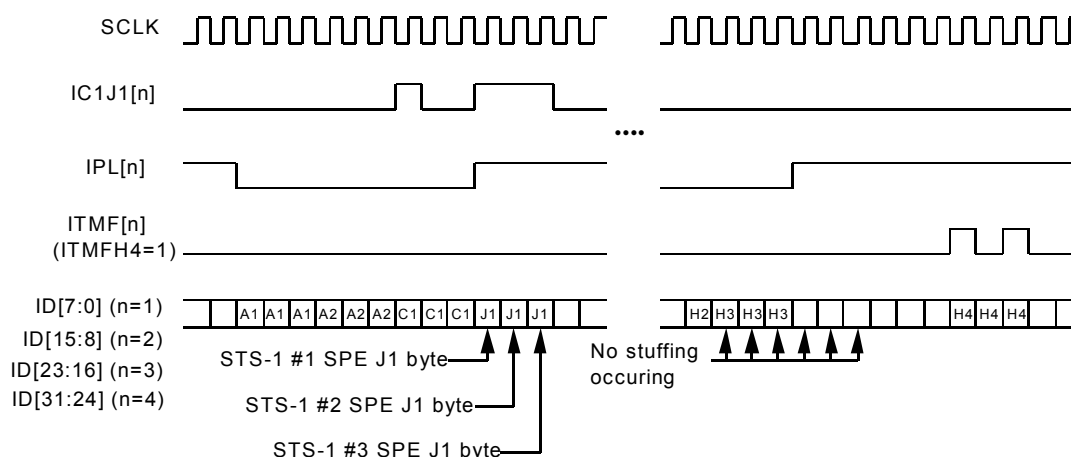
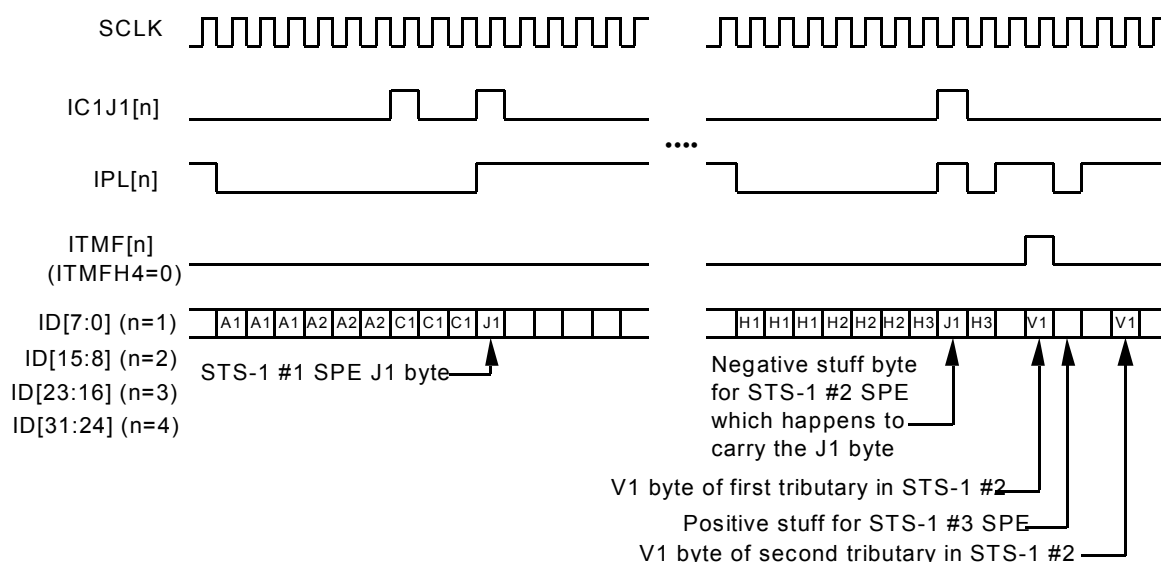
**Figure 18 - STM-1 Input Bus Timing - Simple STS-1/AU3 Case**


Figure 19 shows a more complex STS-3 case that illustrates the flexibility provided by the various input signals associated with each of the four input buses when the TUPP+622 is in STM-1 (STS-3) input interface mode (IHSMODEB set high) ( $n$  is {1, 2, 3, 4}). Data on ID[7:0] (ID[15:8], ID[23:16], ID[31:24]) is sampled on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the IPL[1] (IPL[2], IPL[3], IPL[4]) signal being set high. This example shows a negative stuff event occurring on STS-1 #2 and a positive stuff event occurring on STS-1 #3. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal pulses high while IPL[1] (IPL[2], IPL[3], IPL[4]) is low to mark the position of the C1 byte of STS-1 #1. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal pulses high again to mark the J1 byte of each of the three STS-1 SPEs. The ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) signal is selectable to mark the third byte after J1 in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) is shown to be marking the V1 byte of the first tributary multiframe in STS-1 #2. The three STS-1 SPEs are shown to have different alignments to the STS-3 transport envelope and the alignment is changing for two of the STS-1 SPEs (STS-1 #1 and #2) due to the pointer justification events shown. Other alignments are possible. The four input buses can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the input buses may be different. However, the transport frame alignments of the four input buses must be identical. That is, the C1 portion of all the IC1J1[4:1] signals must be coincident.

This diagram also applies to the AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

**Figure 19 - STM-1 Input Bus Timing - Complex STS-1 / AU3 Case**



The timing of the TUPP+622 input buses when it is in STM-1 (STS-3) input interface mode (IHSMODEB set high) is illustrated in Figure 20 where n is {1, 2, 3, 4}. This diagram shows the relationships of the input signals in STS-1 mode associated with each of the four input buses. Data on ID[7:0] (ID[15:8], ID[23:16], ID[31:24]) is sampled on the rising edge of SCLK. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal pulses high when IPL[1] is set low to mark the position of the C1 byte of the first STS-1 stream in every frame of the STS-3 transport envelope. IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) pulses high when IPL[1] (IPL[2], IPL[3], IPL[4]) is set high to mark the J1 byte in each STS-1 stream. IPL[1] (IPL[2], IPL[3], IPL[4]) identifies the SPE bytes on ID[7:0] (ID[15:8], ID[23:16], ID[31:24]). The ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) input marks the frame containing V1 bytes. It is sampled only at the first V1 byte position of the first STS-1 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the ITPL[1] (ITPL[2], ITPL[3], ITPL[4]) signal being set high when the VT/TU pointer interpretation is disabled. The ITV5[1] (ITV5[2], ITV5[3], ITV5[4]) signal pulses high to mark the V5 bytes of each incoming tributary when the VT/TU pointer interpretation is disabled. In this example, all STS-1 SPEs are aligned to the STS-3 transport envelope such that the J1 bytes

directly follow the C1 bytes. Other alignments are possible. The four input buses can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the input buses may be different. However, the transport frame alignments of the four input buses must be identical. That is, the C1 portion of all the IC1J1[4:1] signals must be coincident. This diagram also applies to the AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

**Figure 20 - STM-1 Input Bus Timing - STS-1 / AU3 (VT/TU Pointer Interpretation Disabled)**

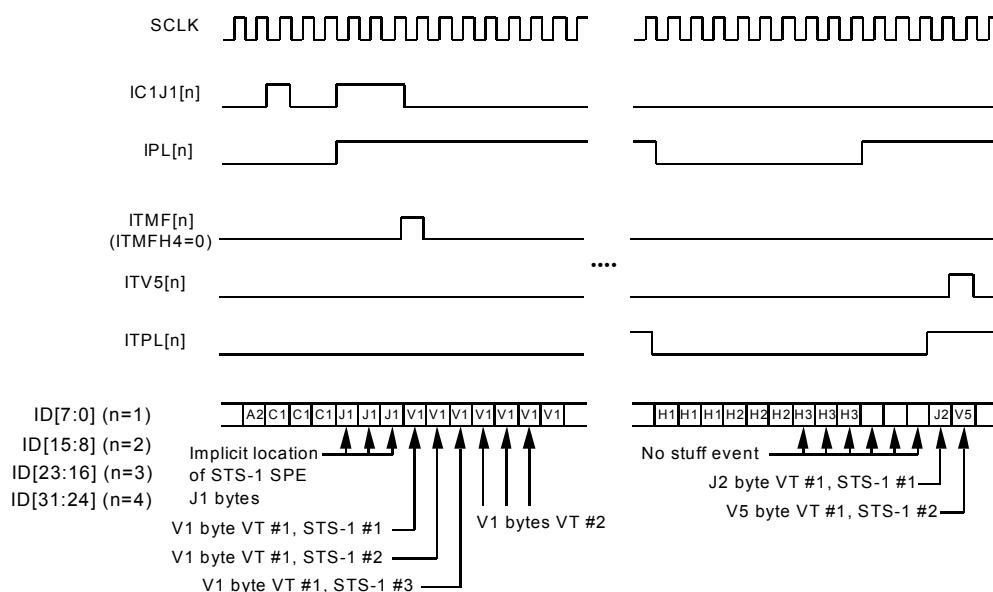


Figure 21 shows timing relationships of the various input signals in the AU4 mode associated with each of the four input buses when the TUPP+622 is in STM-1 (STS-3) input interface mode (IHSMODEB set high) (n is {1, 2, 3, 4}). Data on ID[7:0] (ID[15:8], ID[23:16], ID[31:24]) is sampled on the rising edge of SCLK. The bytes forming the AU4 virtual container are identified by the IPL[1] (IPL[2], IPL[3], IPL[4]) signal being set high. This example shows a negative stuff occurring for the VC4. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal pulses high while IPL[1] (IPL[2], IPL[3], IPL[4]) is set low to mark the position of the single C1 byte in the STM-1 transport envelope. The ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) signal is selectable to mark the third byte after J1, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF[1] (ITMF[2], ITMF[3], ITMF[4]) is shown to be marking the final H4 byte of the tributary

multiframe. The IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) signal pulses high to mark the single J1 byte of the VC4. This diagram applies to input buses in AU4 mode, regardless of whether individual tributary payload processors are configured for TUG3 or TU3 mode. The four input buses can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the input buses may be different. However, the transport frame alignments of the four input buses must be identical. That is, the C1 portion of all the IC1J1[4:1] signals must be coincident.

**Figure 21 - STM-1 Input Bus Timing - AU4 Case**

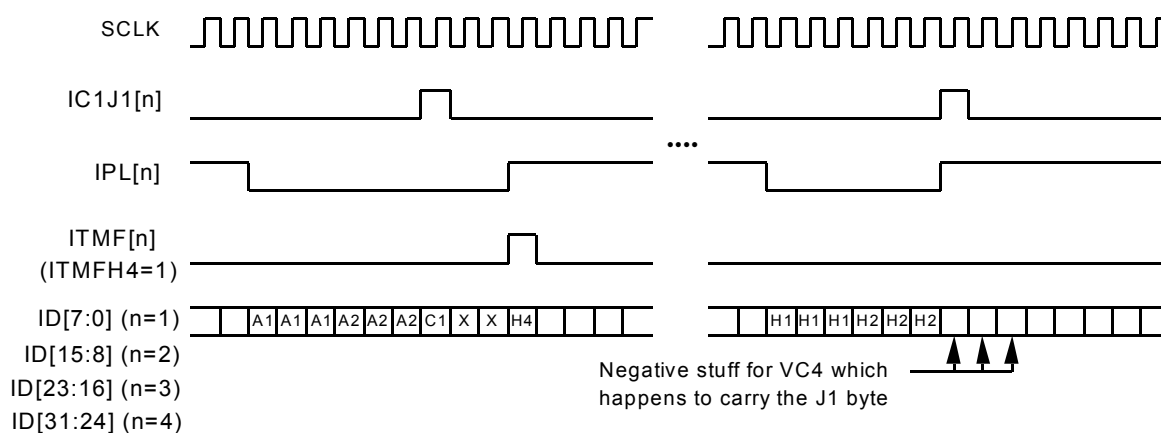
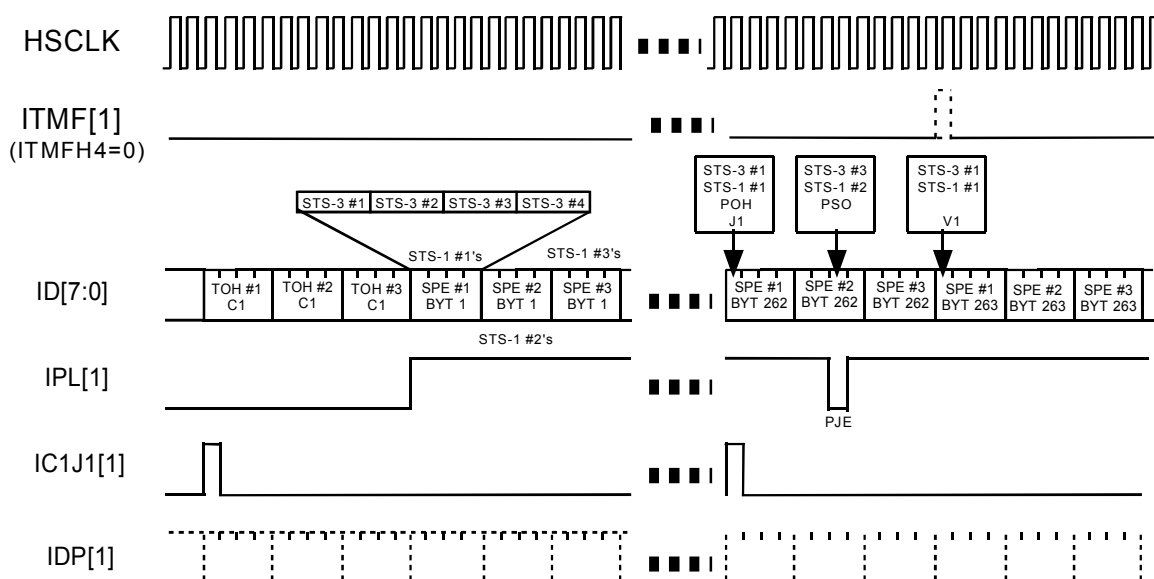


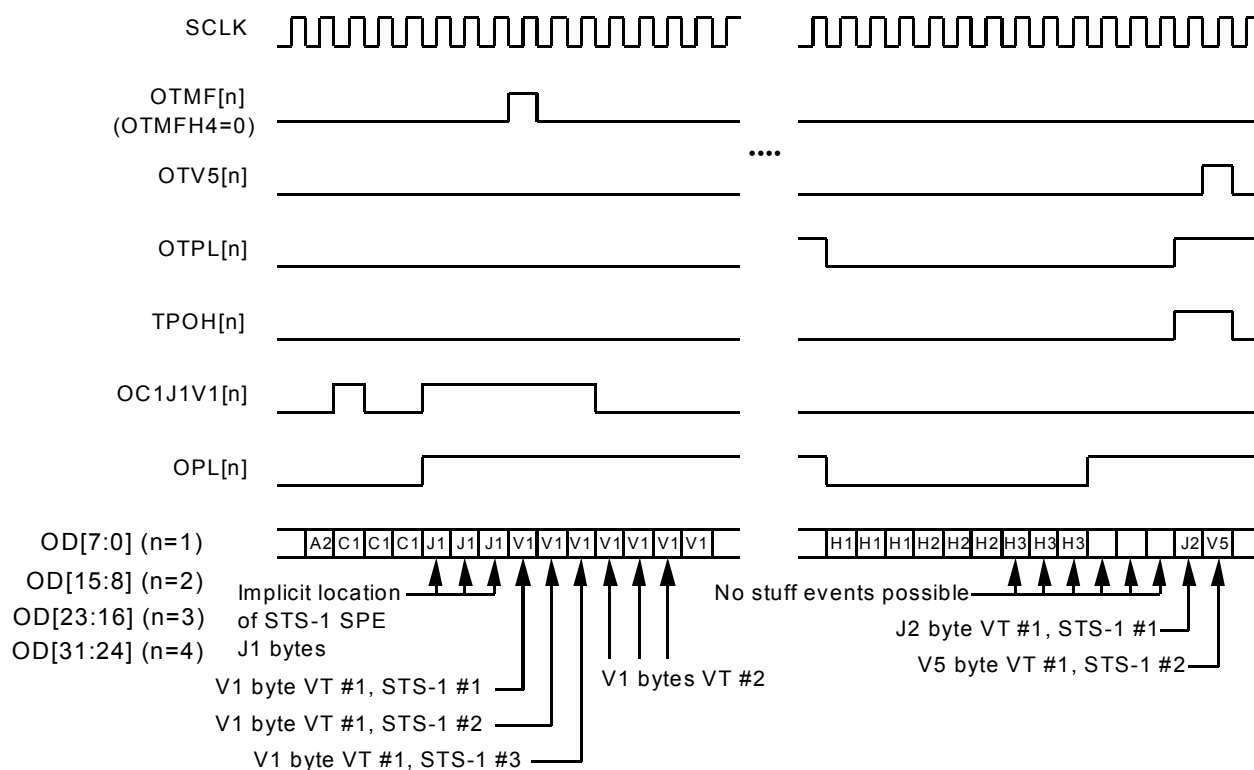


Figure 22 shows a simple four STS-3 case that outlines the function of the various input signals associated with the ID[7:0] input bus when the TUPP+622 is in STM-4 (STS-12) input interface mode (IHSMODEB set low). Data on ID[7:0] is sampled on the rising edge of HSCLK. The bytes forming the STS-1 synchronous payload envelopes are identified by the IPL[1] signal being set high. The IC1J1[1] signal pulses high while IPL[1] is low to mark the position of the first C1 byte in the STS-12 transport envelope. The IC1J1[1] signal is set high for one HSCLK periods while IPL[1] is also set high to mark the J1 byte of each STS-1 SPE. In this diagram, IC1J1[1] is shown to be marking the J1 byte of STS-3 #1 STS-1 #1. The ITMF[1] signal is selectable to mark the third byte after J1 of the first tributary in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF[1] is shown to be marking the V1 byte of the first tributary multiframe in STS-3 #1 STS-1 #1. This diagram also applies to the AU3 mode as it is equivalent to the STS-1 mode, except for nomenclature.

**Figure 22 - STM-4 Input Bus Timing - STS-1/AU3 Case**



The timing of the TUPP+622 output buses when it is in STM-1 (STS-3) output interface mode (OHSMODEB set high) is illustrated in Figure 23 where  $n$  is {1, 2, 3, 4}. This diagram shows the relationships of the output signals in STS-1 mode associated with each of the four output buses. Data on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]) is updated on the rising edge of SCLK. The OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) signal pulses high with OPL[1] (OPL[2], OPL[3], OPL[4]) signal set low to mark the position of the C1 byte of the first STS-1 stream in every frame of the STS-3 transport envelope on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]). In STS-1 mode, the position of the J1 bytes and the STS-1 SPEs is determined by the value written to the STP Outgoing Pointer MSB and LSB registers. All three STS-1 SPEs are aligned in the STS-3 transport envelope. This register settable alignment is reflected in the outgoing stream control signals OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) and OPL[1] (OPL[2], OPL[3], OPL[4]). OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) pulses high with OPL[1] (OPL[2], OPL[3], OPL[4]) signal set high to mark all three J1 bytes and the third byte after J1 of the first tributary in each STS-1 stream. OPL[1] (OPL[2], OPL[3], OPL[4]) identifies the SPE bytes on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]). The OTMF[1] (OTMF[2], OTMF[3], OTMF[4]) input marks the frame containing V1 bytes in OD[7:0] (OD[15:8], OD[23:16], OD[31:24]). It is sampled only at the first V1 byte position of the first STS-1 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL[1] (OTPL[2], OTPL[3], OTPL[4]) signal being set high. The OTV5[1] (OTV5[2], OTV5[3], OTV5[4]) signal pulses high to mark the V5 bytes of each outgoing tributary. The TPOH[1] (TPOH[2], TPOH[3], TPOH[4]) signal marks the tributary path overhead bytes (V5, J2, Z6 and Z7) of each outgoing tributary. In this simple example, all STS-1 SPEs are aligned to the STS-3 transport envelope such that the J1 bytes directly follow the C1 bytes. Other alignments are possible. The four output buses can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the output buses may be different. This diagram also applies to the AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

**Figure 23 - STM-1 Output Bus Timing - STS-1 SPEs / AU3 VCs Case**


The timing of the TUPP+622 output buses when it is in STM-1 (STS-3) output interface mode (OHSMODEB set high) is illustrated in Figure 24 where  $n$  is {1, 2, 3, 4}. This diagram shows the relationships of the output signals in AU4 mode associated with each of the four output buses. The operation of the various signals is analogous to the STS-1 mode, except that there is only a single J1. This timing applies regardless of whether individual tributary payload processors are configured for TUG3 or TU3 mode. Data on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]) is updated on the rising edge of SCLK. The OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) signal pulses high with OPL[1] (OPL[2], OPL[3], OPL[4]) signal set low to mark the position of the single C1 byte in every frame of the AU4 transport envelope on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]). In AU4 mode, the position of the single J1 byte and the VC4 is determined by the value written to the STP Outgoing Pointer MSB and LSB registers. This register settable alignment is reflected in the outgoing stream control signals OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) and OPL[1] (OPL[2], OPL[3], OPL[4]). OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) pulses high with OPL[1] (OPL[2], OPL[3], OPL[4]) signal set high to mark the J1 byte and the third byte after J1 of the first tributary in the AU4 stream. OPL[1] (OPL[2], OPL[3], OPL[4]) identifies the payload bytes on OD[7:0] (OD[15:8], OD[23:16], OD[31:24]). The OTMF[1] (OTMF[2], OTMF[3], OTMF[4]) input marks the frame containing V1 bytes in OD[7:0] (OD[15:8], OD[23:16], OD[31:24]). It is sampled only at the J1 plus one byte position of the first TUG3 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL[1] (OTPL[2], OTPL[3], OTPL[4]) signal being set high. The OTV5[1] (OTV5[2], OTV5[3], OTV5[4]) signal pulses high to mark the V5 bytes of each outgoing tributary. The TPOH[1] (TPOH[2], TPOH[3], TPOH[4]) signal pulses high to mark the tributary path overhead bytes (V5, J2, Z6 and Z7) of each outgoing tributary. In this simple example, the VC4 is aligned to the STM-1 transport envelope such that the J1 byte directly follows the C1 byte. Other alignments are possible. The four output buses can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the output buses may be different.

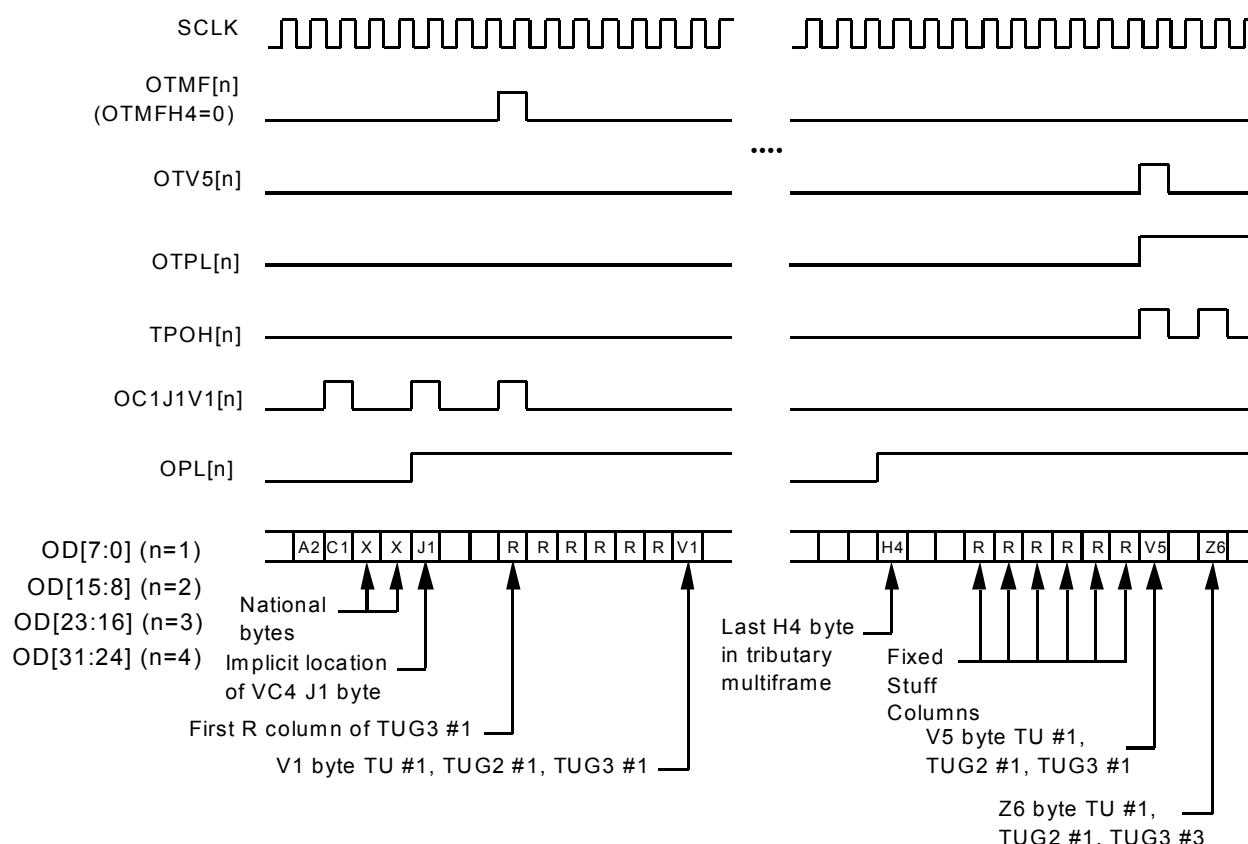
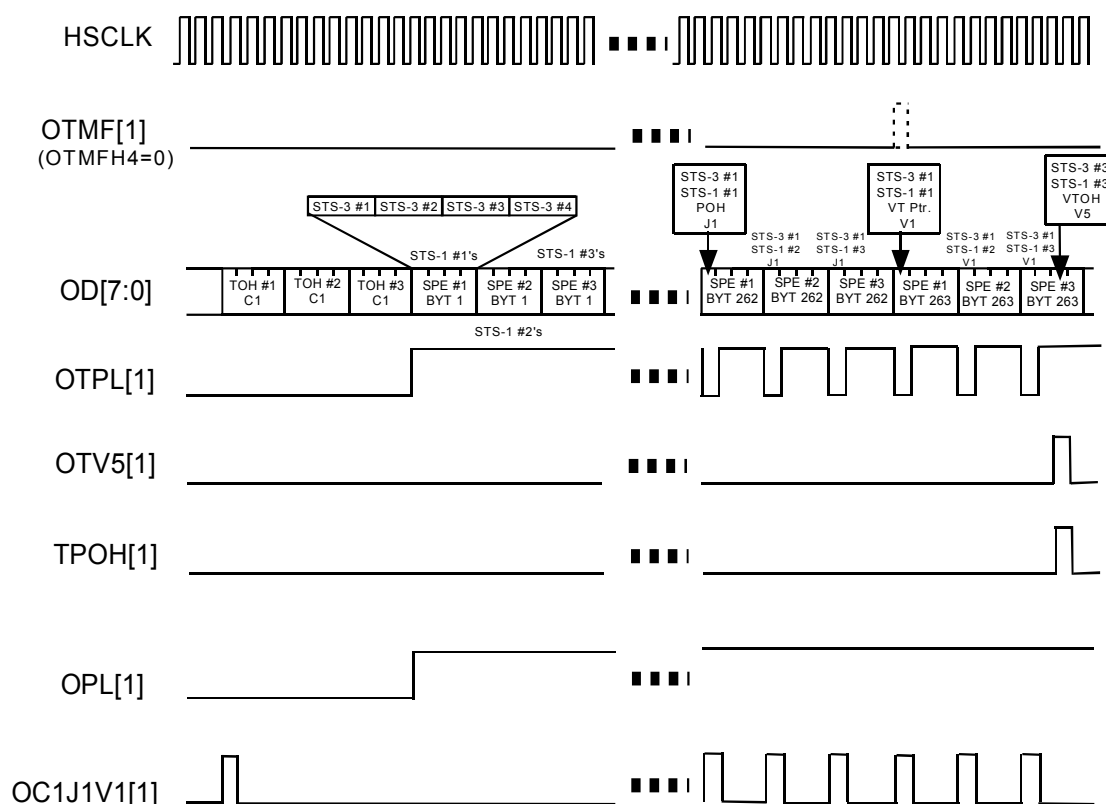
**Figure 24 - STM-1 Output Bus Timing - AU4 VC Case**

Figure 25 shows a simple four STS-3 case that outlines the function of the various output signals associated with the OD[7:0] output bus when the TUPP+622 is in STM-4 (STS-12) output interface mode (OHSMODEB set low). Data on OD[7:0] is updated on the rising edge of HSCLK. The OC1J1V1[1] signal pulses high with OPL[1] signal set low to mark the position of the C1 byte of the first STS-1 stream in every frame of the STS-12 transport envelope on OD[7:0]. In STS-1 mode, the position of the J1 bytes and the STS-1 SPEs in an STS-3 is determined by the value written to the corresponding STP Outgoing Pointer MSB and LSB registers. All three STS-1 SPEs are aligned in an STS-3 stream. This register settable alignment is reflected in the outgoing control signals OC1J1V1[1] and OPL[1]. OC1J1V1[1] pulses high with OPL[1] set high to mark the J1 bytes and the third byte after J1 of the first tributary in each STS-1 stream within the STS-12. OPL[1] identifies the SPE bytes on OD[7:0]. The OTMF[1] input marks the frame containing V1 bytes. It is sampled only at the first V1 byte position of the first STS-1 stream in each of the STS-3 #1, #2, #3 and #4

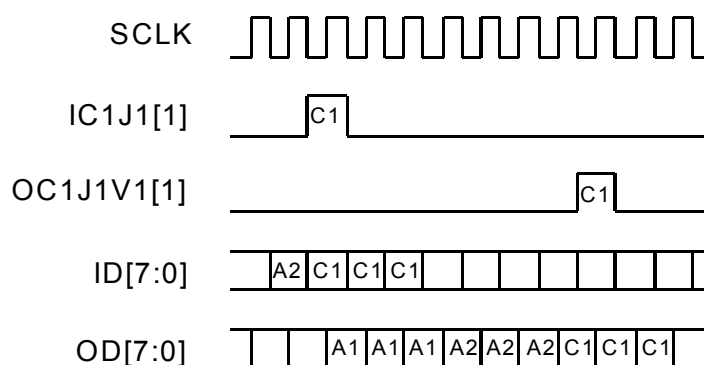
streams within the STS-12 transport envelope. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL[1] signal being set high. The OTV5[1] signal pulses high to mark the V5 bytes of each outgoing tributary. The TPOH[1] signal marks the tributary path overhead bytes (V5, J2, Z6 and Z7) of each outgoing tributary. This diagram also applies to the AU3 mode as it is equivalent to STS-1 mode, except for nomenclature. The four STS-3's (STM-1's) in the outgoing STS-12 stream can be independently configured to handle STS-1/AU3 or AU4 and the SPE/VC alignments of the STS-3 (STM-1) streams may be different.

**Figure 25 - STM-4 Output Bus Timing - STS-1 SPEs / AU3 VCs Case**



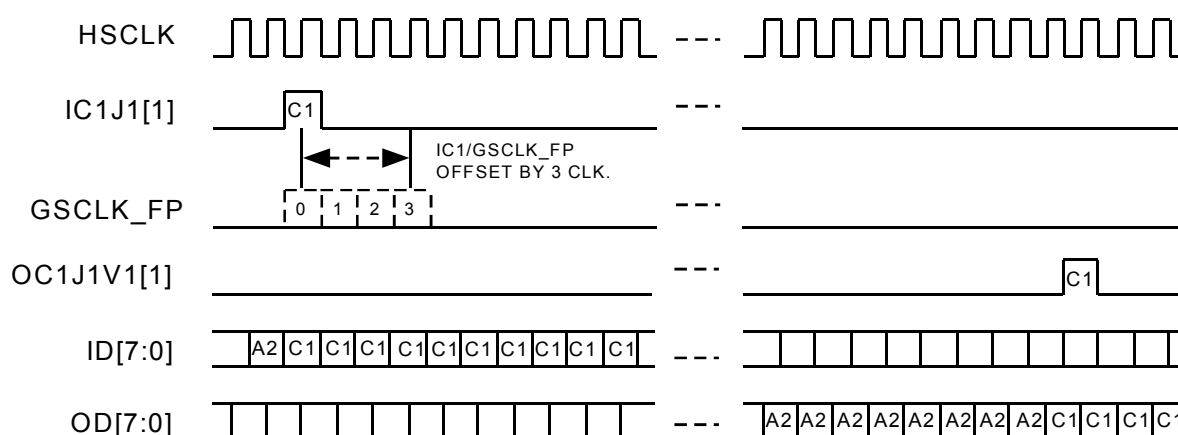
The three tributary payload processors (VTPP) in an STM-1 (STS-3) tributary processor (STP) may be individually disabled or bypassed using the corresponding TUGEN or TUGBYP register bits, respectively. Incoming data destined to a disabled or bypassed processor is re-transmitted unchanged to the outgoing data after some delay. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay. Figure 26 shows the delay for the end to end data path delay from ID[7:0] input to OD[7:0] output in the STM-1 (STS-3) interface mode (IHSMODEB and OHSMODEB set high). The delay from the rising edge of SCLK where TUPP+622 samples ID[7:0] to the rising edge of SCLK where a downstream device samples OD[7:0] is 7 cycles. This diagram also applies to the ID[15:8], ID[23:16] and ID[31:24] input buses and their corresponding output buses. This end-to-end data-path delay is also applicable to the transport frame delay between IC1J1[1] (IC1J1[2], IC1J1[3], IC1J1[4]) and the OC1 portion of OC1J1V1[1] (OC1J1V1[2], OC1J1V1[3], OC1J1V1[4]) in normal tributary processing mode.

**Figure 26 - STM-1 (STS-3) Interface, By-passed and Normal Transport Frame Delay Functional Timing**



The three tributary payload processors (VTPP) in each of the four STM-1 (STS-3) tributary processors (STP) in the TUPP+622 may be individually disabled or bypassed using the corresponding TUGEN or TUGBYP register bits, respectively. Incoming data destined to a disabled or bypassed processor is re-transmitted unchanged to the outgoing data after some delay. The amount of delay from the incoming to the outgoing data stream is a function of the internal data-path pipeline delay and the relative phase of the corresponding incoming frame pulse (IC1J1[1]) and the GSCLK\_FP input signal. Figure 27 shows the end to end data path delay from ID[7:0] input to OD[7:0] output for the four possible alignments of IC1J1[1] in relation to GSCLK\_FP when TUPP+622 is in the STM-4 (STS-12) interface mode (IHSMODEB and OHSMODEB set low). The delay from the rising edge of HSCLK where TUPP+622 samples ID[7:0] to the rising edge of HSCLK where a downstream device samples OD[7:0] is 30, 31, 32 or 33 cycles for an IC1/GSCLK\_FP offset of zero, one, two or three respectively. This end-to-end data-path delay is also applicable to the transport frame delay between IC1J1[1] and the OC1 portion of OC1J1V1[1] in normal tributary processing mode.

**Figure 27 - STM-4 (STS-12) Interface, By-passed and Normal Transport Frame Delay Functional Timing**





The tributary overhead serial interface associated with the STM-1 (STS-3) tributary processor (STP) #1 is shown in Figure 28. The tributary path overhead bytes in each of the STS-1 (AU3) or TUG3 streams on ID[7:0] are individually serialized on POH[3:1]. The most significant bit of the V5 byte of the first tributary (TU#1, TUG2 #1) of each STS-1 stream is identified by a logic high value on the corresponding POHEN[3:1] output. All four tributary path overhead bytes (V5, J2, Z6, Z7) are shifted out once per payload frame. Since the nominal arrival rate of overhead is once per multiframe, each overhead byte is presented on POH an average of four times. To distinguish the first presentation of an overhead byte from subsequent repeat presentations, the corresponding POHEN[3:1] output is set high to mark a fresh byte and set low to mark a stale byte. POHCK provides timing for the POH[3:1], POHFP[3:1] and POHEN[3:1] outputs. POHCK is a 9.72 MHz clock and run continuously.

Tributaries on POH are arranged in the order of transmission as in the incoming data stream ID[7:0]. I.e., TU #1 of TUG2 #1, TU#1 of TUG2 #2, ... TU #1 of TUG2 #7, TU #2 of TUG2 #1, ... TU #2 of TUG2 #7, TU #3 of TUG2 #1, ... TU #4 of TUG2 #7. Timeslot assignment on POH is unrelated to the configuration of the tributary group. Timeslots for four tributaries are always reserved for any tributary group even if it is configured for TU12, VT3 or TU2. At timeslots devoted to non-existent tributaries, for example, tributary 2, 3 and 4 of a TUG2 configured for TU2, POH and POHEN will be set low. The path overhead frame pulse, POHFP, identifies the most significant bit of the first tributary (TU #1 of TUG2 #1) on POH.

In TU3 mode, the POH stream carries the nine path overhead bytes. The bytes are shifted out twice per payload frame. The assignment of TU3 POH bytes to lower order tributary overhead timeslots are:

|         |                                              |
|---------|----------------------------------------------|
| TU3, J1 | -> TU #1, TUG2 #1, V5 and TU #3, TUG2 #1, V5 |
| TU3, B3 | -> TU #1, TUG2 #1, J2 and TU #3, TUG2 #1, J2 |
| TU3, C2 | -> TU #1, TUG2 #1, Z6 and TU #3, TUG2 #1, Z6 |
| TU3, G1 | -> TU #1, TUG2 #1, Z7 and TU #3, TUG2 #1, Z7 |
| TU3, F2 | -> TU #1, TUG2 #2, V5 and TU #3, TUG2 #2, V5 |
| TU3, H4 | -> TU #1, TUG2 #2, J2 and TU #3, TUG2 #2, J2 |
| TU3, Z3 | -> TU #1, TUG2 #2, Z6 and TU #3, TUG2 #2, Z6 |

TU3, Z4 -> TU #1, TUG2 #2, Z7 and TU #3, TUG2 #2, Z7

TU3, Z5 -> TU #1, TUG2 #3, V5 and TU #1, TUG2 #3, V5

This functional timing also applies to tributary overhead serial interfaces, POH[6:4], POH[9:7] and POH[12:10] associated with the STM-1 (STS-3) tributary processor (STP) #2, #3 and #4, respectively.

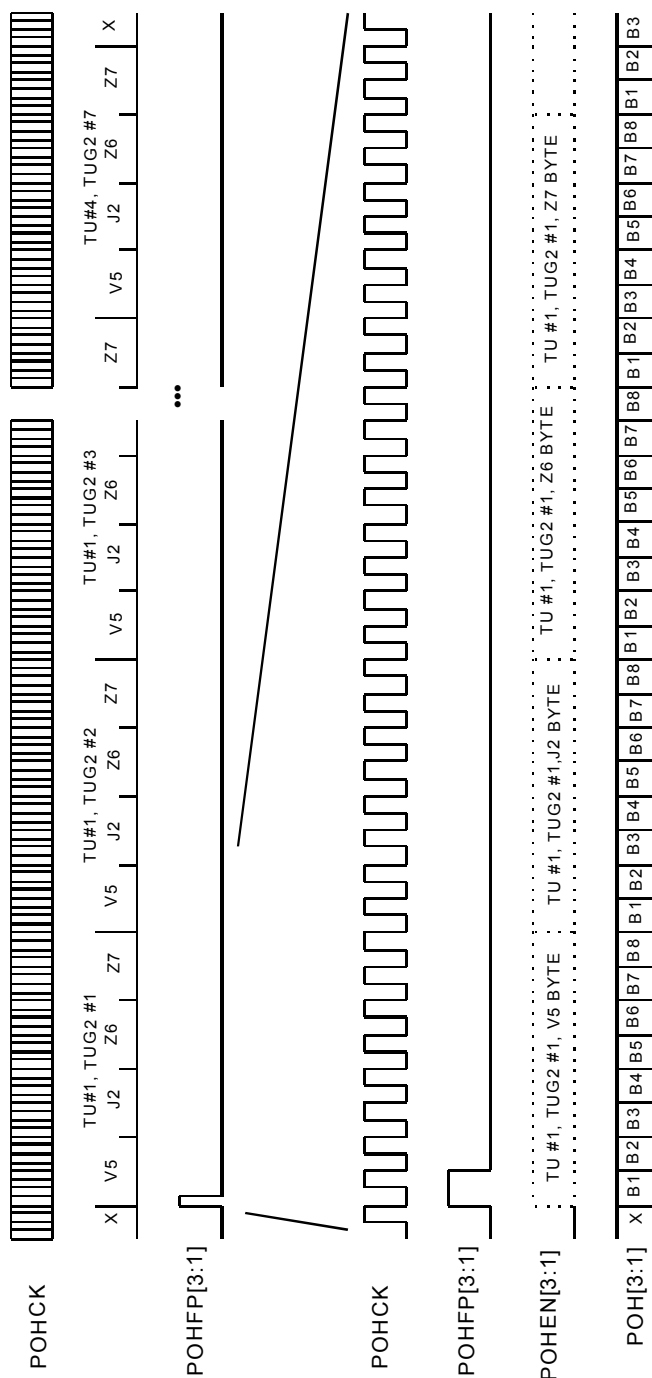
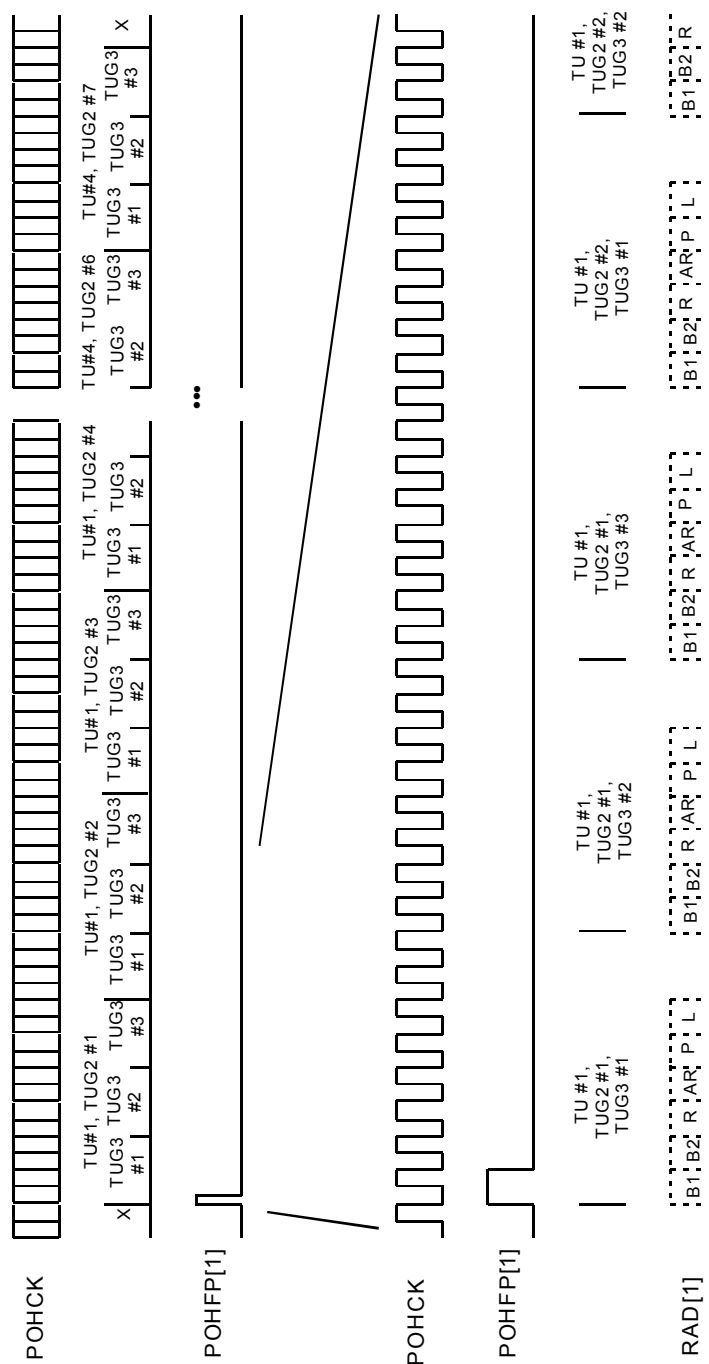
**Figure 28 - Tributary Path Overhead Serialization Functional Timing**


Figure 28 shows the timing of the receive alarm port associated with the STM-1 (STS-3) tributary processor (STP) #1. Timing is provided by the POHCK output which is a continuous 9.72 MHz clock. The BIP-2, RDI, auxiliary RDI, PDI and LOM indications of all the tributaries in the incoming stream are combined and reported on the RAD[1] output. The bits labeled B1 and B2 reports the number of BIP-2 errors. If the number of BIP-2 errors is one, only one of B1 is set high. Both B1 and B2 are set high when two BIP-2 errors are detected. The bit labeled R and AR reports the remote defect indication (RDI) and auxiliary remote defect indication (ARDI) status of the associated tributary. They are set high due to incoming AIS, LOP, PSLM, PSLU, TIM, TIU and LOM. The bit labeled P report the path defect indication (PDI-P) due to tributary path defect indication PDI-V, AIS, LOP and UNEQ states. The PDI-P indications allow a downstream device where the tributaries are aggregated into an SPE to form a C2 byte containing the count of tributaries in alarm state. The bit labeled L reports the loss of multiframe state. Tributaries timeslots on RAD[1] are arranged in the order of transmission as in the incoming data stream ID[7:0]. I.e., TU #1 of TUG2 #1 TUG3 #1, TU #1 of TUG2 #1 TUG3 #2, TU #1 of TUG2 #1 TUG3 #3, TU#1 of TUG2 #2 TUG3 #2, ... TU #1 of TUG2 #7 TUG3 #3, TU #2 of TUG2 #1 TUG3 #1, ..., TU #2 of TUG2 #7 TUG3 #3, ..., TU #4 of TUG2 #7 TUG3 #3. Timeslot assignment on RAD[1] is unrelated to the configuration of the tributary group. Timeslots for four tributaries are always reserved for any tributary group even if it is configured for TU12, VT3 or TU2. At timeslots devoted to non-existent tributaries, for example, tributary 2, 3 and 4 of a TUG2 configured for TU2, RAD[1] will be set low. The path overhead frame pulse, POHFP[1], identifies the BIP-2 error indication for the odd-numbered bits of the first tributary (TU #1 of TUG2 #1 STS-1 #1) on RAD[1].

When a TUG3 stream is configured in TU3 mode, the segregation of RAD[1], for that TUG3, into tributary timeslots are dissolved. Any bit normally carrying tributary BIP-2 indications may carry a TU3 BIP-8 error indication. All remaining bits will report the associated state of the TU3 stream simultaneously.

This functional timing also applies to receive alarm ports, RAD[2], RAD[3] and RAD[4] associated with the STM-1 (STS-3) tributary processor (STP) #2, #3 and #4, respectively. The path overhead frame pulse signals, POHFP[4], POHFP[7] and POHFP[10], identify the BIP-2 error indication for the odd-numbered bits of the first tributary (TU #1 of TUG2 #1 STS-1 #1) on RAD[2], RAD[3] and RAD[4] respectively. When a TUG3 is bypassed by setting corresponding TUGEN bit in the VTPP Configuration register low, no performance monitoring is performed on

that TUG3 stream. Consequently, the timeslots associated with the bypassed stream on the RAD stream are invalid.

**Figure 29 - Receive Alarm Port Functional Timing**


## 15 **ABSOLUTE MAXIMUM RATINGS**

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions.

**Table 7 -TUPP+622 Absolute Maximum Ratings**

|                                         |                 |
|-----------------------------------------|-----------------|
| Ambient Temperature under Bias          | -40°C to +85°C  |
| Storage Temperature                     | -40°C to +125°C |
| Supply Voltage (+3.3 Volt $V_{DD3.3}$ ) | -0.3V to +4.6V  |
| Supply Voltage (+2.5 Volt $V_{DD2.5}$ ) | -0.3V to +3.5V  |
| Voltage on Any Pin                      | -0.3V to +6.0V  |
| Static Discharge Voltage                | $\pm 1000$ V    |
| Latch-Up Current                        | $\pm 100$ mA    |
| DC Input Current                        | $\pm 20$ mA     |
| Lead Temperature                        | +230°C          |
| Absolute Maximum Junction Temperature   | +150°C          |

## 16 D.C. CHARACTERISTICS

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD3.3} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DD2.5} = 2.5\text{ V} \pm 0.2\text{ V}$ )

**Table 8 -TUPP+622 D.C. Characteristics**

| Symbol      | Parameter                                  | Min  | Typ | Max  | Units         | Conditions                                           |
|-------------|--------------------------------------------|------|-----|------|---------------|------------------------------------------------------|
| $V_{DD3.3}$ | 3.3V Power Supply                          | 3.0  | 3.3 | 3.6  | Volts         | Note 5.                                              |
| $V_{DD2.5}$ | 2.5V Power Supply                          | 2.3  | 2.5 | 2.7  | Volts         | Note 5.                                              |
| $V_{IL}$    | Input Low Voltage                          | -0.5 |     | 0.8  | Volts         | Guaranteed Input LOW Voltage.                        |
| $V_{IH}$    | Input High Voltage                         | 2.0  |     | 5.5  | Volts         | Guaranteed Input HIGH Voltage. Note 6.               |
| $V_{OL}$    | Output or Bi-directional Low Voltage       |      |     | 0.4  | Volts         | $I_{OL} = -8\text{ mA}$ for all outputs. Notes 3, 5. |
| $V_{OH}$    | Output or Bi-directional High Voltage      | 2.4  |     |      | Volts         | $I_{OH} = 8\text{ mA}$ for all outputs. Notes 3, 5.  |
| $V_{T+}$    | Schmitt Triggered Input High Voltage       | 2.0  |     | 5.5  | Volts         |                                                      |
| $V_{T-}$    | Schmitt Triggered Input Low Voltage        | -0.5 |     | 0.8  | Volts         |                                                      |
| $V_{TH}$    | Schmitt Triggered Input Hysteresis Voltage |      | 0.5 |      | Volts         | Note 6.                                              |
| $I_{ILPU}$  | Input Low Current                          | +10  | 45  | +100 | $\mu\text{A}$ | $V_{IL} = \text{GND}$ , Notes 1, 3, 5.               |
| $I_{IHPU}$  | Input High Current                         | -10  | 0   | +10  | $\mu\text{A}$ | $V_{IH} = V_{DD}$ , Notes 1, 3                       |
| $I_{IL}$    | Input Low Current                          | -10  | 0   | +10  | $\mu\text{A}$ | $V_{IL} = \text{GND}$ , Notes 2, 3                   |
| $I_{IH}$    | Input High Current                         | -10  | 0   | +10  | $\mu\text{A}$ | $V_{IH} = V_{DD}$ , Notes 2, 3                       |



| Symbol               | Parameter                  | Min | Typ | Max | Units | Conditions                                                                                                    |
|----------------------|----------------------------|-----|-----|-----|-------|---------------------------------------------------------------------------------------------------------------|
| C <sub>IN</sub>      | Input Capacitance          |     | 5   |     | pF    | All pins. Excludes package. Package typically 2 pF. Note 5.                                                   |
| C <sub>OUT</sub>     | Output Capacitance         |     | 5   |     | pF    | All pins. Excludes package. Package typically 2 pF. Note 5.                                                   |
| C <sub>IO</sub>      | Bi-directional Capacitance |     | 5   |     | pF    | All pins. Excludes package. Package typically 2 pF. Note 5.                                                   |
| LPIN                 | Pin Inductance             |     | 2   |     | nH    | All pins. Note 5.                                                                                             |
| I <sub>DDOP3.3</sub> | Operating Current.         |     |     | 60  | mA    | V <sub>DD3.3</sub> = 3.6V, V <sub>DD2.5</sub> = 2.7V, Outputs Unloaded.<br>HSCLK=77.76 MHz.<br>SCLK=GSCLK[0]. |
| I <sub>DDOP2.5</sub> | Operating Current.         |     |     | 395 | mA    | V <sub>DD3.3</sub> = 3.6V, V <sub>DD2.5</sub> = 2.7V, Outputs Unloaded.<br>HSCLK=77.76 MHz.<br>SCLK=GSCLK[0]. |

**Notes on D.C. Characteristics:**

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bi-directional pin with internal pull-down resistor.
5. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.

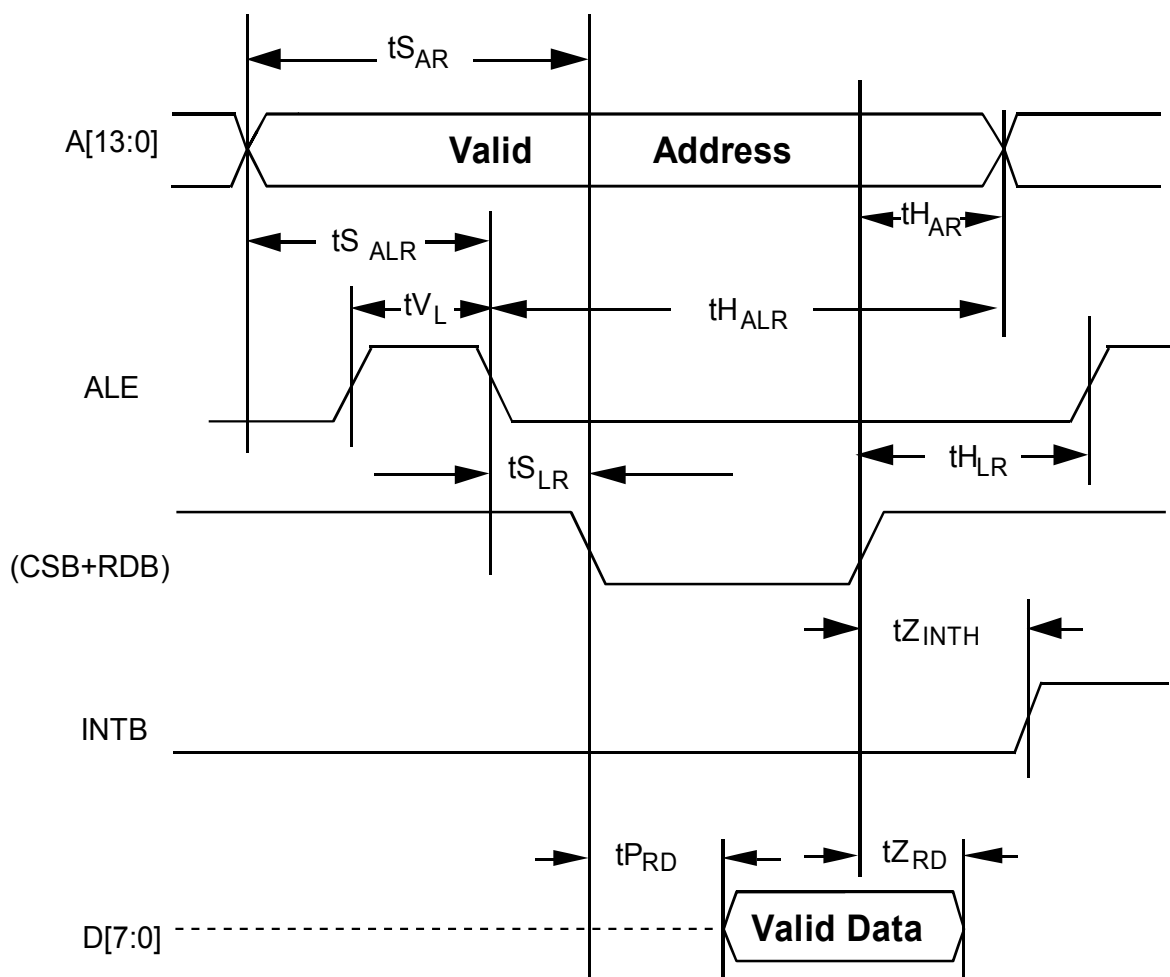
6. Input pin is 5-Volt tolerant.

## **17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS**

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD3.3} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DD2.5} = 2.5\text{ V} \pm 0.2\text{ V}$ )

**Table 9 - Microprocessor Interface Read Access**

| <b>Symbol</b>      | <b>Parameter</b>                           | <b>Min</b> | <b>Max</b> | <b>Units</b> |
|--------------------|--------------------------------------------|------------|------------|--------------|
| t <sub>SAR</sub>   | Address to Valid Read Set-up Time          | 10         |            | ns           |
| t <sub>HAR</sub>   | Address to Valid Read Hold Time            | 5          |            | ns           |
| t <sub>SALR</sub>  | Address to Latch Set-up Time               | 10         |            | ns           |
| t <sub>HALR</sub>  | Address to Latch Hold Time                 | 10         |            | ns           |
| t <sub>VL</sub>    | Valid Latch Pulse Width                    | 5          |            | ns           |
| t <sub>SLR</sub>   | Latch to Read Set-up                       | 0          |            | ns           |
| t <sub>HLR</sub>   | Latch to Read Hold                         | 5          |            | ns           |
| t <sub>SRWB</sub>  | RWB to Read Set-up                         | 10         |            | ns           |
| t <sub>HRWB</sub>  | RWB to Read Hold                           | 5          |            | ns           |
| t <sub>PRD</sub>   | Valid Read to Valid Data Propagation Delay |            | 70         | ns           |
| t <sub>ZRD</sub>   | Valid Read Negated to Output Tri-state     |            | 20         | ns           |
| t <sub>ZINTH</sub> | Valid Read Negated to Output Tri-state     |            | 50         | ns           |

**Figure 30 - Microprocessor Interface Read Access Timing (Intel Mode)**



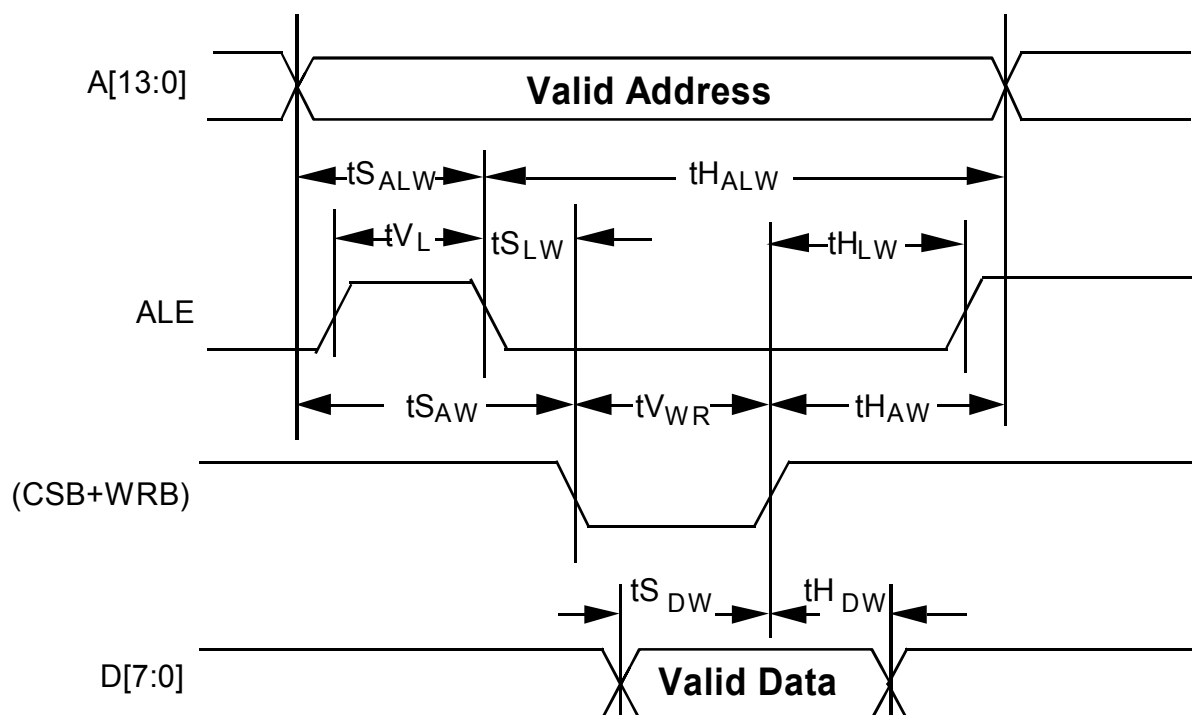
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**Notes on Microprocessor Interface Read Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. In Intel mode, a valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In Motorola mode, a valid read cycle is defined as a logical AND of the E signal, the RWB signal and the inverted CSB signal.
5. Microprocessor Interface timing applies to normal mode register accesses only.
6. In non-multiplexed address/data bus architectures, ALE should be held high, parameters  $t_{S_{ALR}}$ ,  $t_{H_{ALR}}$ ,  $t_{V_L}$ , and  $t_{S_{LR}}$  are not applicable.
7. Parameter  $t_{H_{AR}}$  and  $t_{S_{AR}}$  are not applicable if address latching is used.
8. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
9. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

**Table 10 - Microprocessor Interface Write Access**

| Symbol | Parameter                          | Min | Max | Units |
|--------|------------------------------------|-----|-----|-------|
| tSAW   | Address to Valid Write Set-up Time | 10  |     | ns    |
| tSDW   | Data to Valid Write Set-up Time    | 20  |     | ns    |
| tSALW  | Address to Latch Set-up Time       | 10  |     | ns    |
| tHALW  | Address to Latch Hold Time         | 10  |     | ns    |
| tVL    | Valid Latch Pulse Width            | 5   |     | ns    |
| tSLW   | Latch to Write Set-up              | 0   |     | ns    |
| tHLW   | Latch to Write Hold                | 5   |     | ns    |
| tSRWB  | RWB to Write Set-up                | 10  |     | ns    |
| tHRWB  | RWB to Write Hold                  | 5   |     | ns    |
| tHDW   | Data to Valid Write Hold Time      | 5   |     | ns    |
| tHAW   | Address to Valid Write Hold Time   | 5   |     | ns    |
| tVWR   | Valid Write Pulse Width            | 40  |     | ns    |

**Figure 32 - Microprocessor Interface Write Access Timing (Intel Mode)**



The diagram illustrates the timing relationships for the 68000 microprocessor. The signals shown are:

- A[13:0]**: Address bus, labeled "Valid Address".
- RWB**: Read/Write/Busy signal.
- ALE**: Address Latch Enable signal.
- ( $\overline{\text{CSB}}$  & E)**: Chip Select and Enable signal.
- D[7:0]**: Data bus, labeled "Valid Data".

Key timing parameters are indicated by arrows:

- $t_{SAW}$ : Setup time for address A[13:0] before the first clock edge.
- $t_{SRWB}$ : Setup time for RWB before the first clock edge.
- $t_{HAW}$ : Hold time for address A[13:0] after the first clock edge.
- $t_{HAW}$ : Hold time for address A[13:0] after the last clock edge.
- $t_{VWR}$ : Valid time for  $\overline{\text{CSB}}$  & E before the first clock edge.
- $t_{HAW}$ : Hold time for  $\overline{\text{CSB}}$  & E after the last clock edge.
- $t_{SDW}$ : Setup time for data D[7:0] before the first clock edge.
- $t_{HDW}$ : Hold time for data D[7:0] after the last clock edge.

1. In Intel mode, a valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In Motorola mode, a valid write cycle is defined as a logical AND of the E signal, the inverted RWB signal and the inverted CSB signal.

3. Microprocessor timing applies to normal mode register accesses only.
4. In non-multiplexed address/data bus architectures, ALE should be held high, parameters  $t_{S_{ALW}}$ ,  $t_{H_{ALW}}$ ,  $t_{V_L}$ , and  $t_{S_{LW}}$  are not applicable.
5. Parameters  $t_{H_{AW}}$  and  $t_{S_{AW}}$  are not applicable if address latching is used.
6. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

## 18 TUPP+622 TIMING CHARACTERISTICS

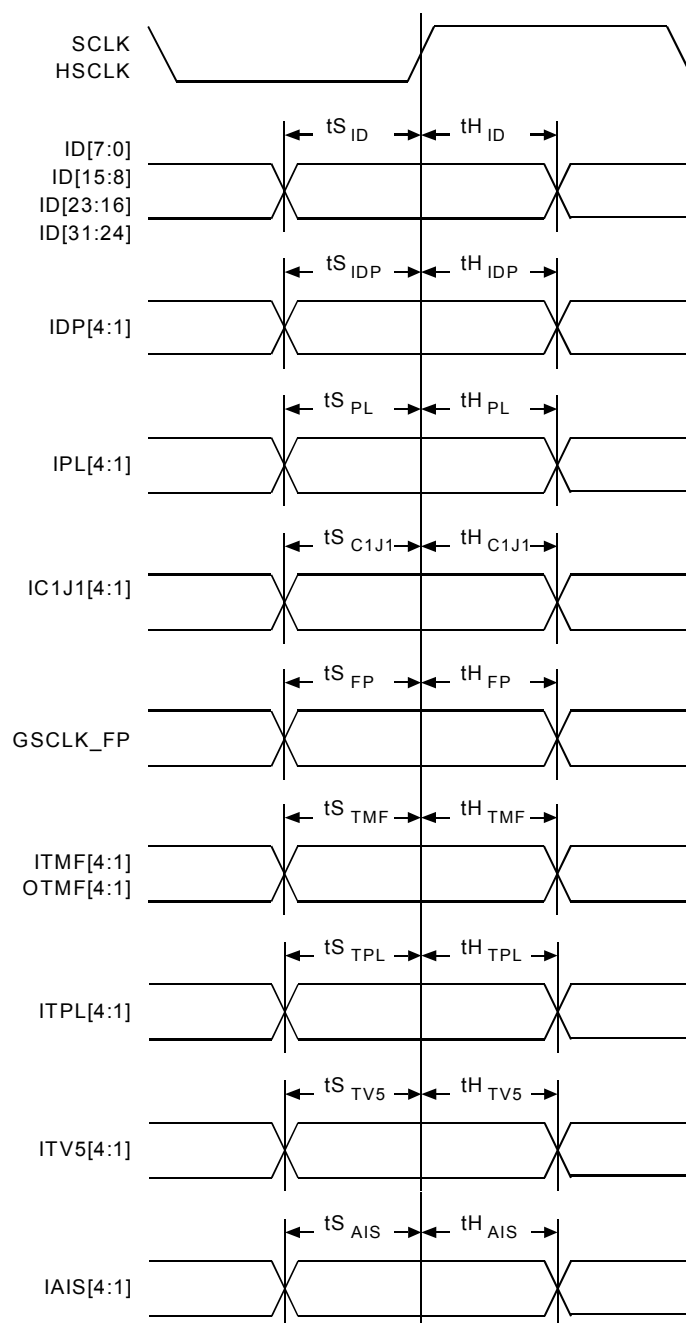
( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD3.3} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DD2.5} = 2.5\text{ V} \pm 0.2\text{ V}$ )

**Table 11 - TUPP+622 Input Timing For SCLK (Figure 34)**

| Symbol             | Description                                         | Min | Max | Units |
|--------------------|-----------------------------------------------------|-----|-----|-------|
|                    | SCLK Frequency (nominally 19.44 MHz )               |     | 20  | MHz   |
|                    | SCLK Duty Cycle                                     | 40  | 60  | %     |
| t <sub>SID</sub>   | ID[7:0], ID[15:8], ID[23:16], ID[31:24] Set-up Time | 3   |     | ns    |
| t <sub>HID</sub>   | ID[7:0], ID[15:8], ID[23:16], ID[31:24] Hold Time   | 1.5 |     | ns    |
| t <sub>SIDP</sub>  | IDP[4:1] Set-up Time                                | 3   |     | ns    |
| t <sub>HIDP</sub>  | IDP[4:1] Hold Time                                  | 1.5 |     | ns    |
| t <sub>SPL</sub>   | IPL[4:1] Set-Up Time                                | 3   |     | ns    |
| t <sub>HP_L</sub>  | IPL[4:1] Hold Time                                  | 1.5 |     | ns    |
| t <sub>SC1J1</sub> | IC1J1[4:1] Set-Up Time                              | 3   |     | ns    |
| t <sub>HC1J1</sub> | IC1J1[4:1] Hold Time                                | 1.5 |     | ns    |
| t <sub>STMF</sub>  | ITMF[4:1] and OTMF[4:1] Set-Up Time                 | 3   |     | ns    |
| t <sub>HTMF</sub>  | ITMF[4:1] and OTMF[4:1] Hold Time                   | 1.5 |     | ns    |
| t <sub>STPL</sub>  | ITPL[4:1] Set-Up Time                               | 3   |     | ns    |
| t <sub>HTPL</sub>  | ITPL[4:1] Hold Time                                 | 1.5 |     | ns    |
| t <sub>STV5</sub>  | ITV5[4:1] Set-Up Time                               | 3   |     | ns    |
| t <sub>HTV5</sub>  | ITV5[4:1] Hold Time                                 | 1.5 |     | ns    |
| t <sub>SAIS</sub>  | IAIS[4:1] Set-Up Time                               | 3   |     | ns    |
| t <sub>HAIS</sub>  | IAIS[4:1] Hold Time                                 | 1.5 |     | ns    |

**Table 12 - TUPP+622 Input Timing HSCLK (Figure 34)**

| Symbol             | Description                           | Min | Max | Units |
|--------------------|---------------------------------------|-----|-----|-------|
|                    | HSCLK Frequency (nominally 77.76 MHz) |     | 80  | MHz   |
|                    | HSCLK Duty Cycle                      | 40  | 60  | %     |
| t <sub>SID</sub>   | ID[7:0] Set-up Time                   | 2   |     | ns    |
| t <sub>HID</sub>   | ID[7:0] Hold Time                     | 0   |     | ns    |
| t <sub>SIDP</sub>  | IDP[1] Set-up Time                    | 2   |     | ns    |
| t <sub>HIDP</sub>  | IDP[1] Hold Time                      | 0   |     | ns    |
| t <sub>SPL</sub>   | IPL[1] Set-Up Time                    | 2   |     | ns    |
| t <sub>HPL</sub>   | IPL[1] Hold Time                      | 0   |     | ns    |
| t <sub>SC1J1</sub> | IC1J1[1] Set-Up Time                  | 2   |     | ns    |
| t <sub>HC1J1</sub> | IC1J1[1] Hold Time                    | 0   |     | ns    |
| t <sub>SFP</sub>   | GSCLK_FP Set-Up Time                  | 2   |     | ns    |
| t <sub>HFP</sub>   | GSCLK_FP Hold Time                    | 0   |     | ns    |
| t <sub>STMF</sub>  | ITMF[1] and OTMF[1] Set-Up Time       | 2   |     | ns    |
| t <sub>HTMF</sub>  | ITMF[1] and OTMF[1] Hold Time         | 0   |     | ns    |
| t <sub>STPL</sub>  | ITPL[1] Set-Up Time                   | 2   |     | ns    |
| t <sub>HTPL</sub>  | ITPL[1] Hold Time                     | 0   |     | ns    |
| t <sub>STV5</sub>  | ITV5[1] Set-Up Time                   | 2   |     | ns    |
| t <sub>HTV5</sub>  | ITV5[1] Hold Time                     | 0   |     | ns    |
| t <sub>SAIS</sub>  | IAIS[1] Set-Up Time                   | 2   |     | ns    |
| t <sub>HAIS</sub>  | IAIS[1] Hold Time                     | 0   |     | ns    |

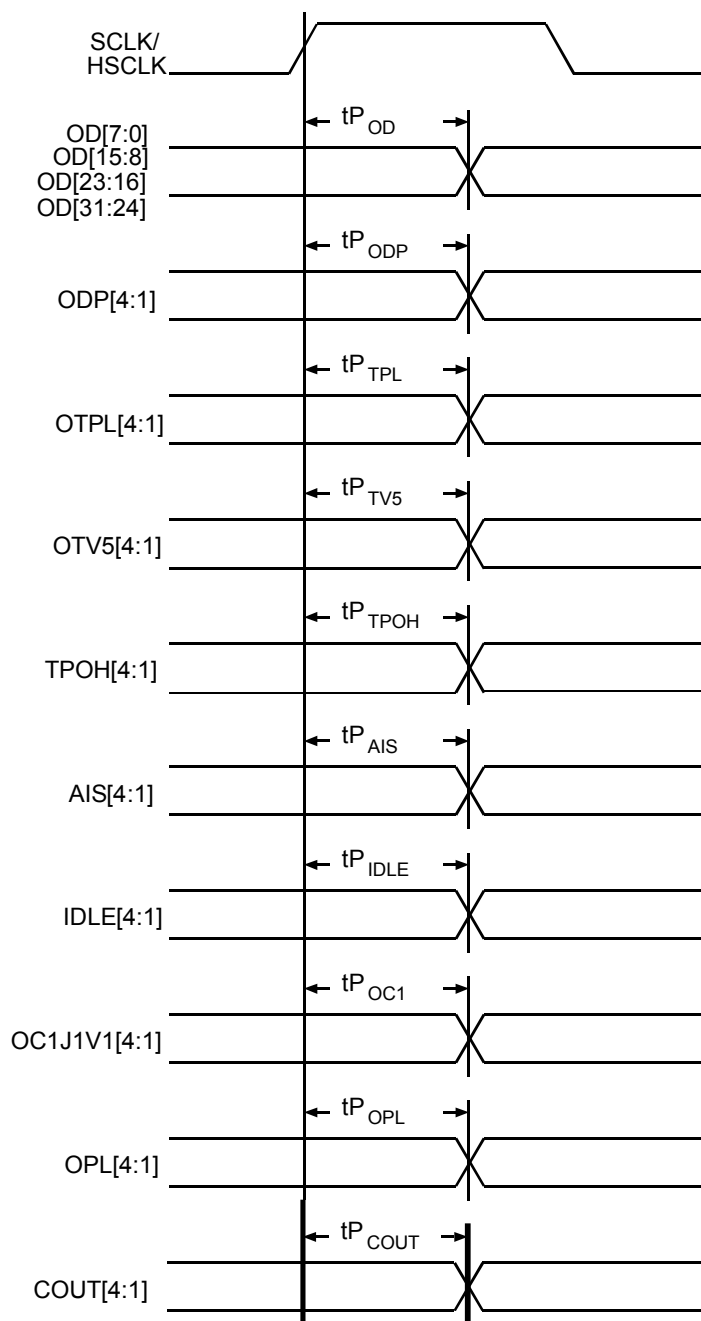
**Figure 34 - Input Timing**


### Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

**Table 13 - TUPP+622 Stream Output**

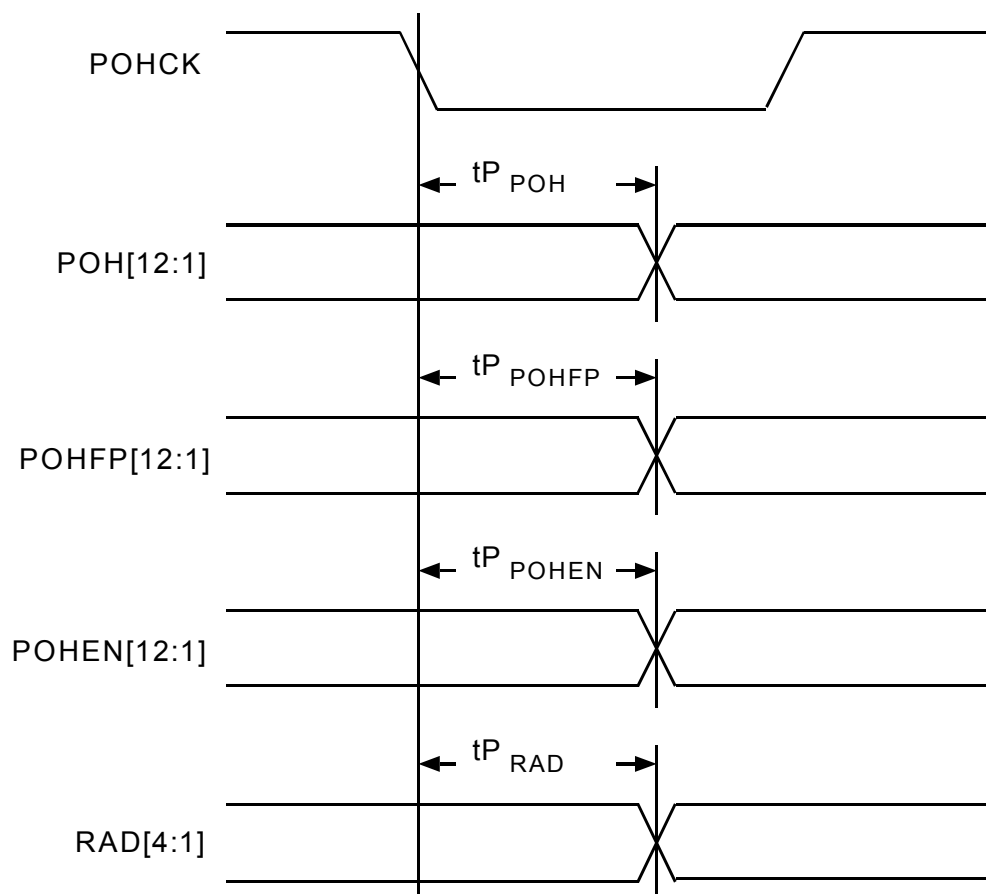
| Symbol             | Description                     | Min | Max | Units |
|--------------------|---------------------------------|-----|-----|-------|
| tP <sub>OD</sub>   | SCLK High to OD[7:0] Valid      | 3.5 | 20  | ns    |
| tP <sub>ODP</sub>  | SCLK High to ODP[4:1] Valid     | 3.5 | 20  | ns    |
| tP <sub>TPL</sub>  | SCLK High to OTPL[4:1] Valid    | 3.5 | 20  | ns    |
| tP <sub>TV5</sub>  | SCLK High to OTV5[4:1] Valid    | 3.5 | 20  | ns    |
| tP <sub>TPOH</sub> | SCLK High to TPOH[4:1] Valid    | 3.5 | 20  | ns    |
| tP <sub>AIS</sub>  | SCLK High to AIS[4:1] Valid     | 3.5 | 20  | ns    |
| tP <sub>IDLE</sub> | SCLK High to IDLE[4:1] Valid    | 3.5 | 20  | ns    |
| tP <sub>OC1</sub>  | SCLK High to OC1J1V1[4:1] Valid | 3.5 | 20  | ns    |
| tP <sub>OPL</sub>  | SCLK High to OPL[4:1] Valid     | 3.5 | 20  | ns    |
| tP <sub>COUT</sub> | SCLK High to COUT[4:1] Valid    | 3.5 | 20  | ns    |
| tP <sub>OD</sub>   | HSCLK High to OD[7:0] Valid     | 1   | 9   | ns    |
| tP <sub>ODP</sub>  | HSCLK High to ODP[1] Valid      | 1   | 9   | ns    |
| tP <sub>TPL</sub>  | HSCLK High to OTPL[1] Valid     | 1   | 9   | ns    |
| tP <sub>TV5</sub>  | HSCLK High to OTV5[1] Valid     | 1   | 9   | ns    |
| tP <sub>TPOH</sub> | HSCLK High to TPOH[1] Valid     | 1   | 9   | ns    |
| tP <sub>AIS</sub>  | HSCLK High to AIS[1] Valid      | 1   | 9   | ns    |
| tP <sub>IDLE</sub> | HSCLK High to IDLE[1] Valid     | 1   | 9   | ns    |
| tP <sub>OC1</sub>  | HSCLK High to OC1J1V1[1] Valid  | 1   | 9   | ns    |
| tP <sub>OPL</sub>  | HSCLK High to OPL[1] Valid      | 1   | 9   | ns    |
| tP <sub>COUT</sub> | HSCLK High to COUT[1] Valid     | 1   | 9   | ns    |

**Figure 35- Stream Output Timing**




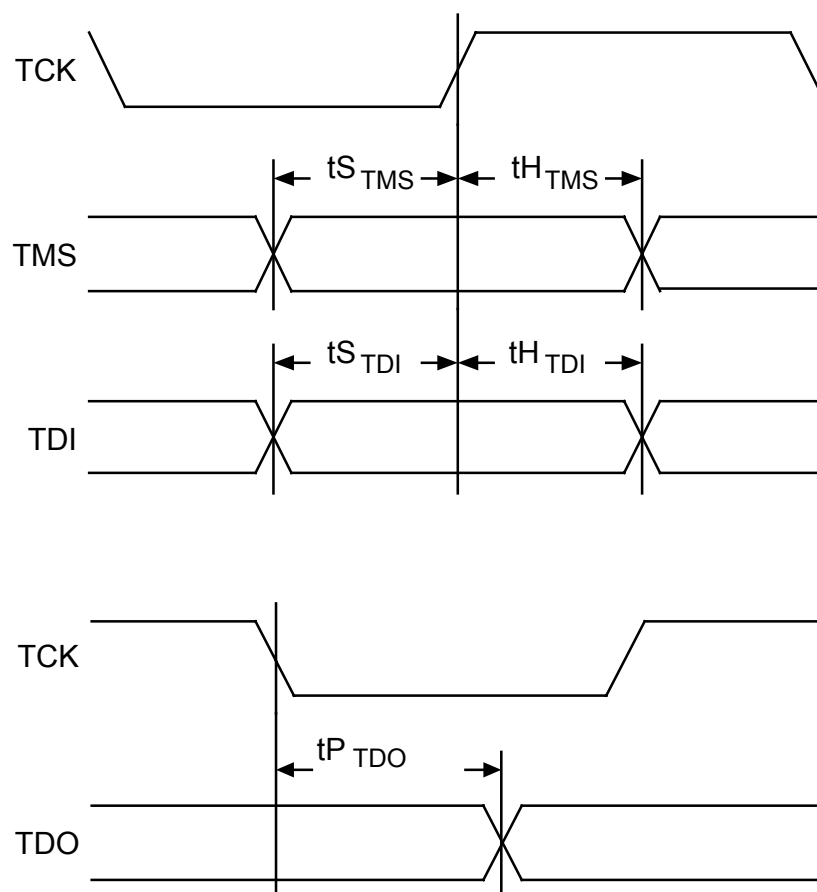
**Table 14 - TUPP+622 Path Overhead Output (Figure 36)**

| Symbol              | Description                                                                                            | Min | Max | Units |
|---------------------|--------------------------------------------------------------------------------------------------------|-----|-----|-------|
|                     | POHCK Duty Cycle<br>(POHCK is nominally 9.72 MHz. POHCK is a divide by two of the system clock, SCLK.) | 40  | 60  | %     |
| tP <sub>POH</sub>   | POHCK Low to POH[12:1] Valid                                                                           | -5  | 25  | ns    |
| tP <sub>POHFP</sub> | POHCK Low to POHFP[12:1] Valid                                                                         | -5  | 25  | ns    |
| tP <sub>POHEN</sub> | POHCK Low to POHEN[12:1] Valid                                                                         | -5  | 25  | ns    |
| tP <sub>RAD</sub>   | POHCK Low to RAD[4:1] Valid                                                                            | -5  | 25  | ns    |

**Figure 36 - Path Overhead Output Timing**

**Table 15 - JTAG Port Interface (Figure 37)**

| Symbol                       | Description            | Min | Max | Units |
|------------------------------|------------------------|-----|-----|-------|
|                              | TCK Frequency          |     | 4   | MHz   |
|                              | TCK Duty Cycle         | 40  | 60  | %     |
| t <sub>TMS</sub>             | TMS Set-up time to TCK | 50  |     | ns    |
| t <sub>H<sub>TMS</sub></sub> | TMS Hold time to TCK   | 50  |     | ns    |
| t <sub>TDI</sub>             | TDI Set-up time to TCK | 50  |     | ns    |
| t <sub>H<sub>TDI</sub></sub> | TDI Hold time to TCK   | 50  |     | ns    |
| t <sub>P<sub>TDO</sub></sub> | TCK Low to TDO Valid   | 2   | 50  | ns    |

**Figure 37 - JTAG Port Interface Timing**

**Notes on Output Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 50 pF load on the outputs except where indicated. For output propagation delays measured with respect to the HSCLK, a 30 pF load on the outputs are used.

3. Output propagation delays of signal outputs that are specified in relation to a reference output are measured with a 50 pF load on both the signal output and the reference output except where indicated.

## **19 ORDERING AND THERMAL INFORMATION**

**Table 16 - Ordering information**

| PART NO.  | DESCRIPTION                      |
|-----------|----------------------------------|
| PM5363-BI | 304 Super Ball Grid Array (SBGA) |

**Table 17 - Thermal information – Theta Jc**

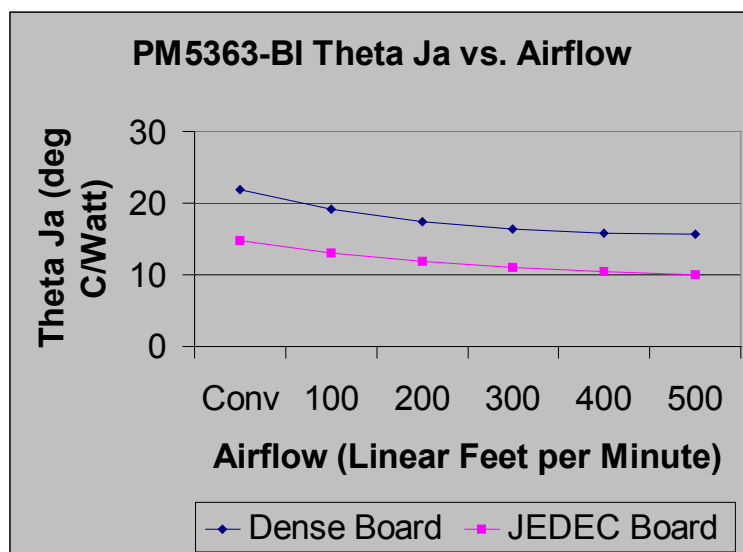
| PART NO.  | AMBIENT TEMPERATURE | Theta Jc |
|-----------|---------------------|----------|
| PM5363-BI | -40°C to 85°C       | 1 °C/W   |

**Table 18 - Maximum Junction Temperature**

|           |                                                        |        |
|-----------|--------------------------------------------------------|--------|
| PM5363-BI | Maximum Junction Temperature for Long Term Reliability | 105 °C |
|-----------|--------------------------------------------------------|--------|

**Table 19 - Thermal information – Theta Ja vs. Airflow**

| Theta Ja @ specified power | Convection | Forced Air (Linear Feet per Minute) |      |      |      |      |
|----------------------------|------------|-------------------------------------|------|------|------|------|
|                            |            | 100                                 | 200  | 300  | 400  | 500  |
| Dense Board                | 21.9       | 19.2                                | 17.4 | 16.3 | 15.8 | 15.6 |
| JEDEC Board                | 14.7       | 13.0                                | 11.8 | 11.0 | 10.4 | 10.0 |

**Figure 38 - Theta Ja vs. Airflow Plot**

**Notes on Theta Ja vs. Airflow:**

1. Dense Board – Board with 3x3 array of the same device with spacing of 4mm between device. 6 layer board (3 signal layers, 3 power layers). Chart represents device in the center of the array. Chart represents values obtained through simulation.

- 
2. JEDEC Board – Single component on a board. 4 layer board (2 signal layers, 2 power layers), metallization length x width = 94 mm x 94 mm. Board dimension = 114mmx142mm. JEDEC Measurement as per EIA/GESD51-1.



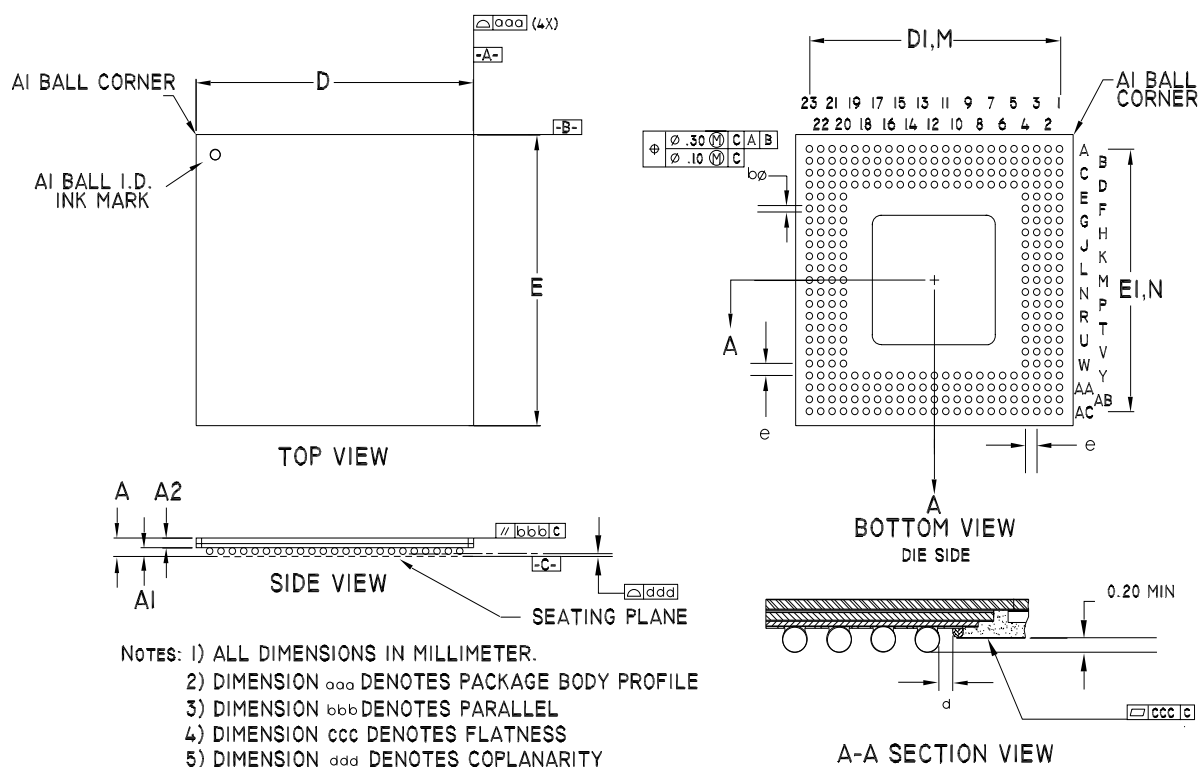
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## 20 MECHANICAL INFORMATION

Figure 39 - Mechanical Drawing 304 Pin Super Ball Grid Array (SBGA)



| PACKAGE TYPE: 304 PIN THERMAL BALL GRID ARRAY |      |      |      |       |       |       |       |       |      |      |      |      |      |      |      |
|-----------------------------------------------|------|------|------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|
| BODY SIZE: 31 x 31 x 1.51 MM                  |      |      |      |       |       |       |       |       |      |      |      |      |      |      |      |
| DIM.                                          | A    | AI   | A2   | D     | DI    | E     | EI    | M,N   | e    | b    | aaa  | bbb  | ccc  | ddd  | d    |
| MIN.                                          | 1.30 | 0.50 | 0.80 | 30.90 | 27.84 | 30.90 | 27.84 |       |      | 0.60 |      |      |      |      | 0.50 |
| NOM.                                          | 1.51 | 0.60 | 0.91 | 31.00 | 27.94 | 31.00 | 27.94 | 23x23 | 1.27 | 0.75 |      |      |      |      |      |
| MAX.                                          | 1.70 | 0.70 | 1.00 | 31.10 | 28.04 | 31.10 | 28.04 |       |      | 0.90 | 0.20 | 0.25 | 0.20 | 0.20 |      |

*TUPP+622*



*PM5363 TUPP+622*

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## **NOTES**

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