PM5372

TSE

TRANSMISSION SWITCHING ELEMENT

CORE CARD REFERENCE DESIGN

PRELIMINARY

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PUBLIC REVISION HISTORY

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1 DEFINITIONS

ADM	Add Drop Multiplexer
CHESS	Channelizer Engine for SONET/SDH
CPLD	Complex Programmable Logic Device
LVDS	Low Voltage Differential Signaling
POS	Packet over SONET
P-TCB	Parallel Telecombus at 77.76 MHz
RWSEL	Read Working Link Select
SCOEB	SYSCLK Output Enable Bar
SDEN	SYSCLK Distribution Enable
S-TCB	Serial Telecombus at 777.6 MHz
xCMP	Grouped Connection Memory Page signals

2 FEATURES

The TSE Core Card Reference Design belongs to the CHESS Set Reference Design and has the following features:

- Demonstrates a non-blocking cross-connect (switch matrix building block) with STS-1 granularity and scalability from 40 Gb/s to 160 Gb/s in a single stage, and up to 2.5 Tb/s in multi-stage fabrics.
- Highlights a single PM5372 TSE Transmission Switch Element device with backplane access to all 64 ingress and 64 egress STS-12 equivalent S-TCB ports.
- 777.6 MHz LVDS serial telecombus (S-TCB) links to 16, OC-48 load devices through CHESS Set Backplane.
- Supports extension to redundant and expanded bandwidth fabrics using multiple cards. A single card supports 40Gb/s.
- Transparent support for UPSR, 2-BLSR, 4-BLSR architectures.
- Generates CHESS Set specific signaling for backplane distribution and manages generation between multiple cards.
- Provides a total of 9 differential PECL SYSCLK pairs to backplane for system side timing.
- Host control and monitoring through 32bit 33MHz CompactPCI interface.
- On-board power regulation provides required 1.8V and 3.3V from cPCI bus.
- Supports hot swapping.

3 APPLICATIONS

- Multiservice Add/Drop Mulitplexer
- Digital Cross Connect
- Terminal Multiplexer

4 REFERENCES

PMC-Sierra, Inc., PMC-1990713, " Transmission Switch Element Data Sheet", Issue 2, January 2000.

PMC-Sierra, Inc., PMC-200-0021, "CHESS Reference Design Hardware Manual", Issue 1, March 2000.

PMC-Sierra, Inc., PMC-1991797, "CHESS User's Guide", Issue 1, March 2000.

Bell Communication Research – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, December 1995.

PICMG, "Compact PCI Specification", Version 2.0 R2.1 Sept, 1997.

5 APPLICATION EXAMPLES

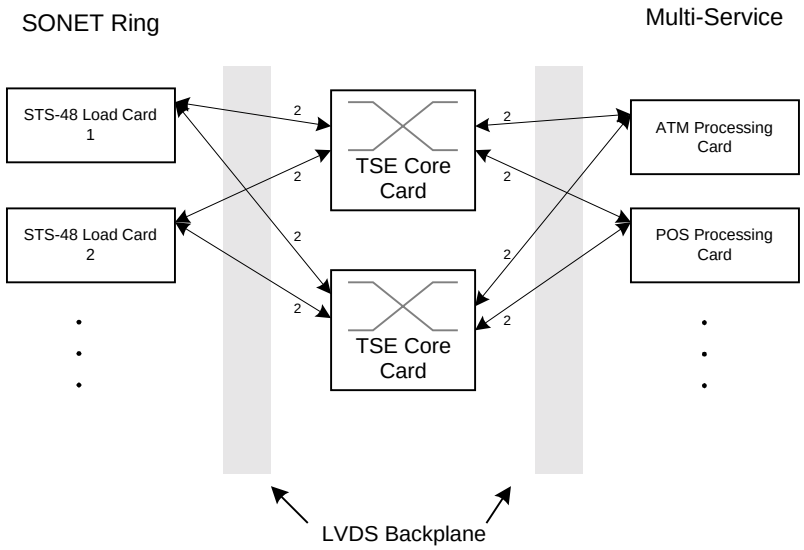
The TSE Core Card Reference Design is a building block for scalable and redundant SONET/SDH switch fabrics. It is applicable for use with any combination of line and service cards as bandwidth and ports permit. The general configuration sees a TBS device (or function) on line or service cards to connect to the ingress and egress ports on the TSE Core Card.

This design finds application in typical SONET network elements: multiservice Add/Drop multiplexer, broadband digital crossconnect and terminal multiplexer.

5.1 Add/Drop Multiplexer

In a multiservice Add/Drop Multiplexer (ADM), the TSE Core Card acts to route the different traffic types the SONET line may contain such as POS, voice, or video, to the appropriate service cards. In this way, the TSE decouples line-side PHY devices of SONET rings from multi-service system cards. Figure 1 is an example configuration for an ADM with a maximum switch bandwidth of 80Gb/s. A 40Gb/s fabric with 1:1 redundancy is formed from this configuration by adding two additional links to each TSE card from each line card.

Figure 1 - Add/Drop Multiplexer

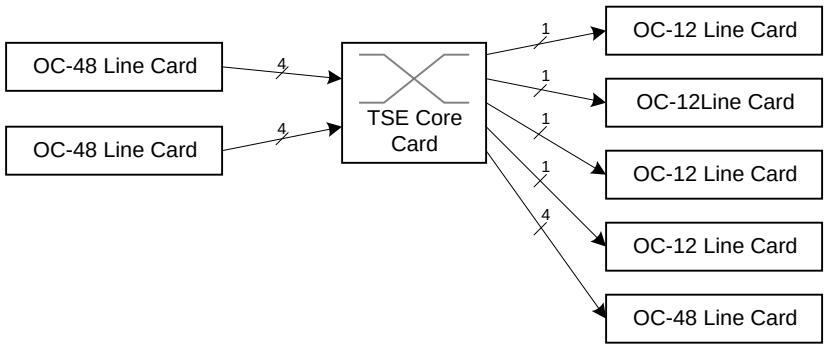


In Figure 1, each line represent both transmit and receive STS-12 bidirectional links. The TSE Core Card completes the SONET ring, routes the drop traffic to the desired processing card, and routes the add traffic to the appropriate line card. Through traffic connects from ingress line card to egress line card through the TSE Core Card. This provides an opportunity for channel spying, redundancy switchovers and traffic grooming. Add traffic is routed to a single ring or to multiple rings using multicast.

The TSE Core Card plays an important role in any UPSR, 2-BLSR, or 4-BLSR ring architecture and does not require additional configuration in any case. The architectural details are accomplished within the switch settings of the TSE device. See the CHESS User's Guide (PMC-1991797) for information on implementing ring architectures.

5.2 Broadband Digital Cross Connect

Figure 2 - Digital Cross Connect (Partially Populated)



A broadband digital cross-connect (DCC) with grooming for (12 x 64=) 768, STS-1 streams (40Gb/s throughput) is formed with a single TSE Core Card. The system bandwidth is scalable (as in any application of the TSE Reference Card) to the desired bandwidth and port count with the use of additional Core Cards. In the DCC, the TSE Card consolidates or segregates STS-1 traffic between the STS-12 equivalent flows found at each port. OC-48 and OC-192 devices are interfaced by aggregating 4 and 16 flows respectively.

A cross connect using only one eighth of the TSE Core Card ports with simple uni-directional connectivity is drawn in Figure 2. Any STS-1 from an ingress card or port can be switched to any STS-1 timeslot on any egress card or port. The number on each line indicates count of uni-directional S-TCB STS-12 streams. Bi-directional connections can be simultaneously added, greatly increasing the

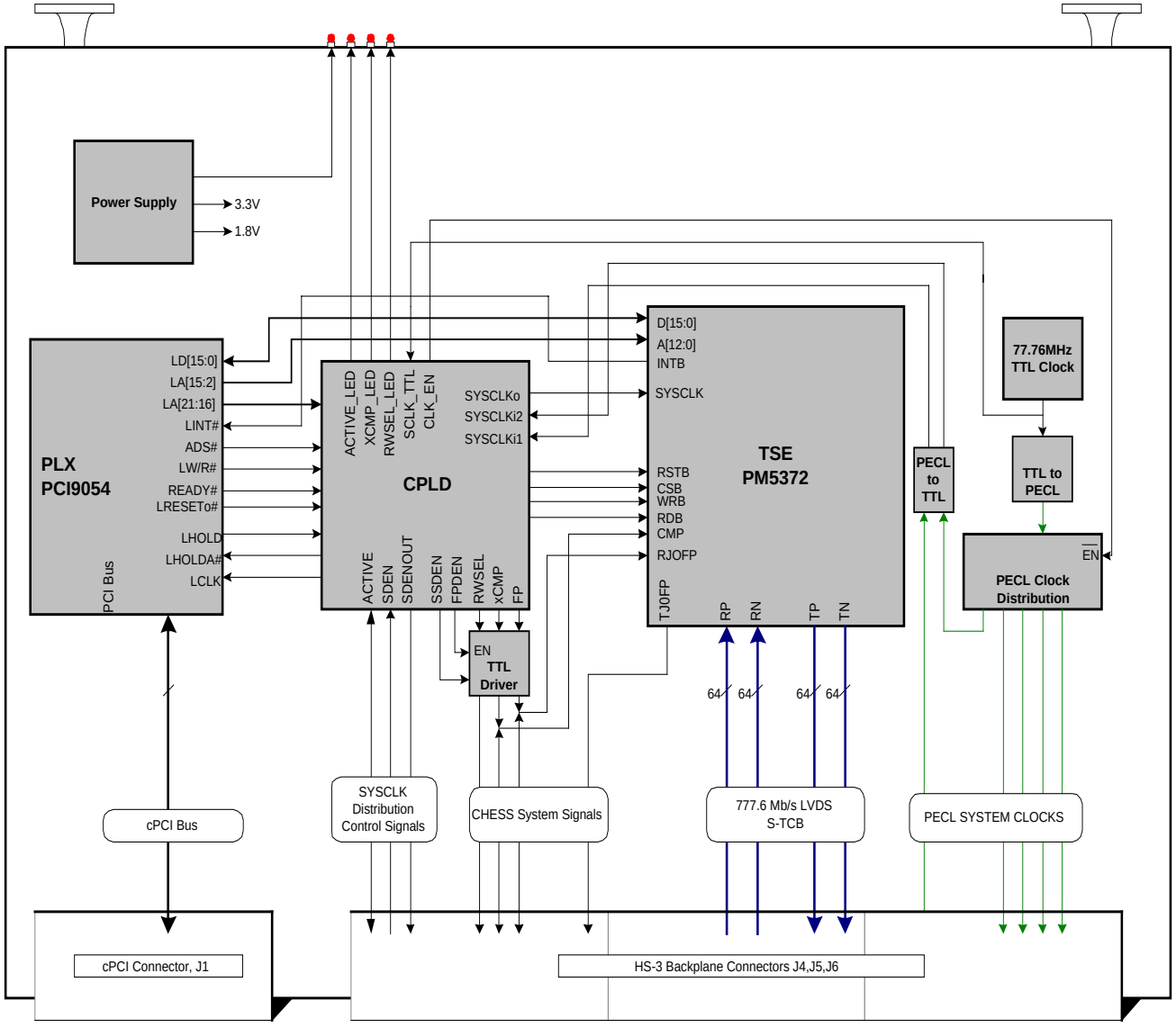
switch possibilities. Additionally, a one-to-one ratio of ingress to egress is implied here but not necessary. Multicast is supported as an output can sample data from any input.

5.3 Terminal Multiplexer

A terminal multiplexer using the TSE Core Card does not differ significantly from the ADM or DCC applications since the same decoupling is provided between the line and service cards.

Note that in all applications using the TSE Reference Design (or the PM5372) discussed here, the bandwidth is scalable with the addition of planes and stages. It is also important to note that redundancy (whether 1:1 or 1:n) can be accomplished for any fabric composition. The CHESS User's Guide (PMC-1991797) describes these issues in greater detail.

6 BLOCK DIAGRAM



7 FUNCTIONAL DESCRIPTION

This design provides an example implementation of the TSE Transmission Switching Element device and CHESS signalling (xCMP, RWSEL, SYSCLK, FP). A CPLD is used for signalling control, and a Compact PCI bus is used for the host interface.

The TSE Core Card Reference Design belongs to the CHESS Reference Design.

7.1 PM5372 TSE

The PM5372 Transmission Switch Element is a time-space-time switch fabric with 40 Gb/s bandwidth. It performs non-blocking permutation switching with STS-1 granularity on 64, STS-12 ingress ports. Each port supports streams formed by any combination of STS-1, STS-3, STS-3c, STS-12, or STS-12c. STS-48 and STS-192 flows are supported by aggregating 4 and 16 STS-12 streams. There are a total of 64 ingress and 64 egress STS-12 ports using 10B/8B encoded 777.76MHz LVDS. All of the TSE ports are available at the backplane connector.

The TSE device switches the STS-12 aligned data streams at STS-1 granularity through ingress Time, Space, and then egress Time switch stages. The time switch stages perform timeslot interchange on each STS-12 data stream. The space switch stage switches data from one STS-12 pipe to another. Each STS-1 timeslot is switched independently in the Space switch stage. The egress time switch stage then provides for an additional timeslot interchange. The result is a reconfigurably non-blocking fabric of STS-1 granularity.

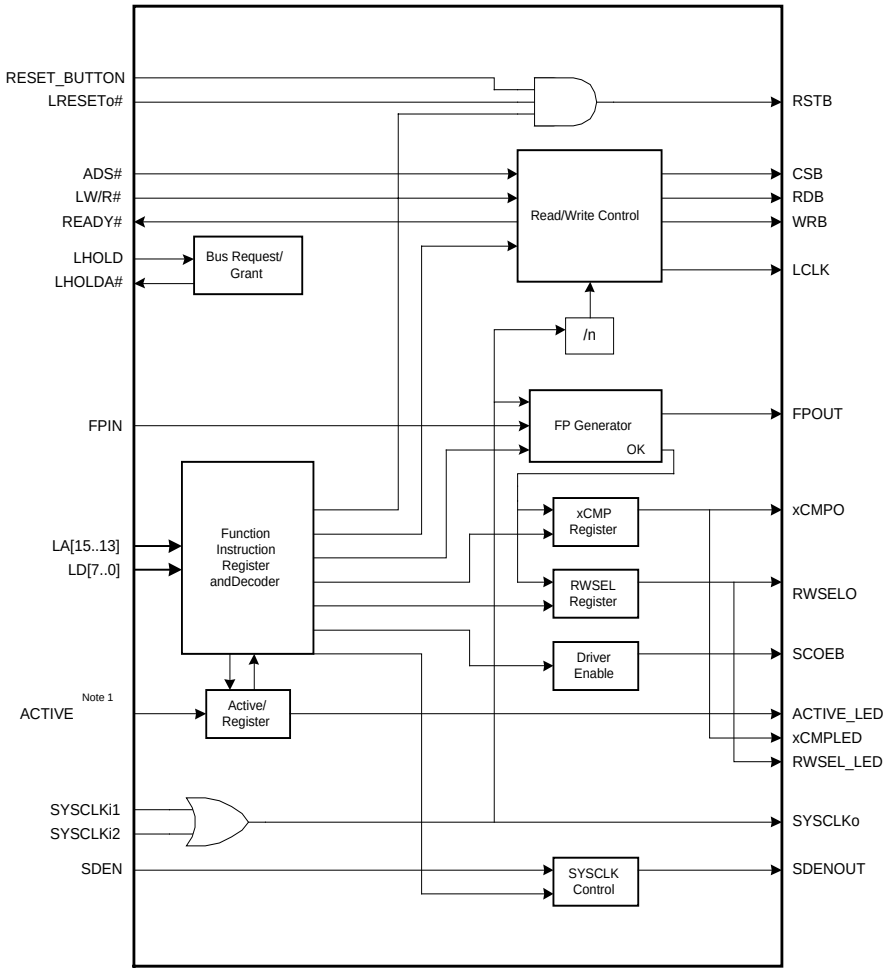
The ports are aligned and framed by the framing pulse (FP) applied to the RJ0FP pin. The TSE device decodes the 8B/10B J0 frame alignment control code found within each STS-12 stream to align the 10B characters. If the alignment criteria is met, SYNC state is entered and each stream will be aligned at the space switch boundary. The write pointers of the 64 ingress FIFOs (buffer the differences between internal timing and the LVDS interface) are reset when the J0 byte is received as expected. This provides the necessary port alignment and framing at switch boundaries.

7.2 CPLD

A complex programmable logic device (CPLD) is used to perform two functions within the TSE Core Card: 1) interface between the PM5372 TSE device and the

cPCI interface device, and 2) generation and control of CHESS system signals (xCMP, FP, RWSEL and SYSCLK).

Figure 3 - CPLD Functional Block Diagram



Note 1 Not Implemented

7.2.1 cPCI Interface

The interface to the cPCI interface chip can be summarized as follows: added signaling (LHOLD, LHOLDA#, ADS#, READY#) not support by the microprocessor interface and decoding for interface signals (RDB, WRB and CSB). Timing for the signals to the TSE device is achieved using counts of SYSCLK.

7.2.1.1 Address Space of Card

The LA<32..2> address space is allocation according to Table 1.

Table 1 - Address Bit Allocation

LA<32..2> bits	Function
13..2	TSE Normal Registers
14..2	TSE Test Registers
15	CPLD Configuration Register
32..16	Unused bits

7.2.2 Configuration Register

The CPLD provides a register for control of CHESS system signalling. Access to the register is through the cPCI interface when LA[15] = 1. The CSB pin of the TSE device is deselected and LD[7..0] is written to the register.

Table 2 - Configuration Register

Bit	Function	Default
0	CMP pin value	1
1	RWSEL pin value	1
2	FP driver enable	1
3	xCMP/RWSEL driver enable	1
4	A/B	1

Bit	Function	Default
5	Master	0
6	Reset	0
7	Reserved	0

7.2.2.1 A/B Jumpers

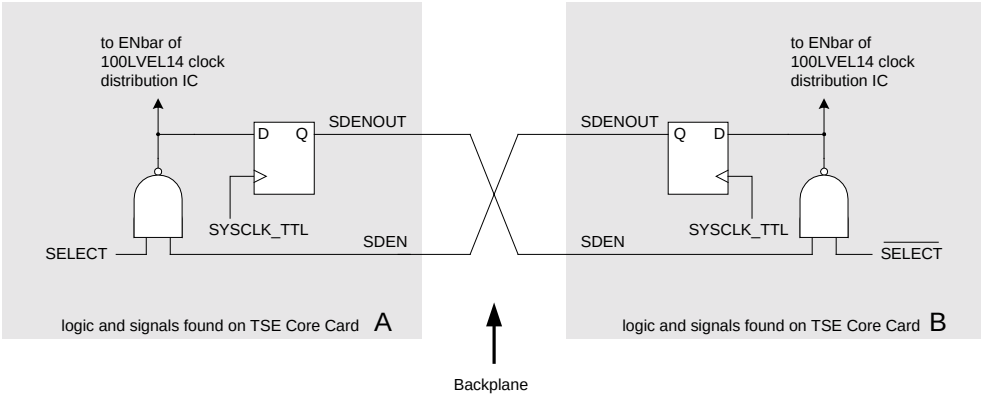
The A/B jumper can be set to differentiate between two TSE Core Cards with Configuration Bit 4. The setting of the jumper is logically XORed with Configuration Bit 4 to determine the active card.

7.2.3 SYSCLK Control

The TSE Core Card generates and distributes the 77.76 MHz CHESS system timing signal, SYSCLK. This signal is important to the timing of the S-TCB (LVDS) interface and the digital switch core timing. It is common for all devices using the S-TCB to avoid FIFO over and under runs. Essentially, frequency is the only consideration for SYSCLK as the system is not sensitive to skew. With this in mind, a centralized SYSCLK source has been implemented.

It was conceived that the source of SYSCLK be switched between two installed TSE Core Cards at specific events. For instance, this may be desired if using a redundant TSE configuration when a change from receiving Working to Protection channels is made (CHESS chipset signal RWSEL change) after the Working data stream is interrupted or has accumulated significant errors.

Figure 4 - Logic of SYSCLK Distribution Control

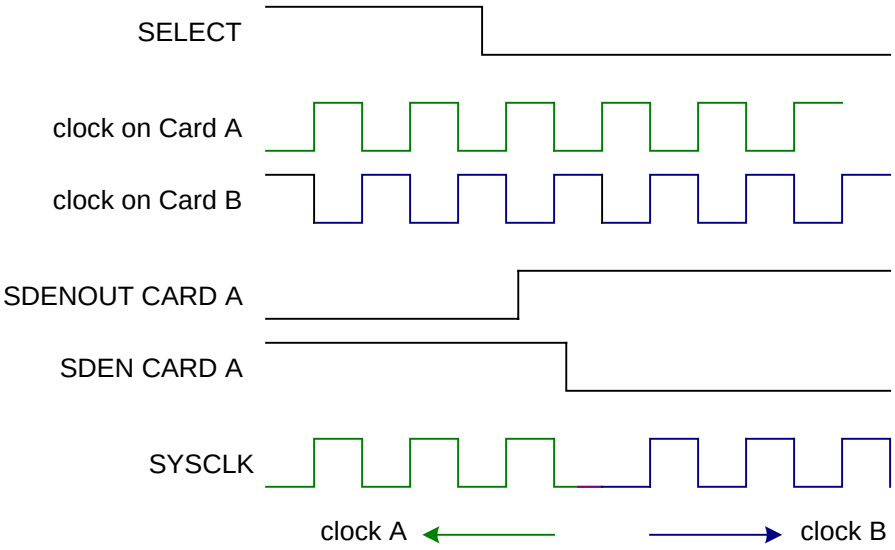


The logic in Figure 4 is used to control the switch between the unique clock sources. This configuration will avoid runt or otherwise glitched clock distribution during the switchover with minimized clock gap. With a change on SELECT, the driving board will hold SYSCLK low on a falling edge. The other card will be enabled once the SDENOUT flip-flop is clocked and will begin SYSCLK distribution on a falling edge of its SYSCLK. SYSCLK distribution is ultimately controlled using the synchronous ENbar of the MC100LVEL14 1:5 clock distribution device. ENbar is set as described in Figure 4.

The clock driver can be disabled by the CPU (via the CPLD) if a second TSE Core Card is used, or an alternate source is desired. The Active A and Active B bits of the Configuration Register holds this status.

Representative timing waveforms drawn in Figure 5 show the cessation of clock A, the resultant lost pulse (low), and the initiation of clock B. Clock B has been drawn with worst case phase.

Figure 5 - SYSCLK Switchover Timing



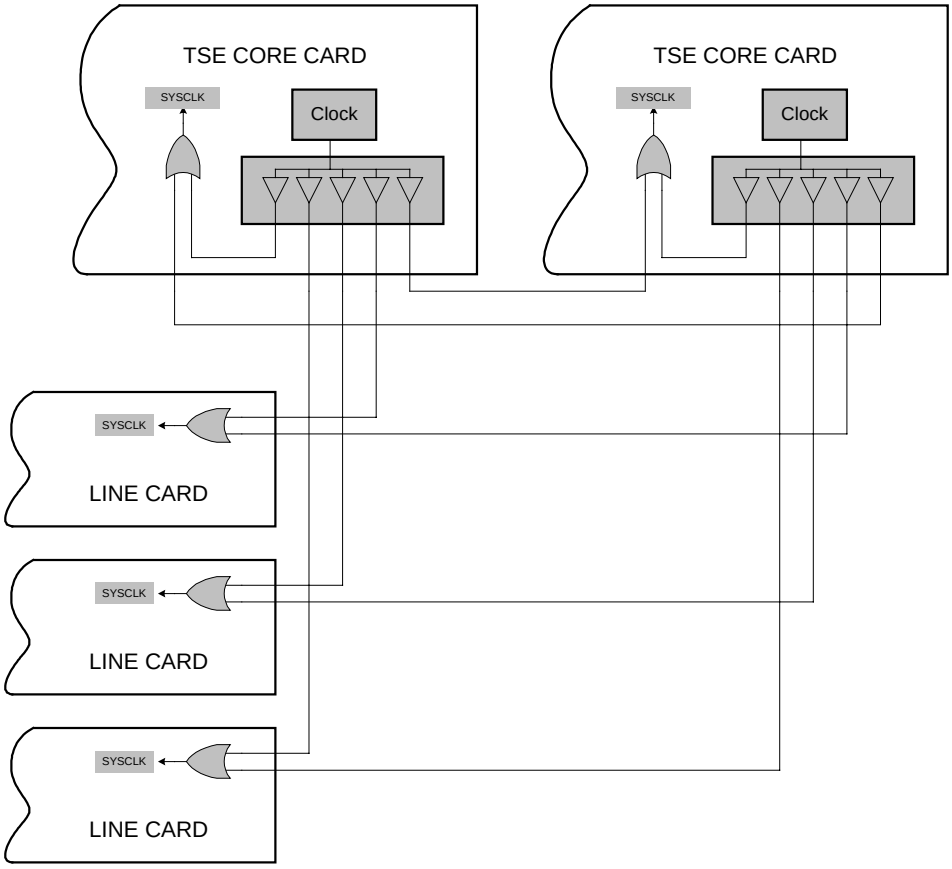
For the TSE Core Card not distributing timing to the backplane, SYSCLK is sampled from the backplane for TSE device timing and for redundant timing of FP. Alignment of the frame pulse (FP) counter between TSE Core Cards is accomplished similarly, as FP is always sampled from the backplane and used to reset the local frame pulse counter.

7.3 CHESS System Signals

7.3.1 SYSCLK Distribution

SYSCLK is distributed within the CHESS Reference Design cards as described in Figure 6. Only one SYSCLK source drives at one time (as described above in Figure 4), hence the OR gate selects the active clock source.

Figure 6 - SYSCLK Inter-Board Distribution



7.3.2 Frame Pulse (FP)

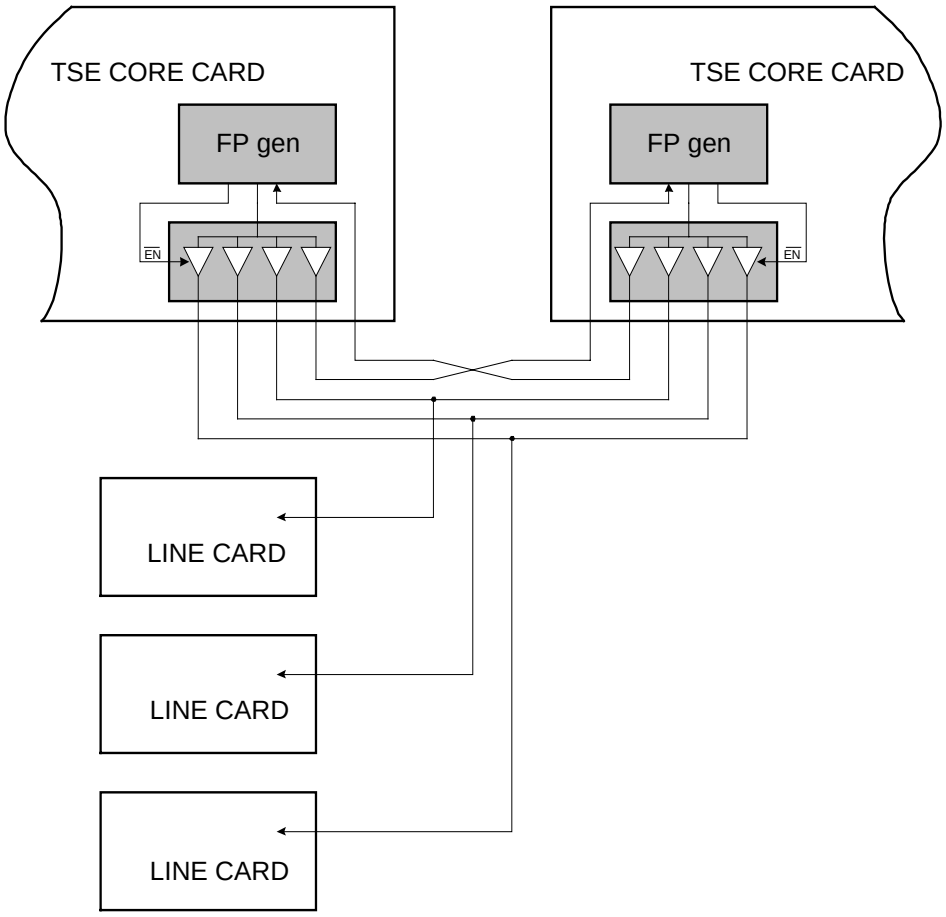
The frame pulse (FP) indicates the STS-12 frame boundaries at the J0 byte. This signal provides synchronization between all CHESS devices to ensure alignment of frames at space and time switch fabric interfaces. It is asserted high for a full SYSCLK period once every 9720 counts of SYSCLK (125µs). FP is not required at every frame as all CHESS devices maintain framing counts, but synchronization must occur at the initialization of operation. FP can be disabled by setting Configuration Register Bit 2 = 0 on both cards.

The OK signal is used to signal the update of XCMP and RWSEL at the end of each frame.

The CPLD is used for counting SYSCLK cycles for FP and for enabling the 49FCT3805 1:4 output driver used in its distribution.

Consult the CHESS User's Guide (PMC-1991797) for additional information on frame alignment and the system effects of the frame pulse.

Figure 7 - Frame Pulse (FP) Inter-board Distribution

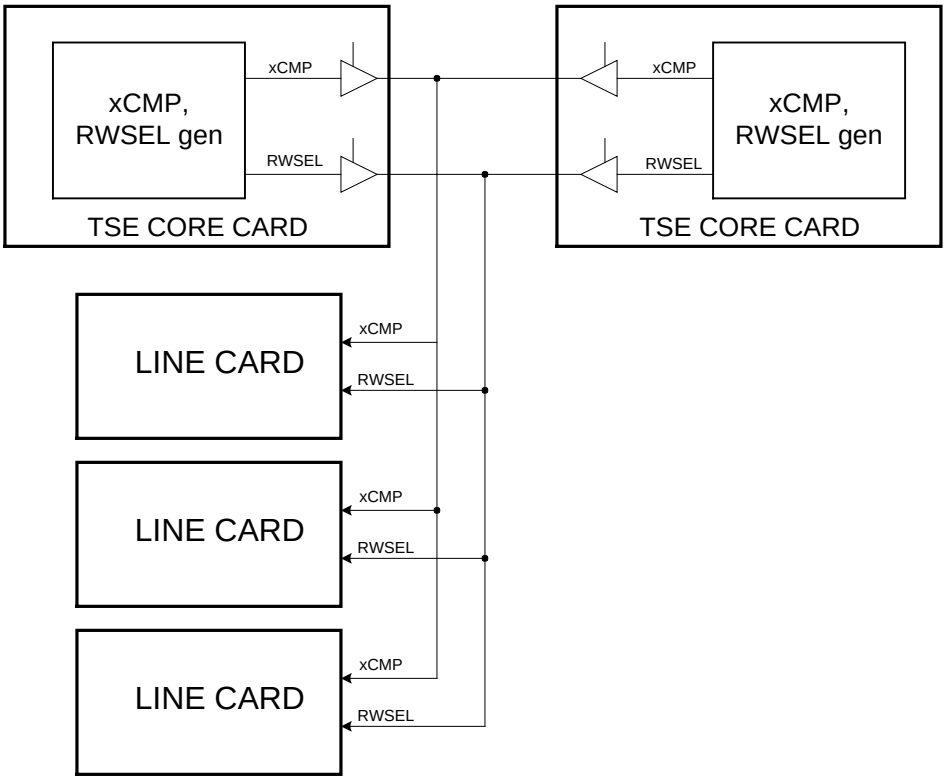


7.3.3 xCMP, RWSEL

The system host determines the CHESS system signals', xCMP and RWSEL, respective states. Each TSE Core Card generates identical versions but only one drives the backplane as set in Configuration Register Bit 3.

As xCMP and RWSEL are sampled at FP, changing their respective states is reserved until immediately before the frame pulse.

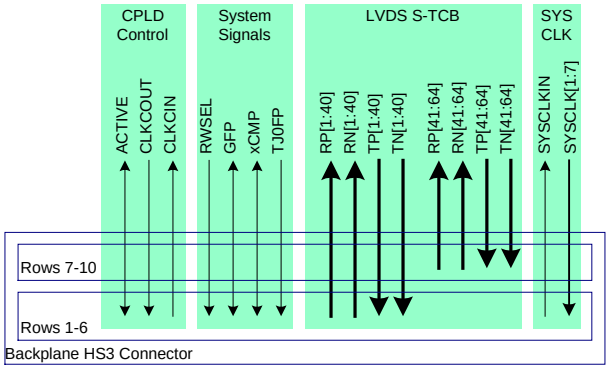
Figure 8 - xCMP and RWSEL Inter-board Distribution



7.4 System Interface

The S-TCB is an 777.6 Mb/s LVDS link. In a normal configuration, the TSE Core Card will connect through the S-TCB backplane to SONET/SDH framer cards with S-TCB interfaces (provided by the PM5315 TBS device). For multi-stage fabrics, one TSE Core Card (or device) would connect to another TSE Core Card (or device).

Figure 9 - Connection Map to Backplane



The separation of the backplane connection into Rows 7-10 and Rows 1-6 was made to enable the optional use of a 6 Row connector or a 10 Row connector. All non-LVDS backplane signaling resides within Rows 1-6, and Rows 7-10 contain only LVDS channels as described in Figure 9.

Note: the pin-out of the HS-3 connector in Table 4 labels the rows as letters (A, B, C,… with 1 being Row A) to be consistent with AMP documentation.

7.4.1 LVDS Termination

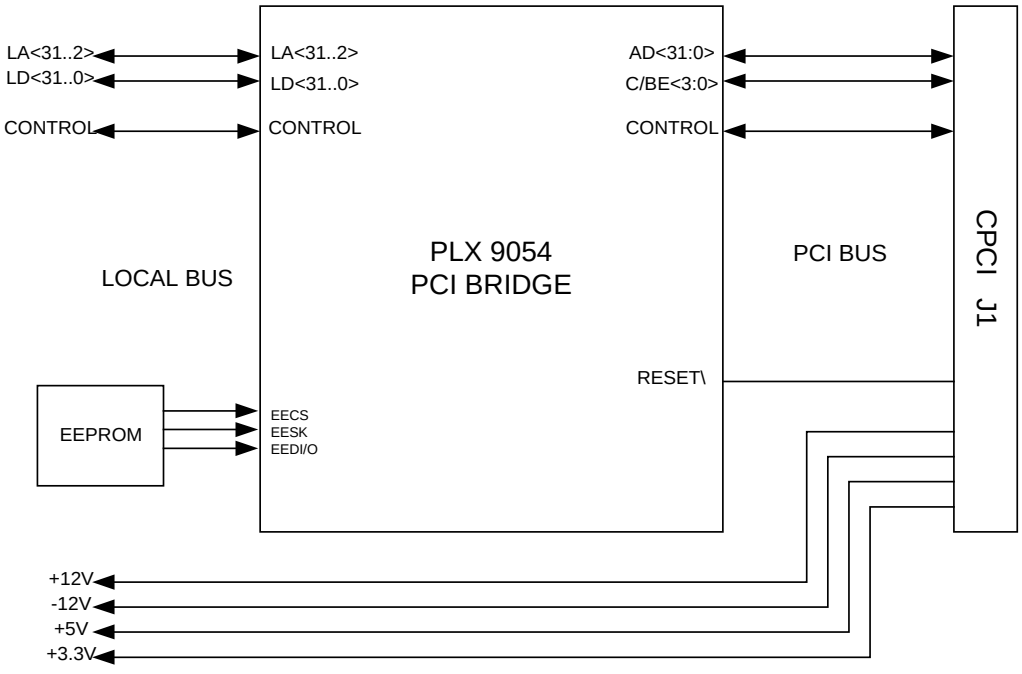
The LVDS receive signals RN/P[1..64] are terminated with 100 Ω internally to the TSE device. No additional termination is normally required.

7.5 Compact PCI Interface

The PM5372 TSE includes a microprocessor interface to provide read/write access to normal and test mode registers as described within the TSE Data Sheet. This design connects a CompactPCI bus to this microprocessor interface.

A block diagram of the cPCI interface and bridge is shown below in Figure 10.

Figure 10 - cPCI Block Diagram.



7.5.1 Interface and Bridge Hardware

The PCI9054 is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The 32 bit multiplexed address/data bus and associated control lines connect directly from the CPCI J1 connector to the PLC PCI9054 bridge device. The bus and control lines are terminated with 10 ohm stub resistance that should be placed close to the J1 connector pins.

For this reference design the PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. Address lines LA<31...2> provide 32-bit word addressing. The lower two bits of the address lines are used for 16 or 8 bit byte access but are unused in this application. The CPLD (Section 7.2.1) implements the local bus glue logic.

A serial EEPROM is required for device configuration after reset or upon power-up. PLX Technology recommends Fairchild Semiconductor the 93CSX6L family serial EEPROMs. The PCI9054 can also be configured by an on board microprocessor/controller if desired.

7.5.2 Hot Swap Features

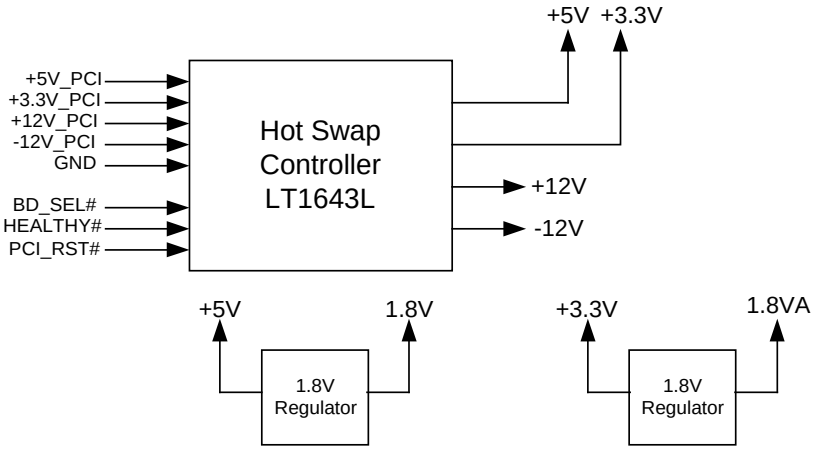
In addition to the local and PCI bus interfaces, the cPCI block provides some of the hardware required for hot swap. The hot swap specification outlines a hardware and software solution to allow cPCI boards to be safely plugged in or removed from an active PCI backplane. Note that this block does not provide the minimum Hot Swap requirements for safe insertion and extraction. An additional Hot Swap controller is required to safely power up and power down the board.

The cPCI block provides 1V precharge voltage to cPCI bus pins to reduce pin bounce during connection or removal. Most cPCI pins are pulled up to 1V with 4 other pins (RST#, ENUM#, INTA#, and REQ#) precharged to V(I/O) to provide a stable clock prior to bus contact.

The PCI9054 provides control circuitry for a blue hot swap LED placed on the front panel of the board. This LED is illuminated when it is safe to extract a board from the backplane. As the user presses the ejector switch to remove a board from the backplane, the LED indicates that system software has been placed in a safe state for extraction. There is no indication as to the hardware integrity. Upon insertion, the LED will remain illuminated until the hardware connection process completes. It will remain off until illuminated by software to indicate extraction is safe.

7.6 Power Supply

Figure 11 - Power Supply Board System Block.



The Power Block provides stable voltage supplies delivered over the CompactPCI backplane from a centralized power supply. Voltage levels of +5V, +3.3V, +12V, -12V and regulated 1.8V are available from this block.

Table 3 - TSE Core Card Power Consumption

PART	SUPPLY	CURRENT	QUANTITY	POWER
TSE	1.8 VDDI	3835mA	1	6903mW
TSE	1.8 AVDL	965mA	1	1824mW
1.8V WORST TOTAL		4800mA		8727mW
TSE	3.3	1298mA	1	4283mW
MC100LVEL14	3.3	40mA	2	264mA
MC100LVELT23	3.3	33mA	1	109mW
MC100LVELT22	3.3	33mA	1	109mW
49FCT3805	3.3	30mA	2	200mW
MB OSCILATOR	3.3	90mA	1	279mW

74ALVC125	3.3	50mA	1	165mW
XC9572XL	3.3	50mA	1	165mW
74HC244	3.3	60mA	1	198mW
SSF-LXH5174	3.3	80mA	2	528mW
PLX9054	3.3	200mA		660mW
3.3V WORST TOTAL		2109mA		6960mW

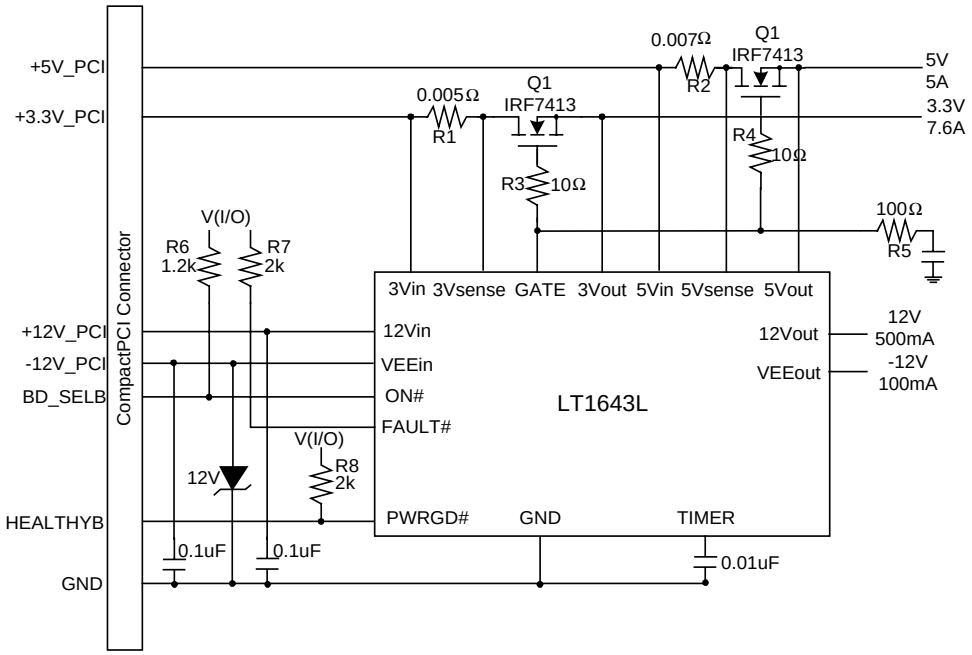
7.6.1 Voltage Regulators

Two voltage regulators supply the 1.8V digital and 1.8V analog pins of the TSE device - 1.8V is not used anywhere else on the board. The supply labelled 1.8V is used for core digital (VDDI) power and uses the 5V for VIN of the regulator. The supply labelled VCC1 is used for AVDL (1.8V analog) pins and uses the 3.3V for VIN. Both regulators are capable of providing up to 5A of supply current at 1.8V.

7.6.2 Hot Swap Controller

The Hot Swap Controller is used to allow a board to be safely inserted or removed from a live cPCI slot. External N-channel MOSFETS control the 3.3V and 5V supplies, while the +12V and –12V supplies are controlled with on-chip switches. The supply voltages are ramped up at a programmable rate. The hot swap controller is implemented using the Linear Technology LTC1643L. A typical cPCI Hot Swap circuit is shown below in Figure 2. Note that only the hot swap controller is implemented in the power block. Additional Hot Swap circuitry including the precharge circuitry for the cPCI bus is included in the CompactPCI block.

Figure 12 - cPCI Hot Swap Circuit



The 3.3V, 5V, +12V, and –12V power supplies are generated from the medium length power pins on the PCI connector (+5V_PCI, +3.3V_PCI, etc). The long power pins which make the first connections are used to generate a 1V precharge voltage on the cPCI bus pins.

In the circuit above, the 3.3V and 5V power supplies are controlled by the N-channel pass transistors Q1 and Q2. Internal circuitry controls the +/-12V rails. R1 and R2 control overcurrent conditions. R5 and C1 provide current control loop compensation. R3 and R4 prevent high frequency oscillations in the pass transistors. Finally, the 12V Zener diode protects against power surges on the –12V rail.

During an insertion and power-up sequence, the BD_SEL# pin is the final pin to connect to the board. This pin is connected to the ON# pin of the Hot Swap Controller. When the ON# pin is pulled low, the pass transistors are turned on by pulling the GATE pin high, and the current in each pass transistor rises at a rate of dv/dt = 50μA/C1, until reaching the preset limit. If there is a high load capacitance, the rate of increase will be controlled by this value. Once the supply voltages stabilize the PWRGD# signal is pulled low.

The current limit for the 5V and 3.3V supplies is set by the sense resistors R1 and R2 in Figure 12 above, and is governed by the following equation:

$$I_{\lim} = 53mV / R_{sense}$$

In the circuit shown above, the 3.3V current limit will be 10.6A, and the 5V limit will be 7.6A.

Upon removal, the /ON pin will be pulled high, and the GATE pin on the pass transistors is pulled low to prevent load currents on the 3.3V and 5V rails from instantaneously going to zero and glitching the power supply. The /PWRGD pin is pulled high if any of the supply voltages moves below its threshold.

Refer to the LT1643 datasheets for additional operation and applications information.

8 IMPLEMENTATION DESCRIPTION

8.1 Root Drawing

The root drawing shows the interconnections between the CPCI_BLOCK, CPLD_BLOCK, TSE_BLOCK, CLOCK_DISTRIBUTION, POWER_BLOCK and SYSTEM_INTERFACE.

8.2 TSE Block Sheets 2,3,4

Signalling for the TSE device is simple and no additional components are used for termination for LVDS – all pairs are internally differentially terminated with 100Ω. Care must be taken to ensure uninterrupted impedance while routing to the HS3 connector when routing the 128 LVDS paired lines to the connector.

All 1.8V supplies for the TSE device require 5% tolerance, while 3.3V supplies have 10% tolerance. Decoupling capacitors of 0.1µF are used for VDDO[1..36] pins at the four corners of the TSE device. Decoupling capacitors of 0.1µF are distributed around the device for all other supply pins. All decoupling capacitors should be positioned as close to the pins as possible to reduce series inductance.

Reference resistors of 3.16 kΩ ±1% are required for TSE analog stages on the RES and RESK pins. The JTAG port and the analog test buses are not accessed. TRSTB shares the device reset RSTB.

8.3 CPLD Block

Buffers have been added for additional current drive for high edge rates of SYSCLK_TSE and FP. Buffers are also present on xCMP and RWSEL to provide for the multidropped loads. To drive the 20mA LEDs, a 74HC244 device is used.

Programming of the XC9572XL device is provided for with the header connection to its JTAG port.

VCCIO and VCCINT are both connected to 3.3V and have been decoupled according to the manufacturers recommendations with 0.01µF and 0.1µF. Decoupling capacitors should be positioned as close to the pins as possible to reduce trace inductance.

A 49.9 Ω series termination resistor is used on the FP output of the 74ALVC125 device to control the effects of fast rise/fall times. The small output resistance of the CMOS driver and the terminating resistor should match the 50 Ω line and matching HS-3 connector. The extra connection after the terminating resistor adds to the load capacitance applied to the line beyond the backplane. xCMP and RWSEL are relatively slow moving signals and their traces do not act like transmission lines.

A 56Ω series termination resistor is used on the SYSCLK_TSE line to match the 65Ω traces used for on-board signalling.

8.3.1 VHDL Programming Code

The programming file for the Xilinx XC9572XL was designed using Xilinx WebPack tools in VHDL. Standard libraries provided with the software were used.

8.4 Clock Block

SYSCLK (77.76 MHz) is distributed using differential PECL signaling to minimize jitter and to maximize noise immunity. As well, backplane noise contributions are reduced with less signal swing compared to a TTL signal. This is accomplished using a 1:5 differential PECL clock driver. Four pairs continue to the backplane and one pair is used as a possible clock source (SYSCLK_IN1) for the TSE device. The second 100LVEL14 device is optional and provides an additional five SYSCLK PECL pairs for a total of nine connecting to the backplane. The scan clock (SCLK) input of the device is left open and ignored with SEL set low.

The FCT3807 device is used to distribute the additional SYSCLK_TTL to the CPLD and uses a 49.9 Ω series termination resistor at the driver. Series termination resistors outputs are used at the PECL-to-TTL converter outputs also.

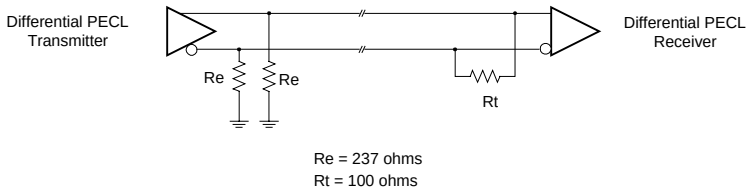
Decoupling capacitors accompany the power pins of each device and should be positioned close to the pin to reduce trace inductance. Termination is required for each differential PECL signal on the destination board, and all PECL lines have been made 50 Ω.

8.4.1 PECL Termination

SYSCLK<9..1> differential PECL pairs require termination resistors. Since a 50 ohm backplane and the HS-3 connector is a controlled 50 Ω a 100 ohm differential impedance results between the PECL pairs. A 100 ohm resistor

should be used at the clock receiver as close to the pins as allowed. Also, a bias resistor, Rpd, is required at the output for all PECL signals.

Figure 13 - PECL Termination for Clock Distribution



8.5 System Interface

As maximum signal density within the HS3 is required, optimal noise pin assignments could not be used. TTL switching signals like FP have been isolated from the LVDS signals to reduce single mode coupling. The pin assignments have followed a similar pattern to the TSE device with groupings of four pairs together.

Only LVDS signals are located in Rows G,H, J and K so a six row connector can be used optionally.

Table 4 - Pinout of Backplane Connection (J4,J5,J6)

J4	A	B	C	D	E	F	G	H	J	K
1	TN1	TP1	TN7	TP7	RN9	RP9	RN15	RP15	TN21	TP21
2	TN2	TP2	TN8	TP8	RN10	RP10	RN16	RP16	TN22	TP22
3	TN3	TP3	RN5	RP5	RN11	RP11	TN17	TP17	TN23	TP23
4	TN4	TP4	RN6	RP6	RN12	RP12	TN18	TP18	TN24	TP24
5	RN1	RP1	RN7	RP7	TN13	TP13	TN19	TP19	RN21	RP21

6	RN2	RP2	RN8	RP8	TN14	TP14	TN20	TP20	RN22	RP22
7	RN3	RP3	TN9	TP9	TN15	TP15	RN17	RP17	RN23	RP23
8	RN4	RP4	TN10	TP10	TN16	TP16	RN18	RP18	RN24	RP24
9	TN5	TP5	TN11	TP11	RN13	RP13	RN19	RP19	TN25	TP25
10	TN6	TP6	TN12	TP12	RN14	RP14	RN20	RP20	TN26	TP26
J5	A	B	C	D	E	F	G	H	J	K
1	TN27	TP27	TN33	TP33	RN33	RP33	RN39	RP39	TN47	TP47
2	TN28	TP28	TN34	TP34	RN34	RP34	RN40	RP40	TN48	TP48
3	TN29	TP29	RN29	RP29	RN35	RP35	TN43	TP43	TN49	TP49
4	TN30	TP30	RN30	RP30	RN36	RP36	TN44	TP44	TN50	TP50
5	RN25	RP25	RN31	RP31	TN39	TP39	TN45	TP45	RN45	RP45
6	RN26	RP26	RN32	RP32	TN40	TP40	TN46	TP46	RN46	RP46
7	RN27	RP27	TN35	TP35	TN41	TP41	RN41	RP41	RN47	RP47
8	RN28	RP28	TN36	TP36	TN42	TP42	RN42	RP42	RN48	RP48
9	TN31	TP31	TN37	TP37	RN37	RP37	RN43	RP43	RN49	RP49
10	TN32	TP32	TN38	TP38	RN38	RP38	RN44	RP44	RN50	RP50
J6	A	B	C	D	E	F	G	H	J	K
1	TN51	TP51	RN51	RP51	TN55	TP55	RN55	RP55	RN59	RP59
2	TN52	TP52	RN52	RP52	TN56	TP56	RN56	RP56	RN60	RP60

3	TN53	TP53	RN53	RP53	TN57	TP57	RN57	RP57	TN63	TP63
4	TN54	TP54	RN54	RP54	TN58	TP58	RN58	RP58	TN64	TP64
5	SYSCLKN1	SYSCLKP1	SYSCLKN5	SYSCLKP5	SYSCLKN8	SYSCLKP8	TN59	TP59	RN61	RP61
6	SYSCLKN2	SYSCLKP2	SYSCLKN6	SYSCLKP6	SYSCLKN9	SYSCLKP9	TN60	TP60	RN62	RP62
7	SYSCLKN3	SYSCLKP3	SYSCLKN7	SYSCLKP7	SYSCLKN_IN	SYSCLKP_IN	TN61	TP61	RN63	RP63
8	SYSCLKN4	SYSCLKP4	GND	GND	GND	FP_IN	TN62	TP62	RN64	RP64
9	GND	RWSEL	xCMP	FP1	FP2	FP3	GND	GND	GND	GND
10	GND	TJOFP	SDEN	SDENOUT	ACTIVE	FP4	GND	GND	GND	GND

8.6 Compact PCI Block

8.6.1 Layout Considerations

The Compact PCI specification outlines a number of layout requirements for the cPCI design. These include:

- All 10 ohm stub termination resistors must be placed within 0.6” of the J1 pins.
- All PCI signal traces must be less than 1.5” except P_CLK.
- P_CLK trace must be 2.5” +/- 0.1”
- CPCI bus traces impedance is 65 Ω.
- 39 ohm stub resistor on REQ# should be placed near its source on the PCI9054.

8.7 Power Block

All 3.3V power requirements for the board are sourced directly from the hot swap control circuitry. The 3.3V requirements are minimal for the TSE device, but all non-PMC devices use the 3.3V supply. A switching regulator module is used to provide the 1.8V supply at high efficiency for digital pins of the TSE device. A 182 Ω resistor on its output draws a stabilizing 10 mA current in all conditions. An additional 1.8V supply using a linear regular has been created for the 1.8V analog pins of the TSE device. To minimize power consumption the regulator uses the 3.3V rail. The output voltage of the 1.8V linear regulator is set by the following formula: $V_{OUT} = V_{REF} (1 + R_2/R_1) + I_{adj}R_2$.

9 SCHEMATICS

10 BILL OF MATERIALS

Table 5 - Bill of Materials

NO.	Part Name - Value	Part Number	Ref Des	Description	Qty
1	1N4148		D7		1
2	74ALVC125_SOIC14 -BAS E-VCC=3.3V	IDT74ALVC125DC	U14	IC 3V3 CMOS QUAD BUS BUFFER GATE W/ 3STATE OUTPUTS	1
3	AMP_HS3_10X10_F EMALE _RA-BASE	97-8159-07	J2, J4, J5	Z-PACK 10 ROW RA HS3 BACKPLANE FEMALE CONNECTOR	3
4	CAPACITOR-0.01UF, 50V, X7R_603	DIGIKEY PCC103BVCT-ND	C74, C81, C83, C85, C87, C89, C91, C93		8
5	CAPACITOR-0.1UF, 16V, X7R_603	PANASONIC -- ECJ-1VB1C104K	C26-C73, C75-C80, C82, C84, C86, C88, C90, C92, C97-C101	MULTILAYER CERAMIC CHIP CAPACITOR X7R 0603 0.1UF 16V	65
6	CAPACITOR-100UF, 10V, ELECTRO	DIGI-KEY -- P1211-ND	C96	PANASONIC HFS RADIAL AL.	1
7	CAPACITOR-10UF, 16V, TANT TEH	DIGI-KEY -- PCT3106CT-ND	C95	PANASONIC TEH TANT. CAP.	1
8	CAPS-0.01UF, 50V, X7R_603	ECU-V1H103KBV	C7, C19	CAP CERAMIC X7R 0603 50V 0.01UF	2
9	CAPS-0.047UF, 50V, X7R_1206	ECU-V1H473KBW	C8	CAP CERAMIC X7R 1206 50V 0.047UF	1
10	CAPS-0.1UF, 16V, X7R_603	ECJ-1VB1C104K	C9, C12-C17	CAP CERAMIC X7R 0603 16V 0.1UF	7
11	CAPS-0.1UF, 50V, X7R_1206	ECU-V1H104KBW	C5, C6, C10, C11, C18, C20	CAP CERAMIC X7R 1206 50V 0.1UF	6
12	CAPS-10UF, 16V, TANCAPC	ECS-H1CC106R	C23, C25	CAP TANCAPC 16V 20% 10UF	2
13	CAPS-10UF, 25V, TANCAPD	ECS-H1ED106R	C21, C22, C24, C94	CAP TANCAPD 25V 20% 10UF	4
14	CAPS-2.2UF, 35V, TANCAPC	ECS-H1VC225R	C2, C3	CAP TANCAPC 35V 20% 2.2UF	2

15	CAPS-220UF, 50V, ELECTRO HFS	ECE-A1HFS221	C1, C4	CAP ELECTRO VA SMD 50V 20% 220UF	2
16	CON_MICTOR_38PIN_2-7 67004-2-BAA	2-767004-2	J7, J8	38 PIN SIGNAL CONNECTOR, MATCHED IMPEDANCE, 0.025, SMD	2
17	CPCI_ESD_STRIP_BOTTO M_EDGE-BASE	PART OF PCB	P1	COMPACT PCI ESD STRIP, CREATE ON PCB LAYOUT	1
18	HEADER6_100MIL-BASE	PZC36SAAN	J10	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	1
19	HEADER_3A_100 MIL-BASE	DIGI-KEY S1011-36-ND	J9	100 MIL SPACING HEADER	1
20	HEADER_4X2_SMT_2MM-B ASE	87267-0850	J3	HEADER 2X4 SMT 2MM MALE	1
21	IRF7413		Q1, Q2		2
22	LED-CLEAR GREEN, LED_5MM VERT PA	DIGIKEY -- LT1132-ND	D2-D4, D6	T-1 3/4 LED CLEAR GREEN VERTICAL PCB MOUNT	4
23	LED-YELLOW, PCB .29 RIGHT ANGLE	DIGI-KEY -- L20367-ND	D8	.29" TALL RIGHT ANGLE PCB MOUNT	1
24	LT1084CM_SMT_REG-BAS E	LT1084CM	U19	5.0A LOW DROPOUT POSITIVE ADJUSTABLE REGULATORS	1
25	LT1117_SOT-ADJ	LT1117CST	U5	ADJUSTABLE REGULATOR	1
26	LTC1643L_SSOP-BASE	LTC1643LCGN	U2	CPCI HOT SWAP CONTROLLER	1
27	MAX811T_SOT143-BASE	MAX811T	U16	4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 3.08V SOT143	1
28	MAX812R_SOT143-BASE	MAX812R	U3	4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 2.63V SOT143	1
29	MB3100H-77.76MHZ, 100PPM	MB3100H-77.76MHZ	Y1	OSC HCMOS/TTL HALF SIZE 8 PIN 77.76MHZ 100PPM	1
30	MC100LVEL14_SOIC-BAS E	MC100LVEL14DW	U10, U11	IC LOW SKEW 1:5 CLOCK DISTRIBUTION CHIP SO20WB	2

31	MC100LVELT22D_SOIC8- BASE	MC100LVELT22D	U9	IC DUAL DIFFERENTIAL LVPECL TO TTL TRANSLATOR SOIC8	1
32	MC100LVELT23D_SOIC8- BASE	MC100LVELT23D	U12	IC DUAL DIFFERENTIAL LVPECL TO TTL TRANSLATOR SOIC8	1
33	MC74HC244ADW_SO20WB- BASE-VCC=3A	MC74HC244ADW	U18	IC OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER SO20WB	1
34	MOUNTING_HOLE_150MIL -BASE	MOUNTING HOLE	M1	MOUNTING HOLE .150" DIA	1
35	NM93CS46_DIP8_SOCKET -BASE	NM93CS46EN	U1	1K-BIT SER EEPROM W/ DATA PROTECT AND SEQ READ DIP8	1
36	PBNO_VERT_6MM-BASE	DIGIKEY -- P8009S-ND	SW1	VERT PCB MOUNT SPST PUSH BUTTOM	1
37	PCI9054_PQFP-BASE	PCI9054-AA50PI	U4	PCI I/O ACCELERATOR	1
38	PI49FCT3805_QSOP20-S PEED GRADEA	PI49FCT3805CQ20	U8, U13	IC 3.3V 2X1:5 CMOS CLOCK DRIVER QSOP20	2
39	RES-0, 5%, 603	ERJ-3GSY0R00V	R31	RES 0603 1/16W 5% ZERO OHM	1
40	RES-1.2K, 5%, 603	ERJ-3GSYJ122V	R2	RES 0603 1/16W 5% 1.2K OHM	1
41	RES-10, 5%, 603	ERJ-3GSYJ100V	R6, R8	RES 0603 1/16W 5% 10 OHM	2
42	RES-100, 1%, 603	ERJ-3EKF1000V	R9	RES 0603 1/16W 1% 100 OHM	1
43	RES-100K, 5%, 603	ERJ-3GSYJ104V	R24	RES 0603 1/16W 5% 100K OHM	1
44	RES-10M, 5%, 805	ERJ=6GEYJ106V	R26-R28	RES 0805 1/10W 5% 10M OHM	3
45	RES-130, 1%, 603	ERJ-3EKF1300V	R22	RES 0603 1/16W 1% 130 OHM	1
46	RES-182, 1%, 603	ERJ-3EKF1820V	R1	RES 0603 1/16W 1% 182 OHM	1
47	RES-2.0K, 5%, 603	ERJ-3GSYJ202V	R3, R4	RES 0603 1/16W 5% 2.0K OHM	2
48	RES-200, 5%, 603	ERJ-3GSYJ201V	R10-R13	RES 0603 1/16W 5% 200 OHM	4

49	RES-24, 5%, 805	ERJ-6GEYJ240V	R21	RES 0805 1/10W 5% 24 OHM	1
50	RES-270, 5%, 603	ERJ-3GSYJ271V	R25	RES 0603 1/16W 5% 270 OHM	1
51	RES-39.2, 1%, 805	ERJ-6ENF39R2V	R16	RES 0805 1/10W 1% 39.2 OHM	1
52	RES-4.75K, 1%, 603	ERJ-3EKF4751V	R14, R17-R20	RES 0603 1/16W 1% 4.75K OHM	5
53	RES-4.7K, 5%, 603	ERJ-3GSYJ472V	R7, R29, R48	RES 0603 1/16W 5% 4.7K OHM	3
54	RES-47.5, 1%, 805	ERJ-6ENF47R5V	R23	RES 0805 1/10W 1% 47.5 OHM	1
55	RESISTOR-.01, 1%, 1206	IRC-TT LRC-LR1206-01-R01 0-F	R15		1
56	RESISTOR-0.005, 5%, 603		R5		1
57	RESISTOR-100, 1%, 603		R44, R45, R56, R57		4
58	RESISTOR-100, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND	R50		1
59	RESISTOR-237, 1%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R38-R41, R52-R55, R58-R73		24
60	RESISTOR-3.16K, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND	R32-R35		4
61	RESISTOR-3.3, 1%, 805	DIGI-KEY -- P<VALUE>DCT-ND	R36		1
62	RESISTOR-4.7K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R42, R43		2
63	RESISTOR-44.2, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND	R30		1
64	RESISTOR-49.9, 1%, 603		R37, R46, R47, R51, R74-R76		7
65	RESISTOR-56.2, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND	R49		1
66	RES_ARRAY_4_SMD-10	DIGI-KEY -- Y4<VALUE CODE>-ND	RN7-RN14, RN17-RN21		13
67	RES_ARRAY_4_SMD-10K	DIGI-KEY -- Y4<VALUE CODE>-ND	RN22-RN34		13
68	RES_ARRAY_4_SMD-150	DIGI-KEY -- Y4<VALUE CODE>-	RN36		1

		ND			
69	RES_ARRAY_4_SMD-1K	DIGI-KEY -- Y4<VALUE CODE>-ND	RN6, RN15		2
70	RES_ARRAY_4_SMD-4.7K	DIGI-KEY -- Y4<VALUE CODE>-ND	RN1-RN5, RN16, RN35		7
71	SIE501-8_SIE-BASE	SIE501.8R	U17	NON-ISOLATED BUCK CONVERTER	1
72	SSF_LXH5147-LGD	SSF-LXH5147LGD	D5	QUAD GREEN LED.	1
73	TEST_POINT_2_PAD50CI R32D-BASE		TP7, TP8	TEST POINT THRU-HOLE PAD50CIR32D	2
74	TEST_POINT_2_PAD60CI R36D-BASE		TP3-TP6, TP9-TP18	TEST POINT THRU-HOLE PAD60CIR36D	14
75	TSE_UBGA560-BASE		U6, U7		2
76	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP1, TP2		2
77	XC9572XL-TQ100-10NS	XC9572XL-10TQ100I	U15	CPLD 3.3V 10NS	1
78	ZENERDIODE-12.0V_1W	DIGI-KEY ZM4742ACT-ND	D1		1
79	ZPACK5X22FH_ASCPCI_2 MM	352068-1	J1	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	1

NOTES

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