PM7390

S/UNI-MACH48

REFERENCE DESIGN

ISSUE 2:FEBRUARY 2001

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	May 2000	Document created
2	Feb 2001	Section 6: Modify block diagram to reflect actual layout Section 7.1.4: Include recommendation to use series source termination resistors based on simulation graph. Section 7.2.3: Added FPGA UL3/PL3 timing section. Added note on FPGA selection Section 7.2.8: Updated FPGA Register Descriptions Section 8.2.3: Added HS3 Pinout Section 13: Remove EEPROM code table.
2		**Update schematics.** Page 2: Added 44.736 MHz clock to DS3TICLK pin, which is required for DS3 applications. Page 6: Add PLX_EN output from FPGA to control PCI9054 reset state. This allows code to download from SPROM prior to PCI9054 coming out of reset. Page 7: Change clocking of TFCLK to run directly from buffer and not from FPGA. This eliminates unnecessary delay in the clock line.

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1 DEFINITIONS

APS	Automatic Protection Switching
ATM	Asynchronous Transfer Mode
CPCI	Compact PCI. An adapted specification from the Peripheral Component Interconnect (PCI) Specification 2.1 or later.
FPGA	Field Programmable Gate Array
LVDS	Low Voltage Differential Signal
POS	Packet Over SONET
PRBS	Pseudo Random Bit Sequence
S-TCB	Serial Telecombus
UL3/PL3	UTOPIA Level 3/POS-PHY Level 3

2 FEATURES

The S/UNI-MACH48 reference design represents only a subset of the MACH48's functional capabilities. The following features are supported in this reference design:

- 777.6 Mbps LVDS Serial Telecombus
- User selectable between Utopia Level 3 and the POS-PHY Level 3 interface
- An on board FPGA that allows the user to loopback the UL3/PL3 for testing and evaluation.
- A CompactPCI interface that allows the user to control and monitor the MACH48 and on board FPGA.
- The ability to switch between an on-board system clock (77.76 MHz) for standalone testing and an off-board clock for system integration.
- Selection of either Working or Protect Serial Telecombus (S-TCB) link data.
- User selectable Time Slot Interchange blocks for input and output.
- User selectable UL3/PL3 interface clock (100MHz) from on-board (master) or off-board (slave). source

3 APPLICATIONS

- Channelized Router/ATM Switch Port Card
- Multi-service ADMs and Switches

4 REFERENCES

1. ATM Forum, ATM User Network Interface Specification, V3.1, September 1994.
2. PMC-1990823, S/UNI MACH48 Data Sheet Issue 2, December 1999.
3. 1030-54000-DTB, PCI 9054 Data Book Version 1.0, November 1998
4. AF-PHY-0136.000, ATM Forum, Utopia 3 Physical Layer Interface, V1.0, November 1999.
5. PICMG 2.0 CompactPCI Specification, R2.1, September 1997.
6. PMC-1991797, CHESS Users Guide, Issue 2, May 2000.
7. PMC-2000299, 777.6 MHz LVDS Serial Telecombus Design Considerations, Issue 1, March 2000.
8. PMC-1980495, POS-PHY Level 3, Issue 4, April 2000.
9. PMC-2000021, CHESS Reference Design Hardware Manual, Dec 2000.
10. Johnson, Howard, “High Speed Digital Design: A Handbook of Black Magic”, Prentice Hall, 1993.

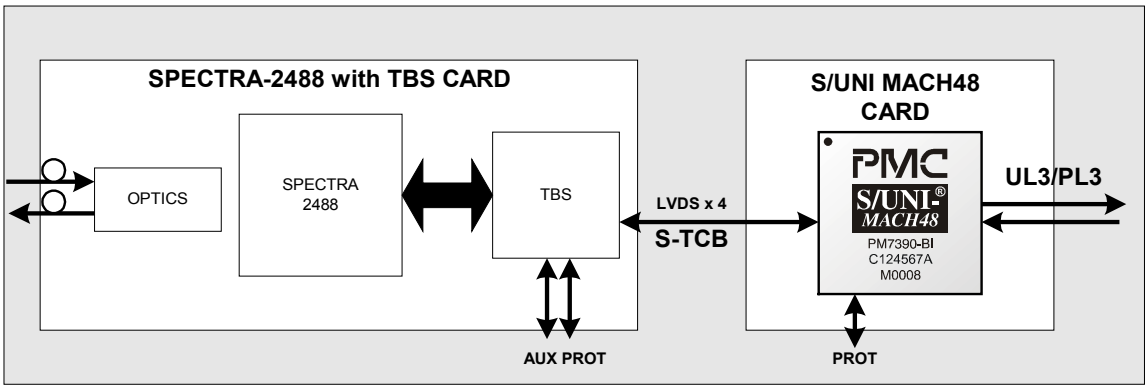
5 APPLICATION EXAMPLES

The S/UNI-MACH48 is one component in PMC-Sierra's CHESS (CHannelized Engine for SONET/SDH) family of high speed network devices. The following are but a few examples of how the S/UNI MACH48 reference design can be used.

5.1 Channelized Router/ATM Switch Port Card

The S/UNI MACH48 Reference Design can be used to implement a multi-service port card configuration as seen in Figure 1. SONET traffic is transferred via the OC-48 optical interface of the SPECTRA-TBS card. On the ingress, payload is extracted and passed to the TBS where the data is serialized and passed to the S/UNI MACH48. The S/UNI MACH48 will perform cell/packet delineation. On the egress, the S/UNI MACH48 performs cell/packet insertion. The TBS then de-serializes the data and transfers it to the SPECTRA for insertion into a SONET frame. The auxiliary and protection data streams can be used for protection switching redundancy.

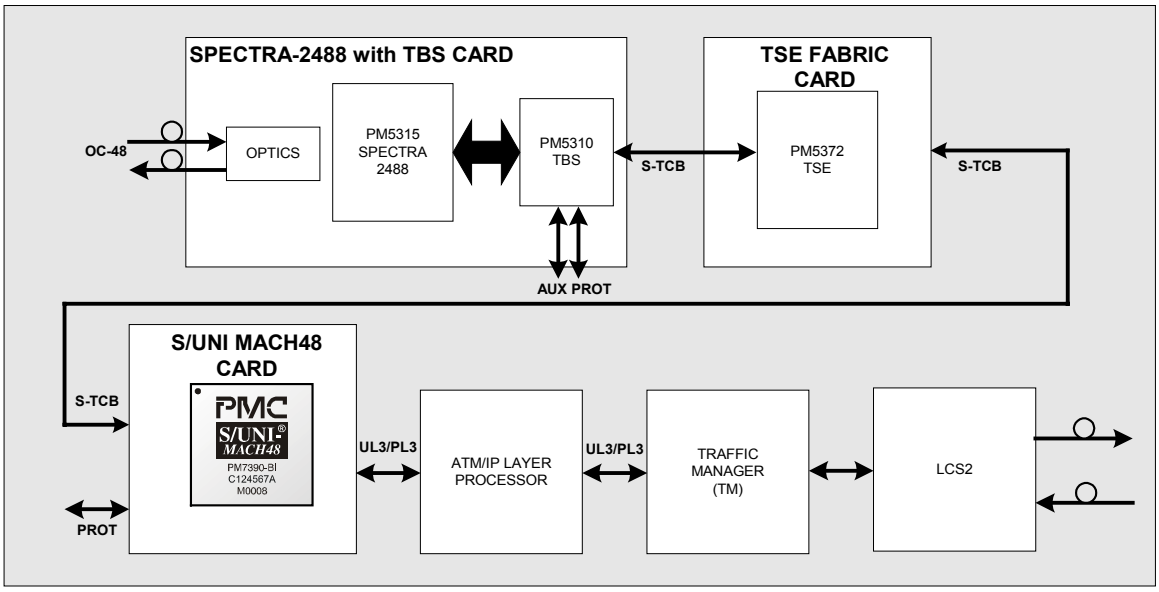
Figure 1 -Router/ATM Switch Port Card



5.2 Multi-service ADMs and Switches

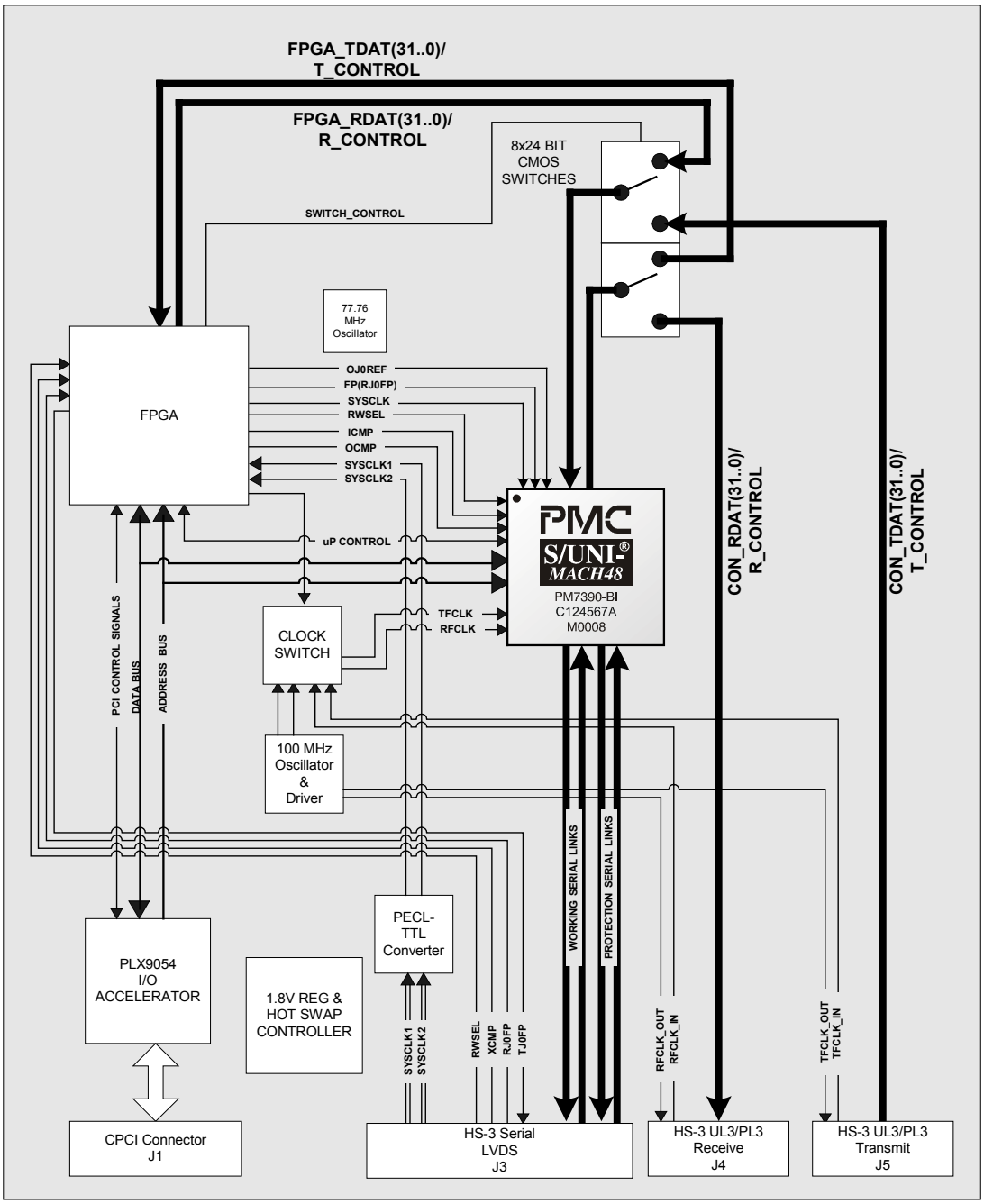
Figure 2 below illustrates a multi-service switch. This example shows only one part of a larger switch. In practice the TSE core card would consist of multiple TSE devices that would comprise a large switch core. Multiple SPECTRA-TBS line cards would also be used to create a protection switching architecture.

Figure 2 Multi-Service Switch using S/UNI MACH48 Device



6 BLOCK DIAGRAM

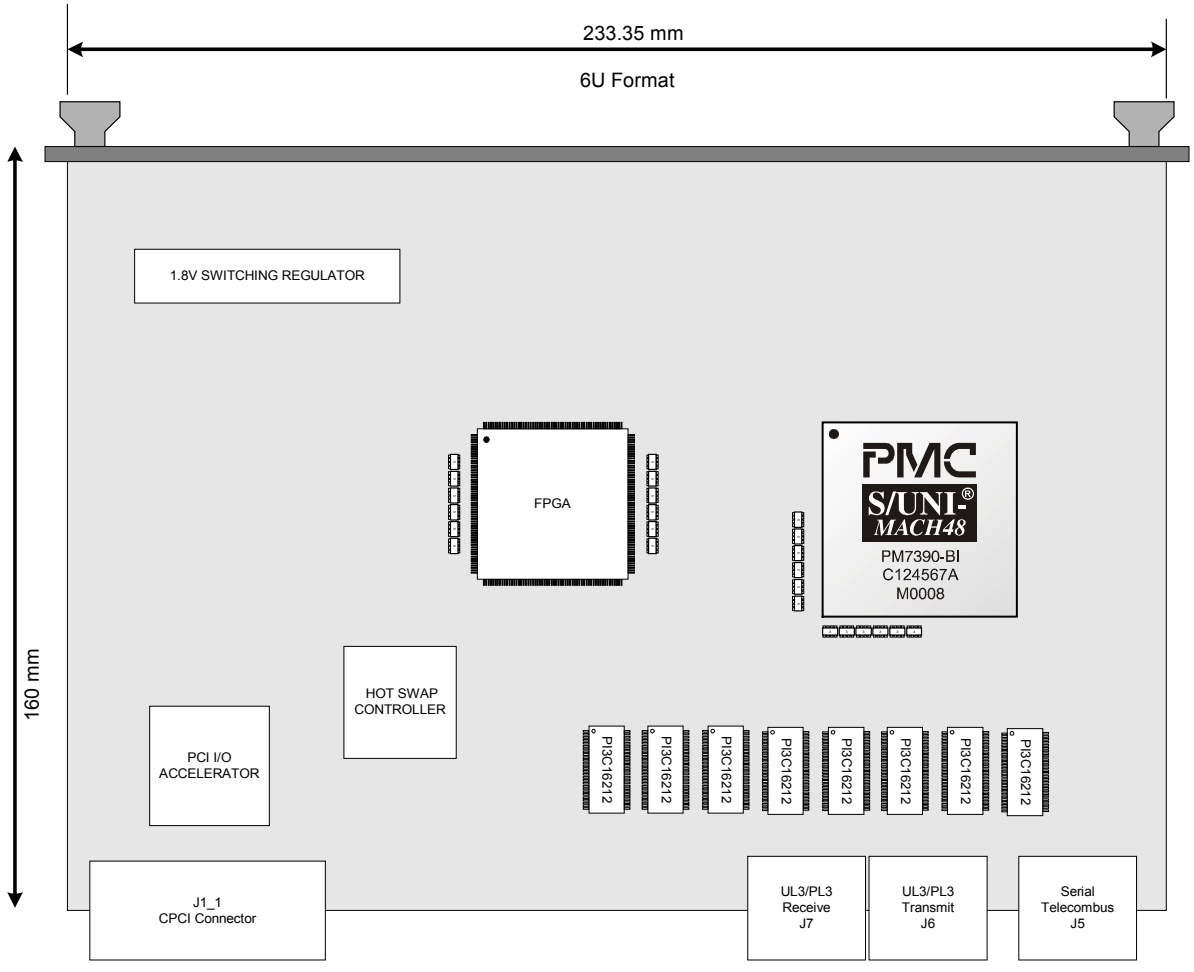
Figure 3 - S/UNI MACH48 Reference Design Block Diagram



7 FUNCTIONAL DESCRIPTION

This reference design is a 6U CompactPCI form factor board designed to demonstrate the features of the S/UNI-MACH48 Multi Service Access Device for CHannelized Interfaces. The board consists of a S/UNI MACH48 device, a FPGA for loopback, and a PCI bridge controller to interface with the PCI bus. There are connectors for interfacing to a CPCI backplane and a custom backplane.

Figure 4 - Board Layout of S/UNI MACH48 Reference Design



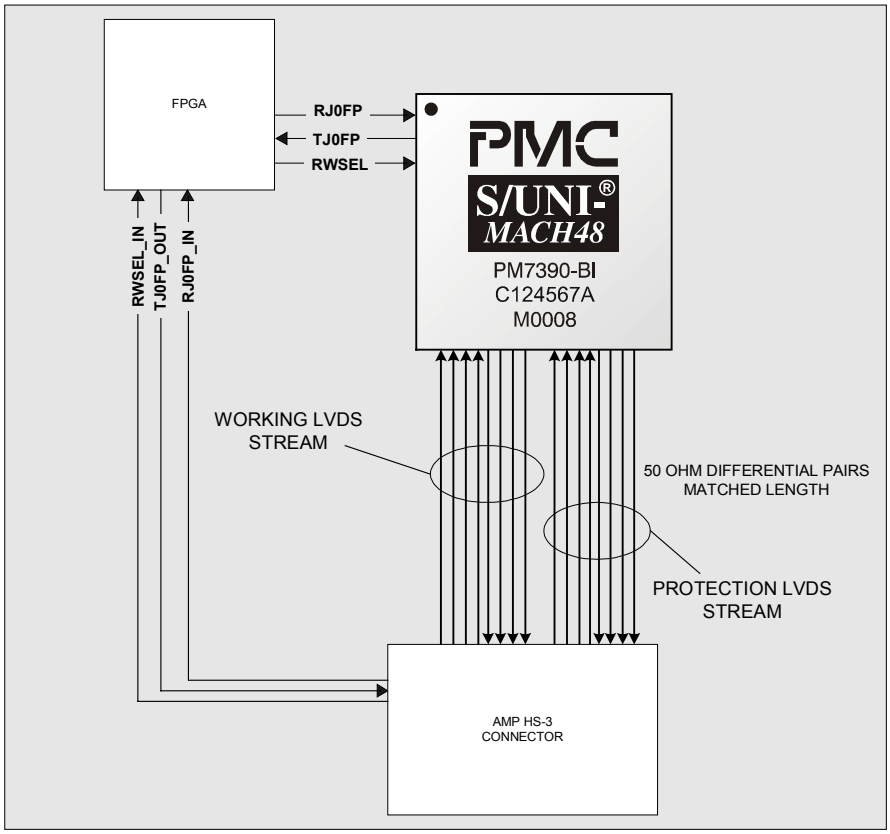
7.1 S/UNI MACH48

7.1.1 777.6 Mbps LVDS Serial Telecombus

The S/UNI-MACH48 has 2 sets of 8 serial LVDS data pairs (4 transmit, 4 receive) that operate at 777.6 Mbps. This rate is required for the 8B/10B encoding used to transfer data on each link at OC-12 rates (10/8 x 622.08 Mbps = 777.6 Mbps). One set of data links is the working data stream and the other is used as the protection data stream. The protection data stream is part of the Protection system architecture used

RWSEL will select whether the working or protection ingress LVDS streams are processed. During normal operation, RWSEL will be controlled by the host system. However, the RWSEL signal can be modified at any time via the microprocessor interface. This will be explained in more detail below.

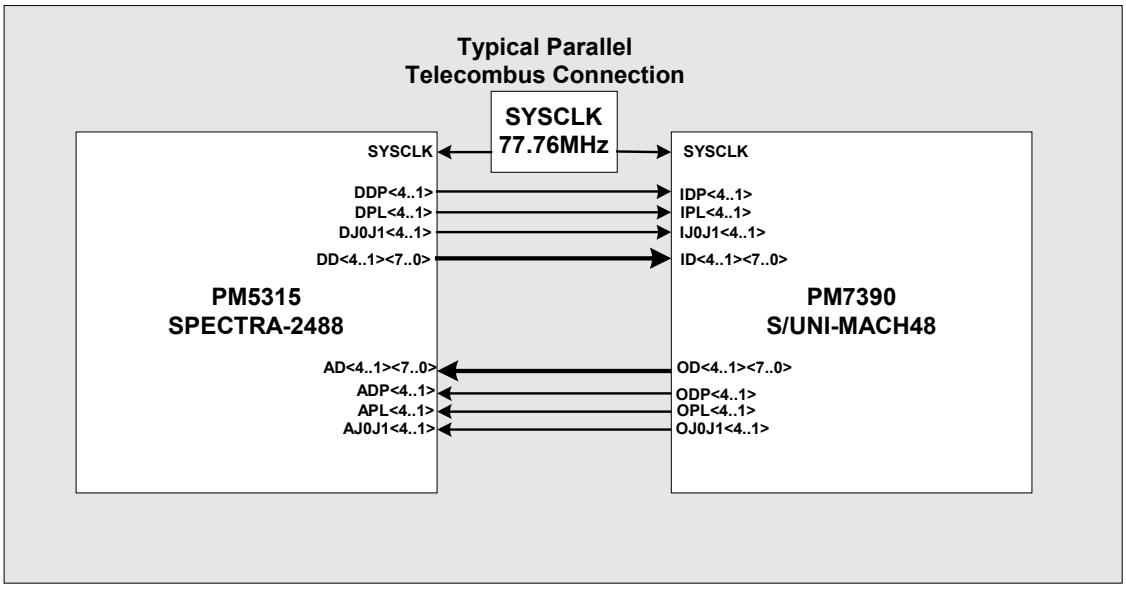
Figure 5 - S/UNI MACH48 Serial LVDS Layout



7.1.2 Parallel Telecombus Interface

The parallel telecombus is not used in the S/UNI MACH48 reference design but its application is illustrated below. The diagram shows a PM5315 SPECTRA-2488 interfacing to a S/UNI MACH48 via the parallel telecombus. This is a point to point connection that is clocked at 77.76 MHz.

Figure 6 - Typical Parallel Telecombus Interface



7.1.3 Time Slot Interchange

The S/UNI MACH48 has the ability to rearrange system side and line side SONET/SDH timeslots. Both the ingress and egress buffer 48 timeslots and rearrange them as desired before outputting them. This feature allows the user to configure timeslot mappings, bypass timeslots, and use predefined mappings for standard Telecombus interfaces.

The S/UNI-MACH48 can channelize data streams from STS-48/STM-16 down to STS-1/STM-0/DS3 granularity for a total aggregate bandwidth of 2.488 Gbps (1 STS-48/STM-16 stream).

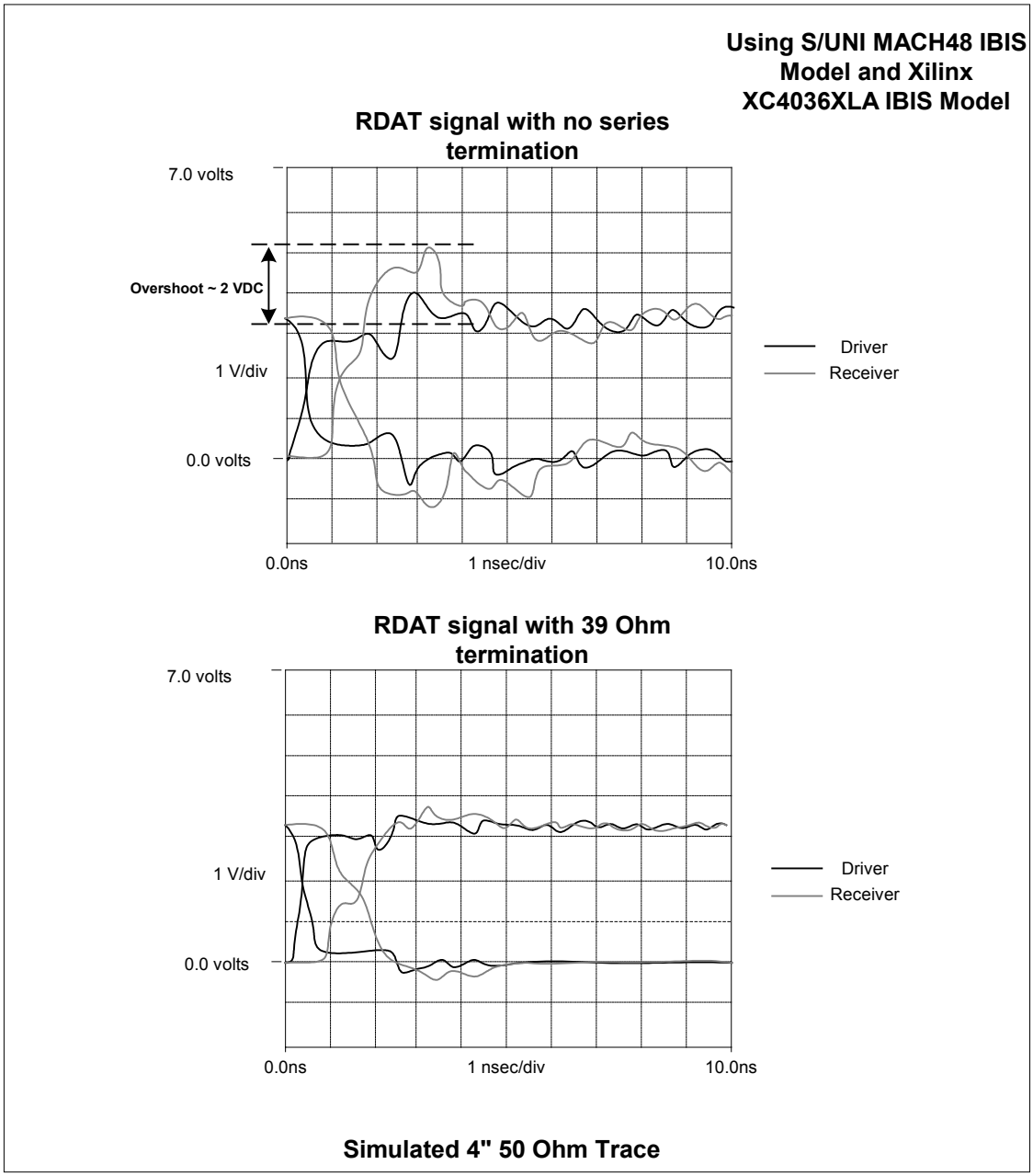
The S/UNI MACH48 reference design makes use of the TSI feature to simplify the PCB layout by re-mapping links in order to avoid crossovers.

For a complete list of legal channel mappings, consult the S/UNI MACH48 Data Sheet (Reference 2).

7.1.4 UL3/PL3 Interface

The S/UNI MACH48 implements a 32 bit ATM Forum specified UTOPIA Level 3 and POS-PHY Level 3 interface. The S/UNI MACH48 can be set to use either interface protocol. The UL3/PL3 interface can be clocked up to 104MHz. The reference design uses a 100MHz clock that can be selected from either the on-board source or from an off-board source. The line to system interface (RDAT) uses series source termination resistors to damp the driving signal. Figure 7, below, shows a Hyperlynx simulation using the IBIS models for the S/UNI MACH48 and the XC4036XLA. The simulation is based on a 4" long trace with 50Ω impedance. The value of the terminating resistor is 39 ohms. When not using a series termination, the receiver is subject to overshoot. Designers that do not intend to use termination resistors must ensure that the receiving device can tolerate the expected overshoot. It is recommended that a series source termination be used to reduce overshoot and improve signal integrity.

Figure 7 - Hyperlynx Simulations on 4” 50 Ω Trace

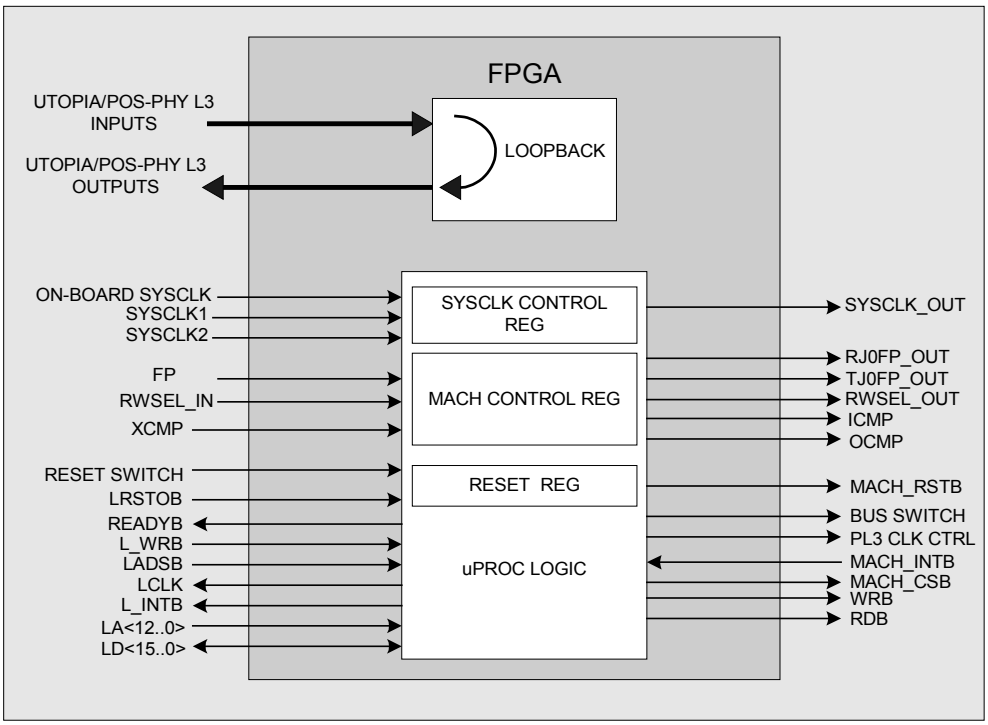


7.2 FPGA

A Xilinx XC4036XLA FPGA performs several functions. These include:

- System Clock (77.76MHz) source selection
- Wire loopback on UTOPIA/POS-PHY Level 3 bus
- UTOPIA/POS-PHY L3 source/destination select
- UTOPIA/POS-PHY L3 clock (100MHz) source select
- Working/Protection Link select
- Input/Output Connection Memory Page select
- PCI to MACH control glue logic
- Reset control

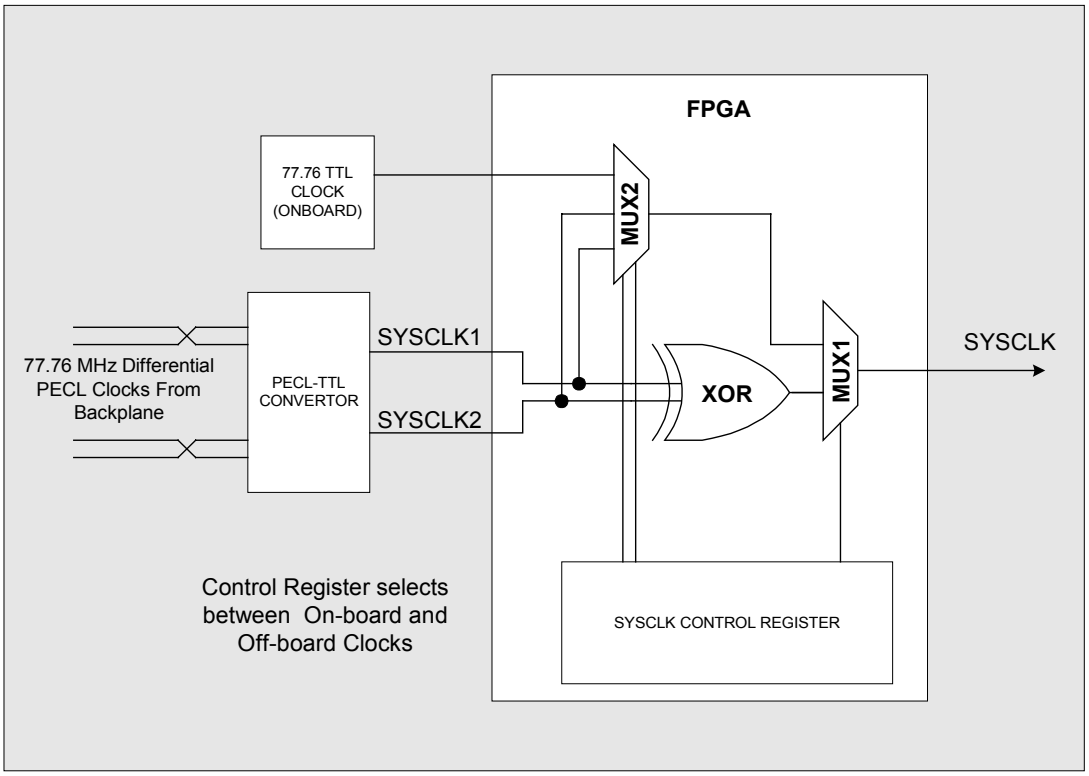
Figure 8 - FPGA Logic



7.2.1 SYSCLK Clock Source Selection

The FPGA is used to select between an on-board 77.76 MHz source clock and an off-board 77.76 MHz differential clock source. The on board clock is used for S/UNI-MACH48 register access during initial testing and diagnostic loopback mode. SYSCLK is sourced from the TSE fabric card when used in the CHESS reference design

Figure 9 - FPGA Clock Source Select Functional Block

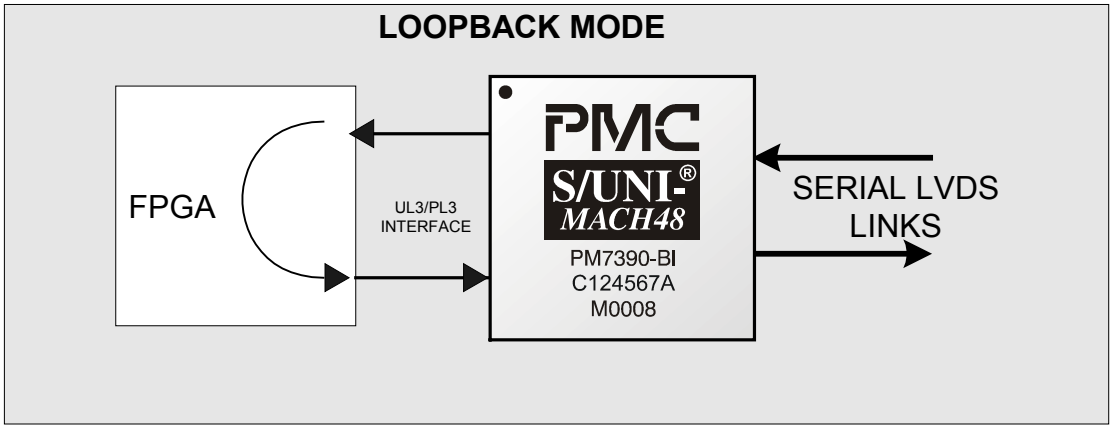


7.2.2 UTOPIA/POS-PHY Level 3 Interface

The UL3/PL3 interface can be used in two modes on the S/UNI MACH48 reference design. The UL3/PL3 interface can be switched onto the FPGA to accommodate a loopback mode or to the off board HS-3 connectors to interface with other CHESS UL3/PL3 compliant devices

In loopback mode, the FPGA will directly route the TXPHY inputs to the RXPHY outputs. This will allow the user to loopback any data input to the S/UNI MACH48 from the LVDS inputs to the LVDS outputs.

Figure 10 -Loopback Mode for FPGA/UL3/PL3 Interface



7.2.3 UL3/PL3 Bus Timing

The bus timing for the loopback interface is show below in Figure 11 and Figure 12. Each figure shows the required setup and hold time for the S/UNI MACH48 and the XC4036XLA. The T_{co} for the S/UNI MACH48 UL3/PL3 Receive bus is specified in a range from 1.5 to 6 ns. Using a 100 MHz oscillator and calculating the trace delay for the longest and shortest trace with respect to the clock, we get the following waveform relationships below.

Figure 11 - UL3/PL3 Bus Timing: Receive at FPGA

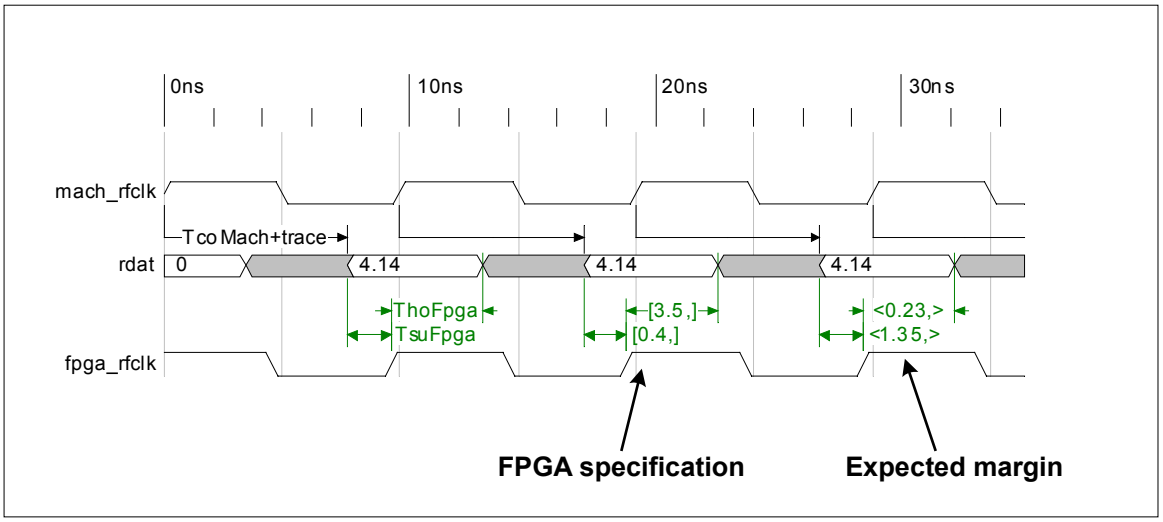
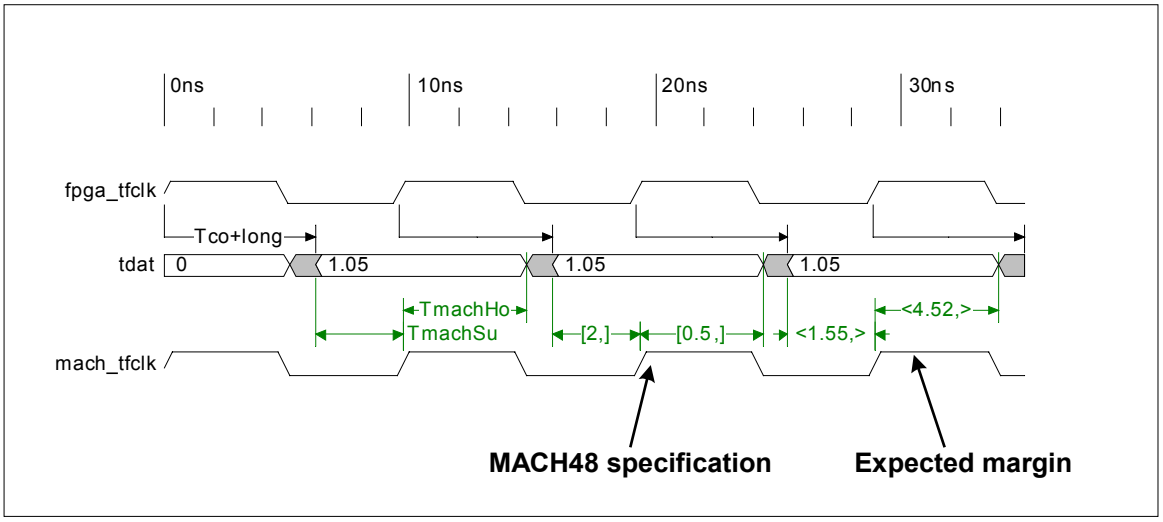


Figure 12 shows the UL3/PL3 Transmit bus timing. The setup and hold time required for the S/UNI MACH48 is 2.0 and 0.5 ns, respectively. Additionally, the T_{CO} for the FPGA combined with the board trace lengths give a range from 5.1 to 6.1 ns. As a result both the setup and hold times have a reasonable margin.

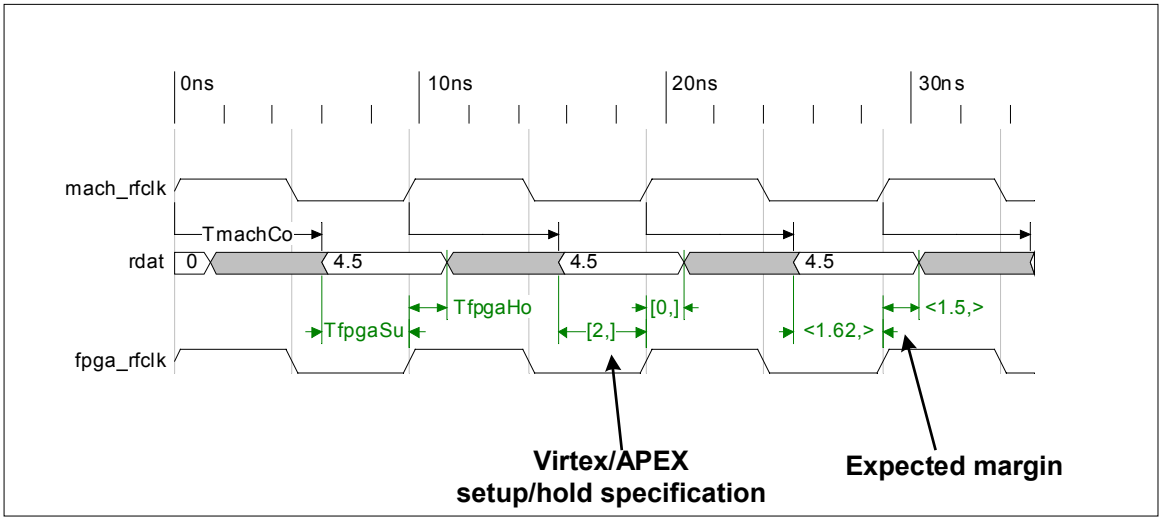
Figure 12 - UL3/PL3 Bus Timing: Transmit at FPGA



A note on FPGA selection:

The Xilinx XC4036XLA has the ability to modify the setup and hold times of the receive interface. This ability accomodates the use of bus switches on the UL3/PL3 interface which neccessitate longer trace lengths for layout while allowing the clocks traces to remain relatively short. These long trace lengths combined with a MACH-48 T_{co} of 1.5 to 6 ns decrease the setup time while increasing the hold time. The XC4036XLA can be configured to have a setup and hold time of 0.4 ns and 3.5 ns, respectively. In a typical application, where the UL3/PL3 bus is connected point to point, the trace lengths will be shorter in relation to the clock trace length, increasing the available setup time while reducing the hold time. In this case, the XC4036XLA can be set to have a setup and hold time of 4.7 and 0, respectively. This setting may not be sufficient to accommodate the full T_{co} range of the S/UNI MACH48. Alternatively, the Virtex XCV200E or APEX20KE FPGAs have improved setup/hold times and DLL functions on global clock resources that allow more concise clock control. In this figure, trace length variation is ignored across the bus.

Figure 13 - Timing on UL3/PL3 Receive Bus (VirtexE / APEX20KE)

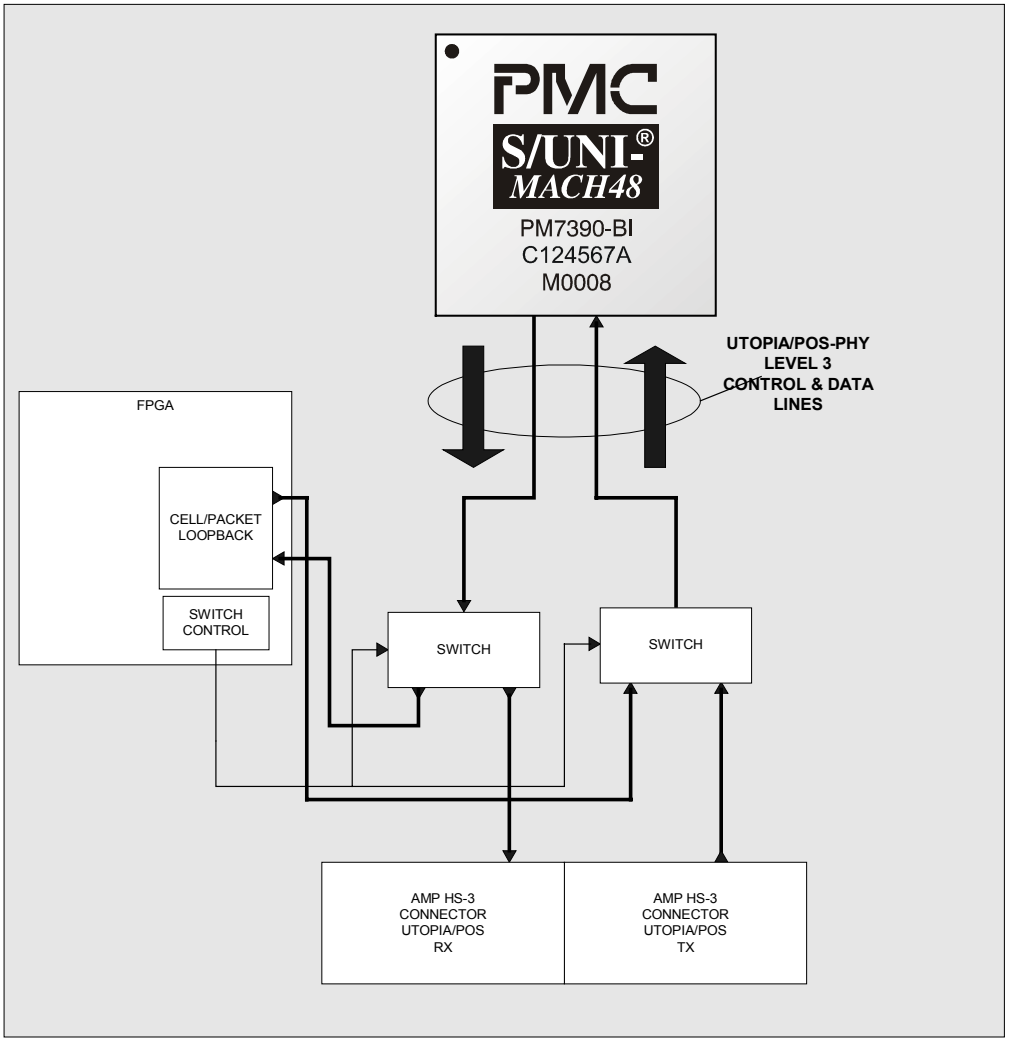


7.2.4 UL3/PL3 Source/Destination Select

The S/UNI-MACH48 reference design allows the user to switch the source and destination of the UL3/PL3 interface. The UL3/PL3 data and control lines can be switched between the FPGA and backplane interfacing connectors. During normal operation the UL3/PL3 interface is switched to the backplane to allow the S/UNI-MACH48 to communicate with other network components

When the FPGA is in loopback mode the S/UNI-MACH48 UL3/PL3 transmit and receive are effectively connected to one another, allowing traffic that is received on the serial LVDS interface to be output back onto that interface. This will allow for testing the S/UNI-MACH48 with a TSE fabric card.

Figure 14 -UTOPIA/POS-PHY INTERFACE SWITCHING



Three control lines determine the UL3/PL3 path. The table below shows the state each line must be in for each function. The FPGA controls these lines.

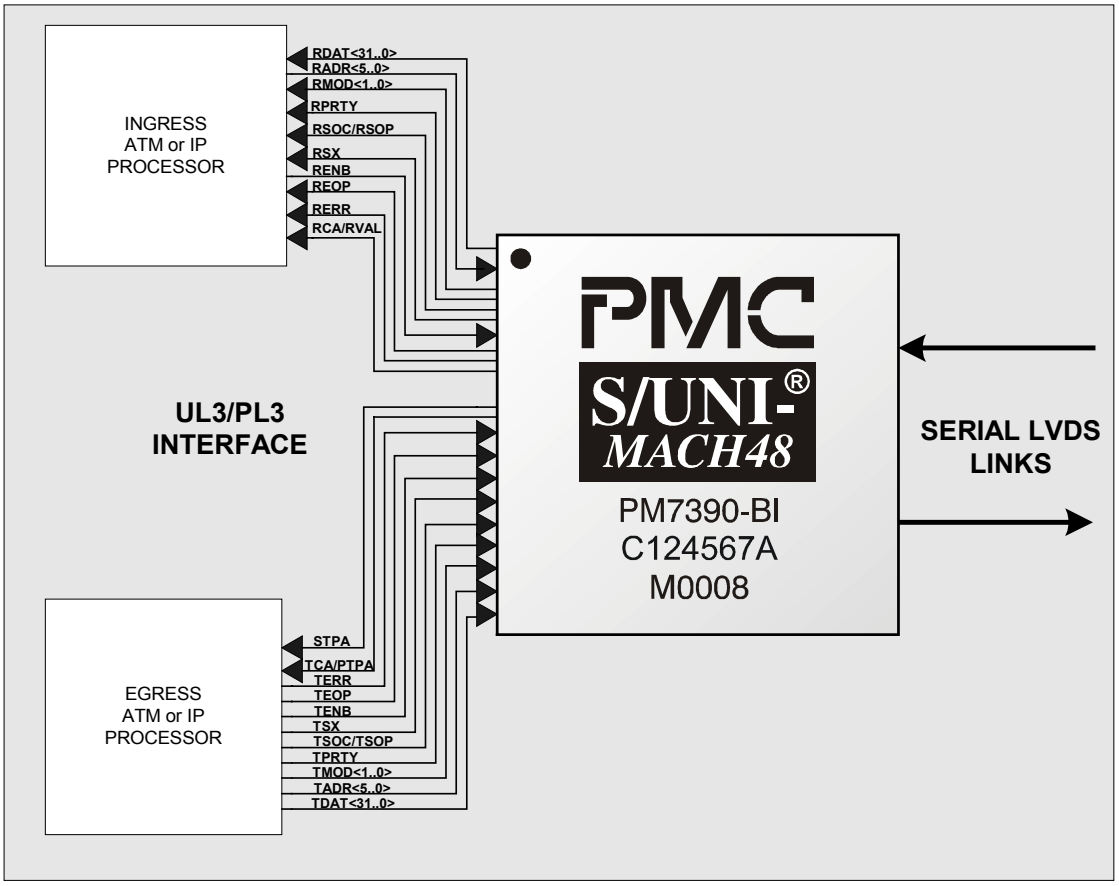
Table 1 UTOPIA/POS-PHY L3 Switching Truth Table

Function	S2	S1	S0	MACH48
Loopback	L	L	H	FPGA
Off Board	L	H	L	Connector

7.2.5 Typical UL3/PL3 Bus Layout

The S/UNI MACH48 reference design uses high speed bus switches to switch the UL3/PL3 bus between an onboard FPGA and a connector to the backplane. In a typical application, however, this switching functionality is not required and the interface is much simpler. Shorter trace lengths can also be achieved which may allow the elimination of termination resistors. A series source termination may be required for longer trace lengths, depending on how much overshoot the receiving device can tolerate (see Section 7.1.4 for calculations). A point to point interconnect is shown below

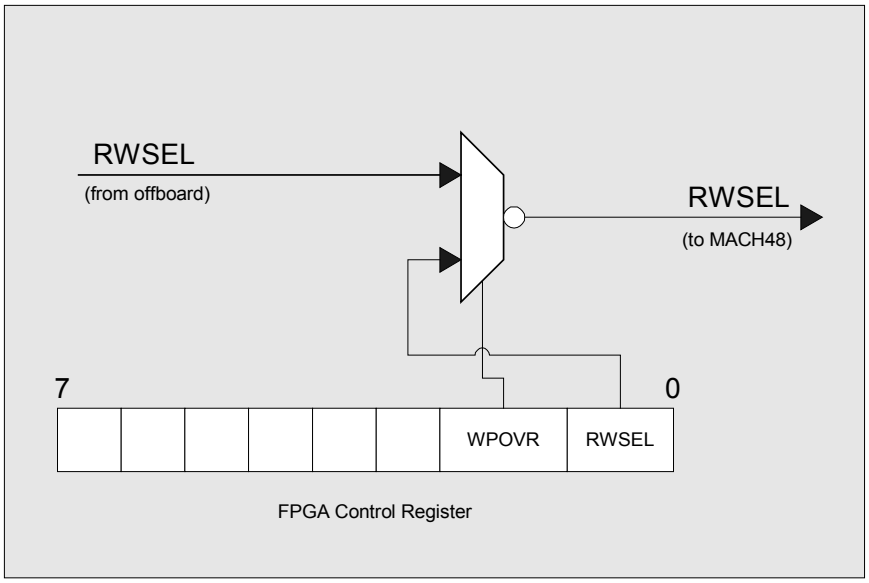
Figure 15 -Point to point UL3/PL3 interconnect



7.2.6 Working/Protection Data Link Selection

The S/UNI MACH48 switches between working and protection links depending on the state of the RWSEL input. During normal operation, the state of the RWSEL input is dictated by the system. The system will determine the best data path (either working or protection) to read from. The FPGA allows the user to manually override the RWSEL input from the system for testing purposes. The RWSEL output from the FPGA is inverted due to the re-mapping of the protection and working links as described in section 8.2.4.

Figure 16 - Multiple Sources for RWSEL



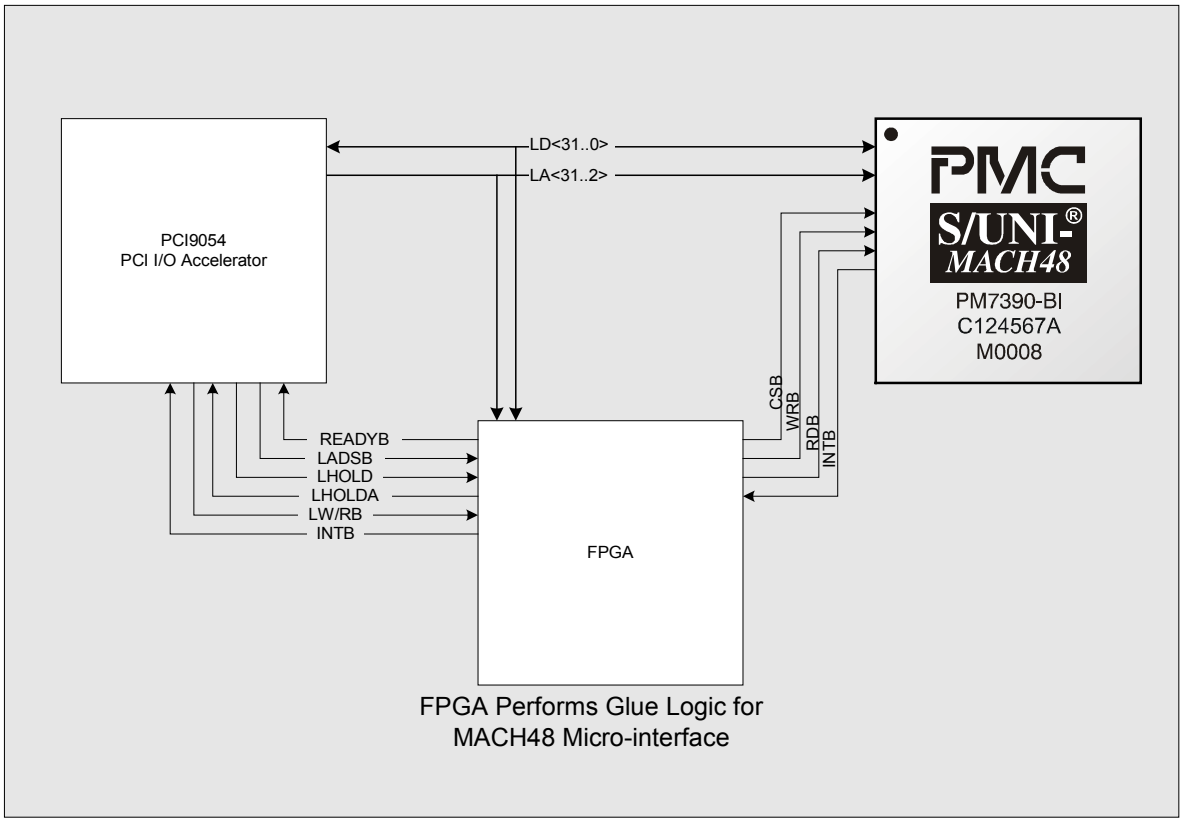
7.2.7 Connection Memory Page Selection

The incoming and outgoing connection memory pages are selected by the ICMP and OCMP pins, respectively. During normal operation, both pins are controlled by the XCMP signal from the TSE fabric card. The ICMP and OCMP can be independently modified through the MACH Control Register.

7.2.8 Microprocessor interface

The FPGA also performs glue logic to interface the S/UNI MACH48's generic microprocessor to the PCI9054 bridge device.

Figure 17 -FPGA/Microprocessor Interface



7.2.9 FPGA Register Description

Device Reset Register 0x0000

Bit	Type	Function	Default
Bit 7	R/W	NOT USED	0
Bit 6	R/W	NOT USED	0
Bit 5	R/W	NOT USED	0
Bit 4	R/W	NOT USED	0
Bit 3	R/W	NOT USED	0
Bit 2	R/W	NOT USED	0
Bit 1	R/W	NOT USED	0
Bit 0	R/W	MACH_RESETB	1

The Device Reset Register controls the reset status of each of the devices on the board.

MACH_RESETB

Writing a ‘0’ to this bit will hold the S/UNI MACH48 in reset. Writing a ‘1’ will take the device out of reset.

FPGA Control Register 0x0010

Bit	Type	Function	Default
Bit 7	R/W	NOT USED	0
Bit 6	R/W	NOT USED	0
Bit 5	R/W	FPEN	1
Bit 4	R/W	CMPOVR	0
Bit 3	R/W	ICMPSEL	0
Bit 2	R/W	OCMPSEL	0
Bit 1	R/W	WPOVREN	0
Bit 0	R/W	RWSEL	0

FPEN

When the Frame Pulse Enable bit is set, the 8kHz frame pulse generated from off board is passed to the MACH48. When FPEN is 0, this pulse does not pass to the MACH48.

CMPOVR

The default for CMP is to have these values set by the off board XCMP signal. This occurs when CMPOVR is set to 0. However, when set to 1, both the ICMPSEL and OCMPSEL values become valid and the off board value is ignored.

ICMPSEL

ICMPSEL will select the Incoming Connection Memory Page. If ICMPSEL is 0, the FPGA will set the ICMP pin on the MACH48 to 0,setting Memory connection Page 0. If ICMPSEL is 1, Memory Connection Page 1 is selected. If CMPOVR is 0, this bit is ignored.

OCMPSEL

OCMPSEL will select the Outgoing Connection Memory Page in the MACH48. If OCMPSEL is 0, Memory Connection Page 0 will be selected. If OCMPSEL is 1, Memory Connection Page 1 will be selected. If CMPOVR is 0, this bit is ignored.

WPOVR

The WPOVR (**W**orking/**P**rotect **OV**e**R**ride) bit controls whether the RWSEL bit is controlled by an off-board source (TSE card) or by the control register. When WPOVR is 0, the RWSEL bit is controlled by the off-board source, which is passed transparently through the FPGA. When WPOVR is 1, RWSEL is controlled by the Control Register.

RWSEL

The RWSEL bit selects between the Working and Protection Data streams on the MACH48. When RWSEL is 1, the Working data stream is selected. When RWSEL is 0, the Protection data stream is selected. If WPOVREN is set to 0, this bit is ignored.

SYSCLK Control Register 0x0020

Bit	Type	Function	Default
Bit 7	R/W	NOT USED	0
Bit 6	R/W	NOT USED	0
Bit 5	R/W	NOT USED	0
Bit 4	R/W	NOT USED	0
Bit 3	R/W	NOT USED	0
Bit 2	R/W	MUX1	0
Bit 1	R/W	MUX2A	1
Bit 0	R/W	MUX2B	1

MUX1 – MUX2B

The following truth table will switch the SYSCLK accordingly.

Table 2: Truth Table for SYSCLK Switching

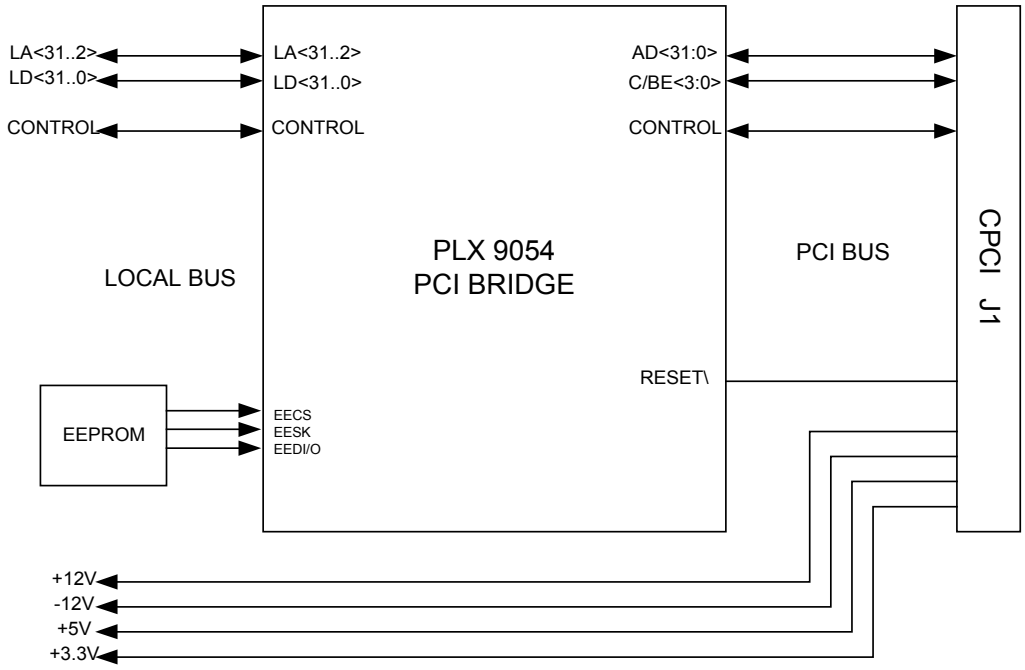
MUX1	MUX2A	MUX2B	FUNCTION
0	0	0	SYSCLK1
0	0	1	SYSCLK2
0	1	1	ON BOARD SYSCLK1
1	X	X	SYSCLK2 XOR SYSCLK2

7.3 CompactPCI Interface

The PM7390 S/UNI MACH48 includes a microprocessor interface to provide read/write access to normal mode registers as described within the S/UNI MACH48 Data Sheet. This design connects a CompactPCI bus to this microprocessor interface.

A block diagram of the cPCI interface and bridge is shown below in Figure 18.

Figure 18 -CompactPCI Block Diagram.



7.3.1 Interface and Bridge Hardware

The PCI9054 is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The 32 bit multiplexed address/data bus and associated control lines connect directly from the CPCI J1 connector to the PLC PCI9054 bridge device. The bus and control lines are terminated with 10 ohm stub resistance that should be placed close to the J1 connector pins.

For this reference design the PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. Address lines LA<31...2> provide 32-bit word addressing. The lower two bits of the address lines are used for 16 or 8 bit byte access but are unused in this application. The FPGA implements the local bus glue logic.

A serial 93CS66L EEPROM is used for device configuration after reset or upon power-up. The PCI9054 can also be configured by an onboard microprocessor if desired.

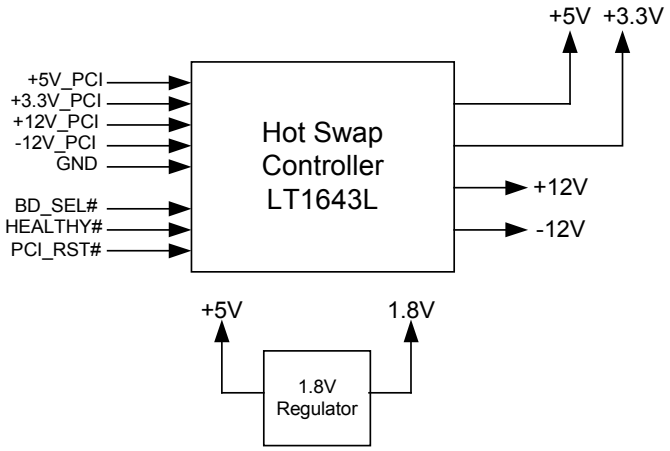
7.3.2 Hot Swap Capability

In addition to the local and PCI bus interfaces, the cPCI block provides some of the hardware required for hot swap. The hot swap specification outlines a hardware and software solution to allow cPCI boards to be safely inserted or removed from an active CPCI backplane. Note that this block does not provide the minimum Hot Swap requirements for safe insertion and extraction. An additional Hot Swap controller is required to safely power up and power down the board.

The cPCI block provides 1V pre-charge voltage to cPCI bus pins to reduce pin bounce during connection or removal. Most cPCI pins are pulled up to 1V with 4 other pins (RST#, ENUM#, INTA#, and REQ#) pre-charged to V(I/O) to provide a stable clock prior to bus contact.

7.4 Power Supply

Figure 19 - Power Supply Board System Block.



The Power Block provides stable voltage supplies delivered over the CompactPCI backplane from a centralized power supply. Voltage levels of +5V, +3.3V, +12V, -12V and regulated 1.8V are available from this block.

8 IMPLEMENTATION DESCRIPTION

This section details the hardware on the S/UNI-MACH48 reference design and references the schematics in Section 9.

8.1 Sheet 1, Root Drawing

This sheet shows the interconnection between the functional blocks of the S/UNI MACH48 reference design. The design is comprised of five functional blocks: the MACH48 Block, FPGA Block, System Interface, CPCI Block and Power Block.

8.2 Sheet 2,3,4,5 MACH48 Block

8.2.1 Sheet 2: Microprocessor Interface

This block shows the generic microprocessor interface. Note that A[13] has a 4.7K pull down resistor. This pull down will cause the device to default accesses to the normal mode registers. If A[13] is set high, the device will allow access to test mode registers. JTAG pins are not connected. The DS3 overhead is not used in this application and these pins are connected to a 2x16 pin header.

8.2.2 Sheet 3: UTOPIA/POS-PHY Level 3 Interface

This block shows the UTOPIA/POS-PHY Level 3 (UL3/PL3) interface on the S/UNI-MACH48. All lines for this interface are 50 Ohm controlled impedance with series source terminations of 39 ohms.

8.2.3 Sheet 4: Serial Telecombus Interface

This block shows both the Parallel and Serial Telecombus interfaces. In this reference design, the parallel telecombus is not used (disabled via register). The serial telecombus operates at 777.6 Mbps, which is synthesized from the 77.76Mhz system clock. It is important that these differential pairs be matched 50 ohm impedance lines with equal trace lengths (within 0.050 inches). The serial telecombus is connected to an AMP HS3 type connector that allows the interface to transmit and receive LVDS signals from a custom backplane. For further information on LVDS design considerations, consult Reference 7.

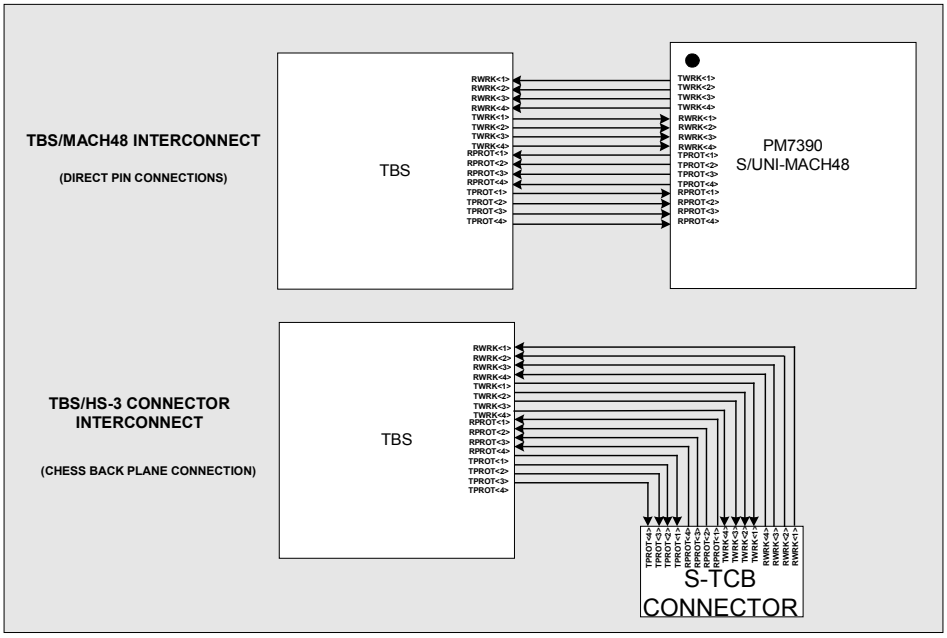
Table 3 Pinout of S-TCB HS3 Connector

	A	B	C	D	E	F
1	GND	SYSCLK1P	SYSCLK1N	SYSCLK2P	SYSCLK2N	GND
2	GND	RPPROT4	RNPROT4	TPPROT4	TNPROT4	GND
3	GND	RPPROT3	RNPROT3	TPPROT 3	TNPROT3	GND
4	GND	RPPROT2	RNPROT2	TPPROT2	TNPROT2	GND
5	GND	RPPROT1	RNPROT1	TPPROT1	TNPROT1	GND
6	GND	RPWRK4	RNWRK4	TPWRK4	TNWRK4	GND
7	GND	RPWRK3	RNWRK3	TPWRK3	TNWRK3	GND
8	GND	RPWRK2	RNWRK2	TPWRK2	TNWRK2	GND
9	GND	RPWRK1	RNWRK1	TPWRK1	TNWRK1	GND
10-	GND	TJ0FP_OUT	RJ0FP_IN	RWSEL_IN	XCMP_IN	GND

8.2.4 Port Re-mapping of Serial Telecombus

The S/UNI MACH48 Serial Telecombus (S-TCB) pin out locations are organized for direct connection to the TBS device. This direct connection is duplicated for the backplane connector of the CHESS reference design.

Figure 20 - TBS-MACH48 LVDS Interconnections



In order to create a backplane with generic line card interfaces for the CHESS reference design, it is necessary to route the S/UNI MACH48 S-TCB to match the TBS to connector pin out. This creates difficulty when trying to layout the LVDS links from the S/UNI MACH48, as an increasing number of board layers are required to accommodate the trace crossovers. Using the STS-12 port re-mapping capability of the S/UNI MACH48 allows the software to re-map the channels. Re-mapping the channels according to Table 4 will simplify PCB routing by eliminating crossovers.

Figure 22 - Routing with Software Re-mapping

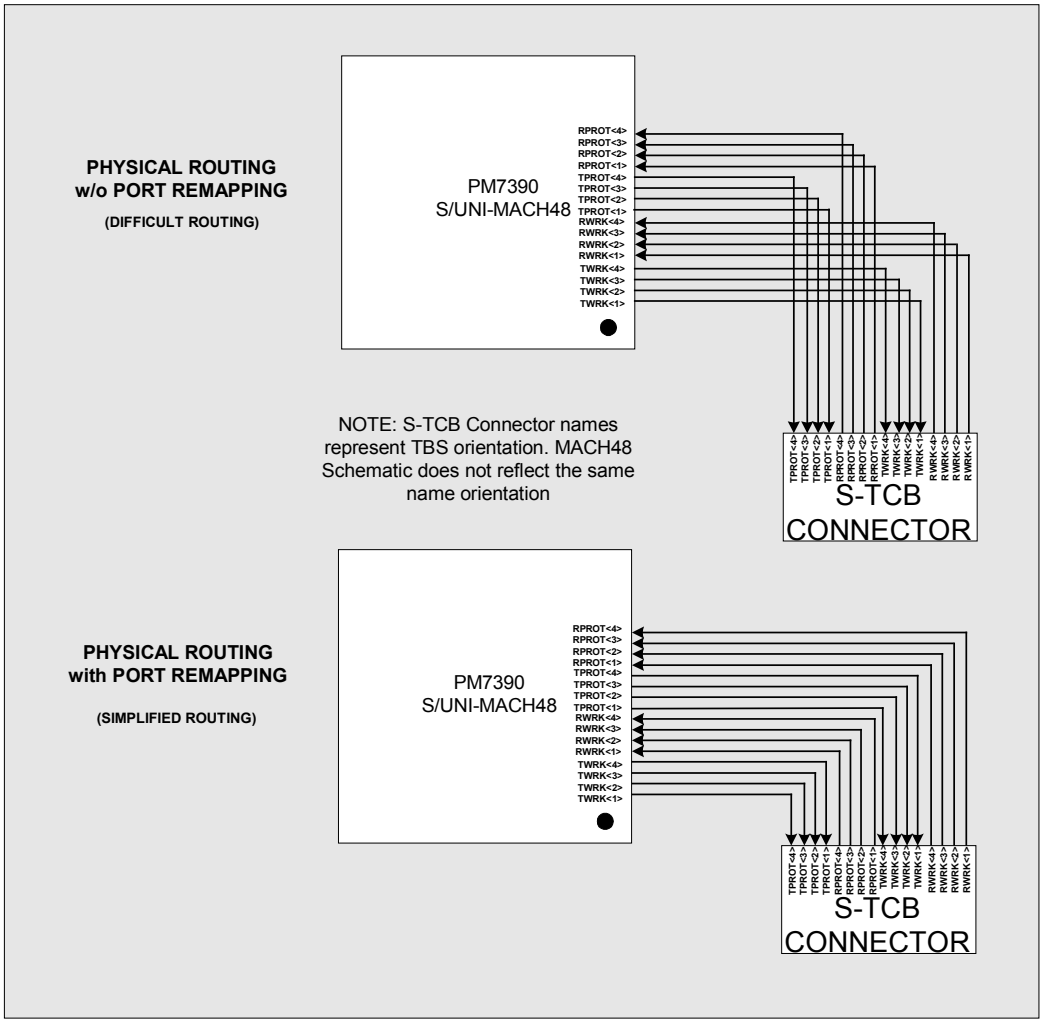


Table 4 STS-12 Port Remapping for S-TCB

S/UNI MACH48	HS-3 Off-Board Connector (TBS References)
RWRK<1..4>	RPROT<4..1>
TWRK<1..4 >	TPROT<4..1>
RPROT<1..4>	RWRK<4..1>
TPROT<1..4>	TWRK<4..1>

This re-mapping scheme transposes the working data links with the protection data links. While this will not affect the operation of the device, it is useful to maintain the logic of the working and protect links. By inverting the logic of the RWSEL signal, the S/UNI MACH48 will maintain the sense of the link. This logic inversion is done with the FPGA. If the MACH48 is to be installed in a fixed backplane position, then the backplane can be routed to reduce signal crossovers.

8.2.5 Sheet 5:S/UNI MACH48 Power Block

The power block shows all of the power and ground connections for the MACH48 device. It is required that the 3.3 VDC I/O be powered before or at the same time as the 1.8 VDC core supply to prevent damage to the ESD protection structures within the MACH48 device. The 3.3VDC AVDH analog power supplies are filtered with an RC network attached to each analog power pin. The 1.8VDC AVDL analog power pins have their own regulator which will provide the required current while maintaining the +/- 5% tolerance. The tolerance on the 3.3 VDC supply is +/- 10%.

Table 5 S/UNI MACH48 Typical Power Consumption

Power Supply	Current (mA)	Power (mW)
AVDL(1.8V)	210	378
AVDH(3.3V)	160	528
VDDI total	2450	4410
VDDO total	240	792
Total Consumption	**3060**	**6108**

Note: VDDO total power is approximately 500 mW without the Parallel telecombus.

8.3 Sheet 6,7 FPGA Block

8.3.1 Sheet 6: FPGA Block

This sheet shows the Xilinx XC4036XLA-8 FPGA. This performs several functions on the S/UNI MACH48 reference design. The connections for the UL3/PL3 interface are optimized for minimum delay when in loopback mode. At power up, the FPGA code is loaded from one of two Xilinx XC1701L SPROMS. A three pin jumper is used to determine which PROM to download code from prior to power up. Alternatively, the FPGA can be programmed directly from the on board header. This requires a Xilinx Xchecker programming cable.

8.3.2 Sheet 7: UL3/PL3 Bus Switching Block

This sheet shows the CMOS switches used to switch the UTOPIA/POS-PHY bus between the FPGA and the HS3 Connector. This switch array uses 8 Pericom PI5C16212 high bandwidth, 24 bit bus exchanges switch devices. The switches are controlled by the FPGA through the L_SEL<2..0> bus. The 100MHz UL3/PL3 clock can be switched between on-board and off-board sources. This is done using a QS4A201Q high speed two bit switch which is also controlled by the FPGA through the CLK_SEL<1..0> bus. The 100MHz (100ppm) oscillator and driver is also shown on this sheet. The Pericom PI49FCT3807 clock driver must be B grade or better (>= 100MHz). This clock driver will also provide clocking for other boards connected by the UL3/PL3 backplane if desired. It should be noted that these bus switches are not required in a typical UL3/PL3 configuration.

8.4 Sheet 9 System Interface Block

The system interface block shows three AMP HS-3 connectors that are used to interface the Serial Telecombus and the UL3/PL3 receive and transmit. A PECL to TTL converter is also present to convert the off board 77.76MHz differential system clock to TTL levels.

8.5 Sheet 9,10 CompactPCI Block

8.5.1 Sheet 9: I/O Accelerator Block

This sheet shows the PCI 9054 I/O Accelerator. This is the bridge chip that allows the PCI bus to communicate with the local microprocessor interface.

The CPCI_BLOCK shows the PLX 9054 signal and power circuitry connections.

The PCI9054 is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The 32 bit multiplexed address/data bus and associated control lines connect directly from the CPCI J1 connector to the PLC PCI9054 interface device. The bus and control lines are terminated with 10 ohm stub resistance that should be placed close to the J1 connector pins.

The PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. Address lines LA<31...2> provide 32 bit word addressing. The lower two bits of the address lines are used for 16 or 8 bit byte access but are unused in this application.

A serial EEPROM is required for device configuration after reset or upon power-up. A NM93CS66 serial EEPROM is used to program the 9054.

The Compact PCI specification outlines a number of layout requirements for the CPCI design. These include:

- All 10 ohm stub termination resistors must be placed within 0.6 of the J1 pins,
- All PCI signal traces must be less than 1.5 (including stub resistor) except P_CLK,
- P_CLK trace must be 2.5 +/- 0.1,
- CPCI bus traces impedance is 65 Ω,
- 39 ohm stub resistor on REQ# should be placed near its source on the PCI9054.

8.5.2 Sheet 11: CompactPCI Connector

This sheet shows the CPCI connector J1. An AMP Z-PACKS connector is used per the CPCI Specification (PICMG 2.0 R2.2)

8.6 Sheet 12, Power Supply and Hot Swap Controller Block

This sheet shows the power supplies for the board. All CPCI compliant voltages are present as well as a 1.8 V source for driving the MACH 48 logic. The

switching regulator is driven by the PCI bus 5 VDC supply. The 3.3 VDC(VDDO, AVDH) supply must be present on the MACH48 before the 1.8 VDC (VDDI, AVDL) supply. To do this, a power supply supervisory circuit is used to control the power supply enable such that if the 3.3 VDC is not present, the 1.8 VDC supply will not turn on. There is also a Hot Swap controller that allows for the removal and replacement of circuit boards into a live PCI slot without damage to on board components. The PWROK_1_8V pin connected to the FPGA is used to indicate when the 1.8V supply is fully powered up. The FPGA will delay any switching until the core voltage is fully powered. The 12VDC and –12VDC supplies are present but not used in this application. For more information on power supply sequencing, See Reference 6, Section 8.3 “Power Sequencing Rules for 1.8V and 3.3V Supplies”.

9 SCHEMATICS

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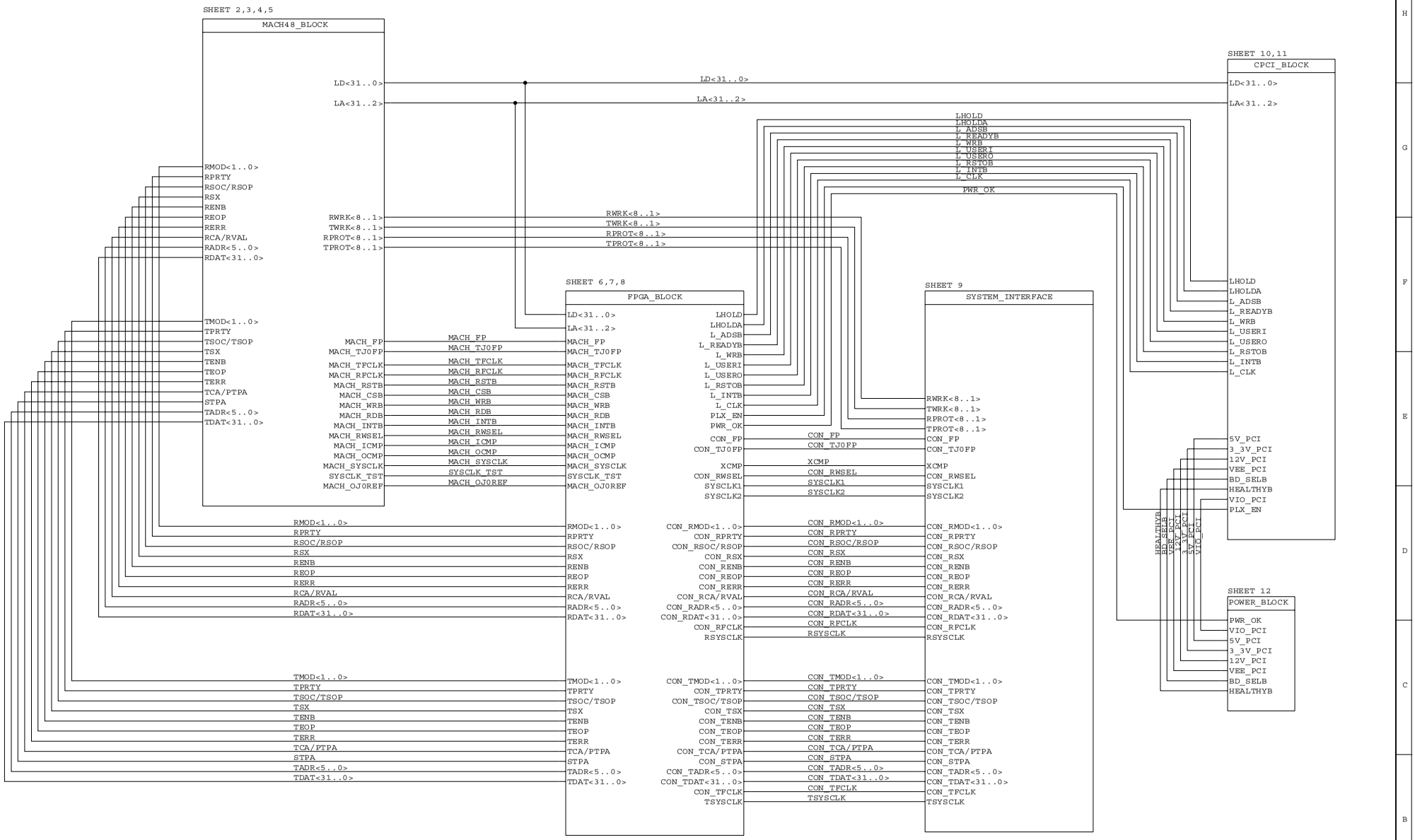

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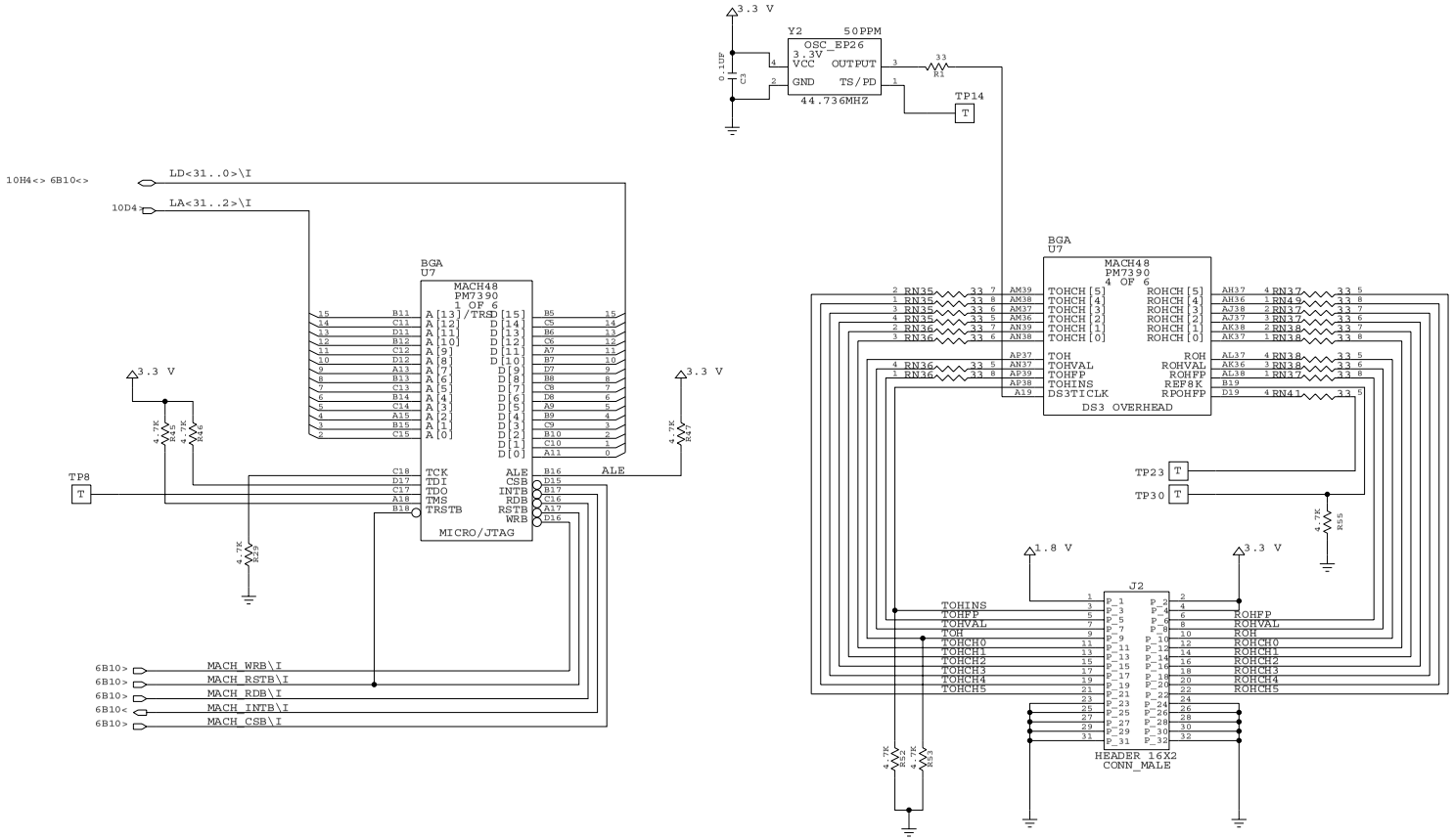

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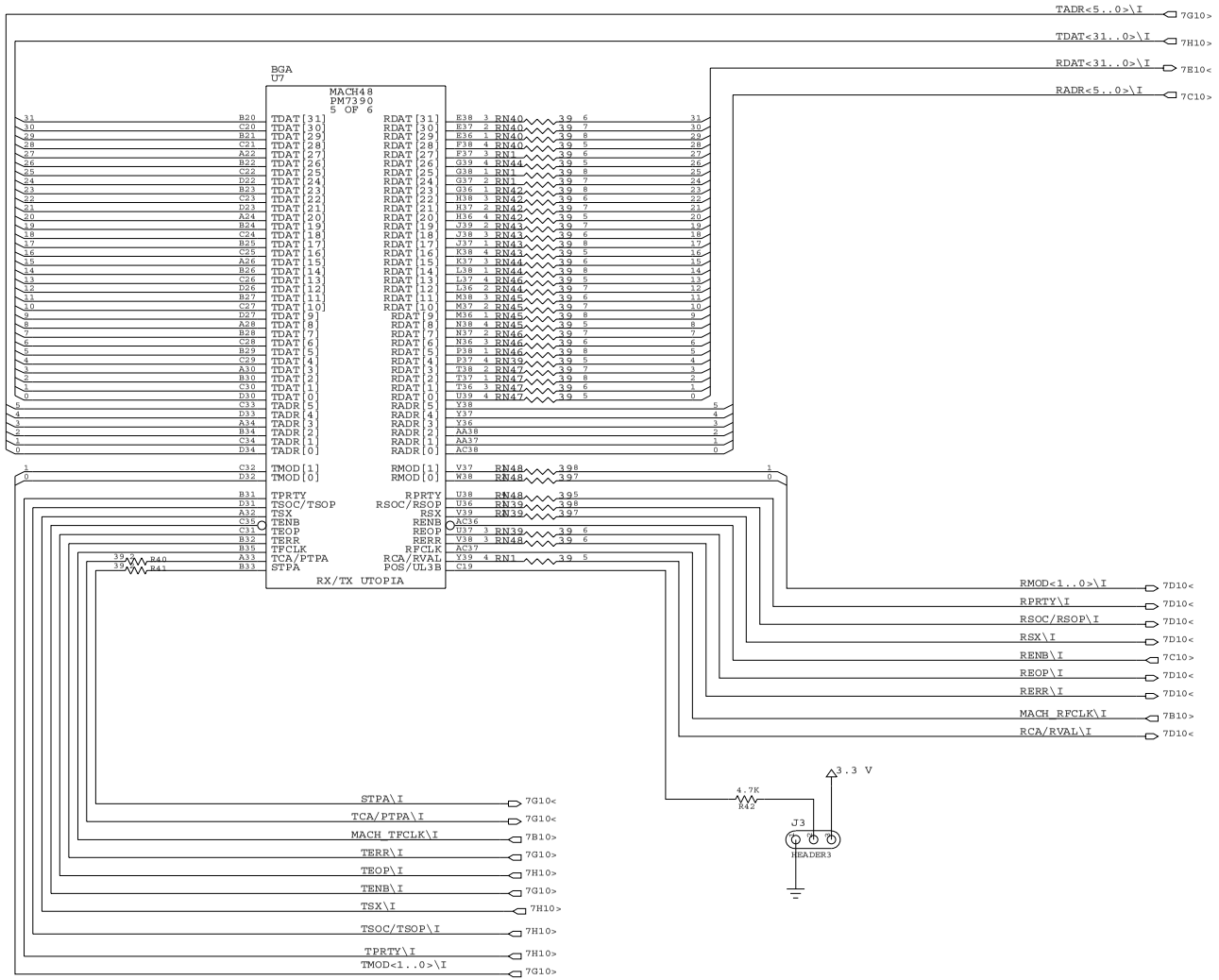

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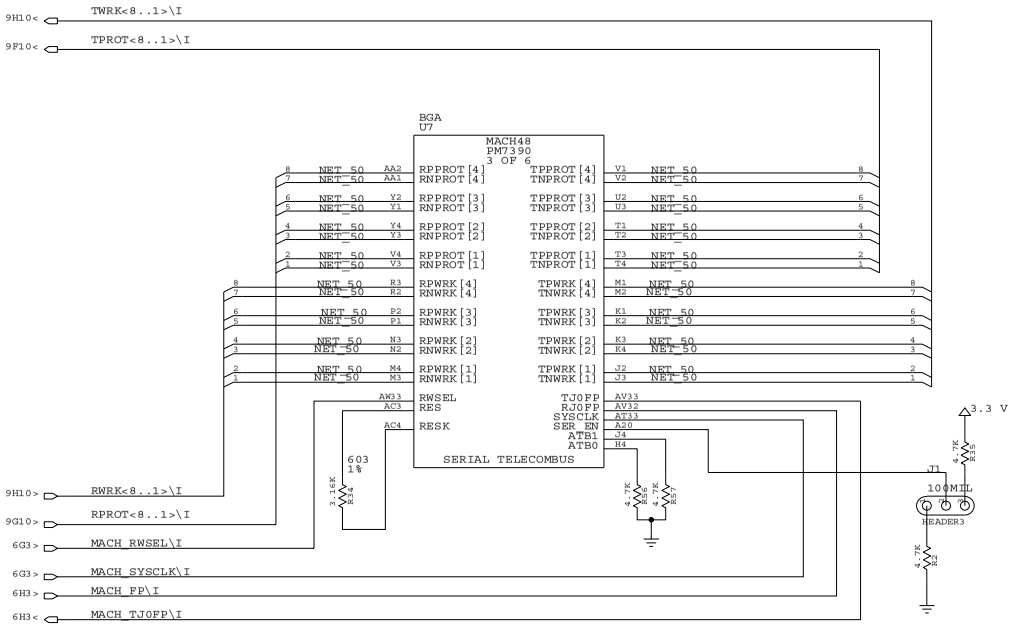

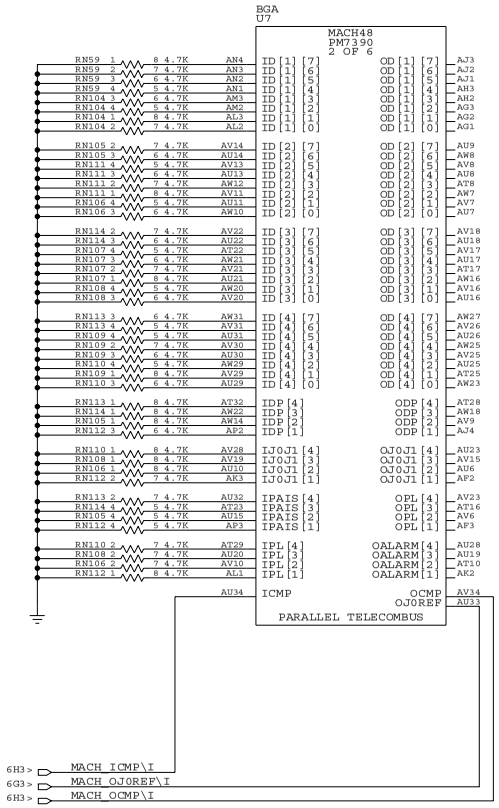

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ENGINEER: RS	PAGE:4 OF 12

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PLACE 0.1UF CAPS NEAR PINS

3.3 V

805 5% 0 R36 — 0.1UF C40
805 5% 0 R30 — 0.1UF C44
805 5% 0 R31 — 0.1UF C45
805 5% 0 R32 — 0.1UF C46

ANALOG 3.3 VDC

NOTE: SOLDER BRIDGE IS FOR TEST PURPOSES ONLY

1.8 V

SB1 SOLDERBRIDGE (P<1> P<2> P<3> P<4>)

3.3 V

TO263 3A ADJ U14 — LM1085 (INPUT, OUTPUT, TAB, ADJ/GND)

10UF C35

100 1% 603 R27

1% 805 402 R33

10UF C109, 10UF C29, 10UF C30, 10UF C110

1.8 VA

ANALOG 1.8 VDC

1.8 VA

0.1UF C36, 0.1UF C37, 0.1UF C38, 0.1UF C43, 0.1UF C47, 0.1UF C48

PLACE CAPS NEAR POWER PINS

BGA U7

MACH4 8 PM7390 6 OF 6

L4	AVDH3	VSS75	AW39
R4	AVDH2	VSS74	AW38
W4	AVDH1	VSS73	AW37
AA4	AVDH0	VSS72	AW36
		VSS71	AW34
P3	AVDL4	VSS70	AW32
W2	AVDL3	VSS69	AW30
AB4	AVDL2	VSS68	AW28
AB3	AVDL1	VSS67	AW26
AA3	AVDL0	VSS66	AW24
		VSS65	AW19
B2	VDDO56	VSS64	AW17
B3	VDDO55	VSS63	AW15
B4	VDDO54	VSS62	AW13
C2	VDDO53	VSS61	AW11
C3	VDDO52	VSS60	AW9
C4	VDDO51	VSS59	AW4
D2	VDDO50	VSS58	AW3
D3	VDDO49	VSS57	AW2
D4	VDDO48	VSS56	AA39
D6	VDDO47	VSS55	AC39
D10	VDDO46	VSS54	AE39
D14	VDDO45	VSS53	AG39
D21	VDDO44	VSS52	AJ39
D25	VDDO43	VSS51	AL39
D29	VDDO42	VSS50	AT39
B36	VDDO41	VSS49	AU39
B37	VDDO40	VSS48	AV39
B38	VDDO39	VSS47	B39
C36	VDDO38	VSS46	C39
C37	VDDO37	VSS45	D39
C38	VDDO36	VSS44	H39
D36	VDDO35	VSS43	M39
D37	VDDO34	VSS42	T39
D38	VDDO33	VSS41	AU1
P36	VDDO32	VSS40	AP1
K36	VDDO31	VSS39	AK1
P36	VDDO30	VSS38	AF1
AA36	VDDO29	VSS37	AD1
AE36	VDDO28	VSS36	AH1
AJ36	VDDO27	VSS35	AM1
AJ38	VDDO26	VSS34	AT1
AT37	VDDO25	VSS33	AV1
AT36	VDDO24	VSS32	P39
AU38	VDDO23	VSS31	K39
AU37	VDDO22	VSS30	F39
AU36	VDDO21	VSS29	W1
AV38	VDDO20	VSS28	U1
AV37	VDDO19	VSS27	R1
AV36	VDDO18	VSS26	N1
AT34	VDDO17	VSS25	L1
AT30	VDDO16	VSS24	J1
AT26	VDDO15	VSS23	D1
AT19	VDDO14	VSS22	AW1
AT15	VDDO13	VSS21	C1
AT11	VDDO12	VSS20	B1
AV4	VDDO11	VSS19	A39
AV3	VDDO10	VSS18	A38
AV2	VDDO9	VSS17	A37
AU4	VDDO8	VSS16	A36
AU3	VDDO7	VSS15	A31
AU2	VDDO6	VSS14	A29
AT4	VDDO5	VSS13	A27
AT3	VDDO4	VSS12	A25
AT2	VDDO3	VSS11	A23
AP4	VDDO2	VSS10	A21
AK4	VDDO1	VSS9	A16
AF4	VDDO0	VSS8	A14
		VSS7	A12
D9	VDDI37	VSS6	A10
D5	VDDI36	VSS5	A8
D13	VDDI35	VSS4	A6
D18	VDDI34	VSS3	A4
D20	VDDI33	VSS2	A3
D24	VDDI32	VSS1	A2
D28	VDDI31	VSS0	A1
J36	VDDI30		
N39	VDDI29		
R36	VDDI28		
V36	VDDI27		
W36	VDDI26		
W37	VDDI25		
W39	VDDI24		
AB36	VDDI23		
AG36	VDDI22		
AL36	VDDI21		
AN36	VDDI20		
AP36	VDDI19		
AT35	VDDI18		
AT31	VDDI17		
AT27	VDDI16		
AT24	VDDI15		
AT21	VDDI14		
AT20	VDDI13		
AT18	VDDI12		
AT14	VDDI11		
AT12	VDDI10		
AT9	VDDI9		
AT7	VDDI8		
AT6	VDDI7		
AR4	VDDI6		
AM4	VDDI5		
AL4	VDDI4		
AH4	VDDI3		
AG4	VDDI2		
AD4	VDDI1		
C7	VDDI0		

POWER

1.8 V

3.3 V

1.8 V

3.3 V

0.1UF C49, 0.1UF C50, 0.1UF C51, 0.1UF C52, 0.1UF C53, 0.1UF C54, 0.1UF C55, 0.1UF C56, 0.1UF C57, 0.1UF C58, 0.1UF C59, 0.1UF C60, 0.1UF C61, 0.1UF C62, 0.1UF C63, 0.1UF C64, 0.1UF C65, 0.1UF C66, 0.1UF C67, 0.1UF C68, 0.1UF C69, 0.1UF C70, 0.1UF C71, 0.1UF C72, 0.1UF C73, 0.1UF C74, 0.1UF C75, 0.1UF C76, 0.1UF C77, 0.1UF C78, 0.1UF C79, 0.1UF C80, 0.1UF C81, 0.1UF C82, 0.1UF C83, 0.1UF C84, 0.1UF C85, 0.1UF C86, 0.1UF C87, 0.1UF C88, 0.1UF C89, 0.1UF C90, 0.1UF C91, 0.1UF C92, 0.1UF C93, 0.1UF C94, 0.1UF C95, 0.1UF C96, 0.1UF C97, 0.1UF C98, 0.1UF C99, 0.1UF C100, 0.1UF C101, 0.1UF C102, 0.1UF C103

10UF C111, 10UF C107, 10UF C125, 10UF C127, 10UF C129, 10UF C134, 10UF C132

PLACE TWO 10UF CAPACITORS ON EACH EDGE OF THE MACH48

10UF C124, 10UF C126, 10UF C128, 10UF C130, 10UF C131, 10UF C133, 10UF C135, 10UF C153

PLACE TWO 10UF CAPACITORS ON EACH EDGE OF THE MACH48

3.3 V

1.8 V

TP9, TP11, TP15, TP17, TP19, TP25

TP10, TP13, TP16, TP18, TP20, TP26

DISTRIBUTE TEST POINTS THROUGHOUT PCB
AND LABEL WITH VOLTAGE VALUE

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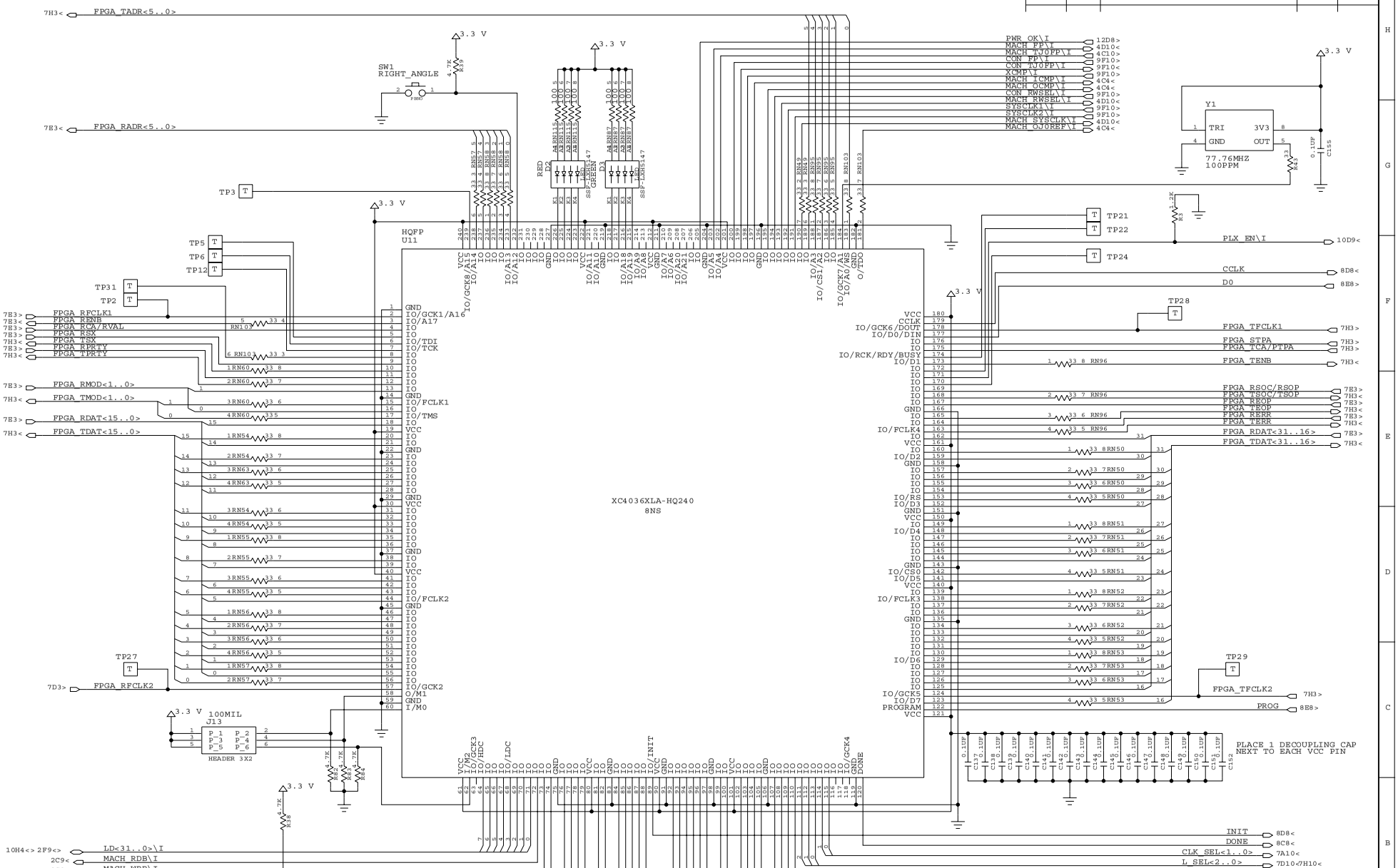

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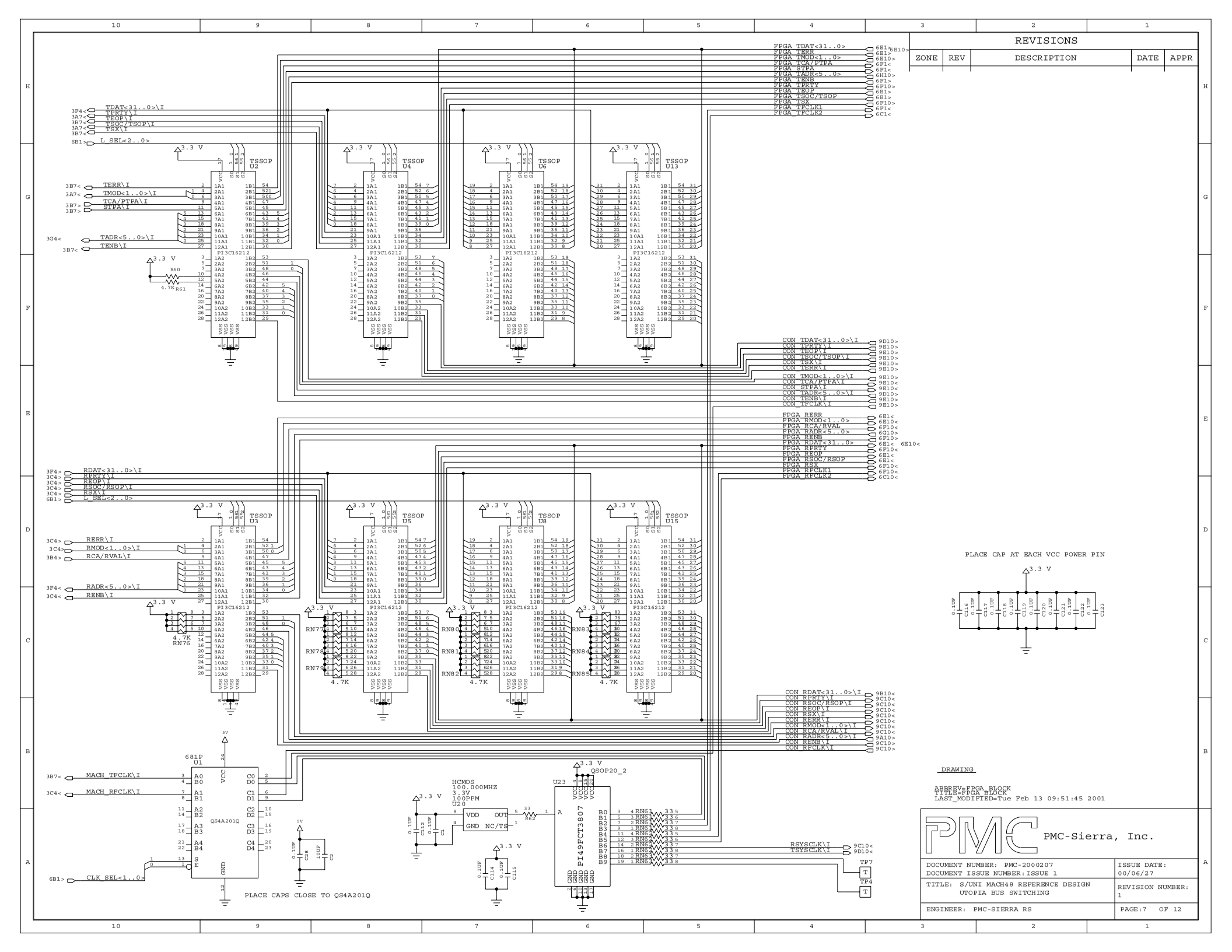
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FPGA_TADR<5..0>
FPGA_TENB
FPGA_TPRTY
FPGA_TEOP
FPGA_TSOC/TSOP
FPGA_TSX
FPGA_TFCLK1
FPGA_TFCLK2
TDAT<31..0>\I
TPRTY\I
TEOP\I
TSOC/TSOP\I
TSX\I
L_SEL<2..0>
TERR\I
TMOD<1..0>\I
TCA/PTPA\I
STPA\I
TADR<5..0>\I
TENB\I
TSSOP U2
TSSOP U4
TSSOP U6
TSSOP U13
PI3C16212
R60
4.7K R61
CON_TDAT<31..0>\I
CON_TPRTY\I
CON_TEOP\I
CON_TSOC/TSOP\I
CON_TSX\I
CON_TERR\I
CON_TMOD<1..0>\I
CON_TCA/PTPA\I
CON_STPA\I
CON_TADR<5..0>\I
CON_TENB\I
CON_TFCLK\I
FPGA_RERR
FPGA_RMOD<1..0>
FPGA_RCA/RVAL
FPGA_RADR<5..0>
FPGA_RENB
FPGA_RDAT<31..0>
FPGA_RPRTY
FPGA_REOP
FPGA_RSOC/RSOP
FPGA_RSX
FPGA_RFCLK1
FPGA_RFCLK2
RDAT<31..0>\I
RPRTY\I
REOP\I
RSOC/RSOP\I
RSX\I
L_SEL<2..0>
RERR\I
RMOD<1..0>\I
RCA/RVAL\I
RADR<5..0>\I
RENB\I
TSSOP U3
TSSOP U5
TSSOP U9
TSSOP U15
4.7K RN76
RN77
RN78
RN79
RN80
RN81
RN82
RN83
RN84
RN85
4.7K
CON_RDAT<31..0>\I
CON_RPRTY\I
CON_RSOC/RSOP\I
CON_REOP\I
CON_RSX\I
CON_RERR\I
CON_RMOD<1..0>\I
CON_RCA/RVAL\I
CON_RADR<5..0>\I
CON_RENB\I
CON_RFCLK\I
PLACE CAP AT EACH VCC POWER PIN
C116 0.1UF
C117 0.1UF
C118 0.1UF
C119 0.1UF
C120 0.1UF
C121 0.1UF
C122 0.1UF
C123 0.1UF
681P U1
MACH_TFCLK\I
MACH_RFCLK\I
QS4A201Q
CLK_SEL<1..0>
PLACE CAPS CLOSE TO QS4A201Q
C28 0.1UF
C2 10UF
HCMOS 100.000MHZ 3.3V 100PPM U20
C112 0.1UF
C1 0.1UF
R62 33
C114 0.1UF
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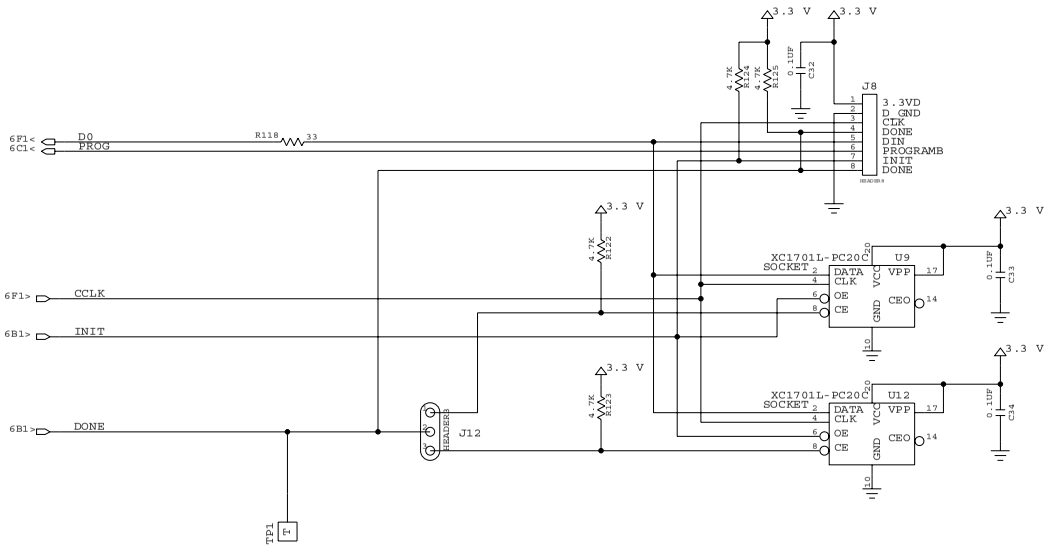
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-2000207
DOCUMENT ISSUE NUMBER: ISSUE 1
ISSUE DATE: 00/06/27
TITLE: S/UNI MACH48 REFERENCE DESIGN UTOPIA BUS SWITCHING
REVISION NUMBER: 1
ENGINEER: PMC-SIERRA RS
PAGE:7 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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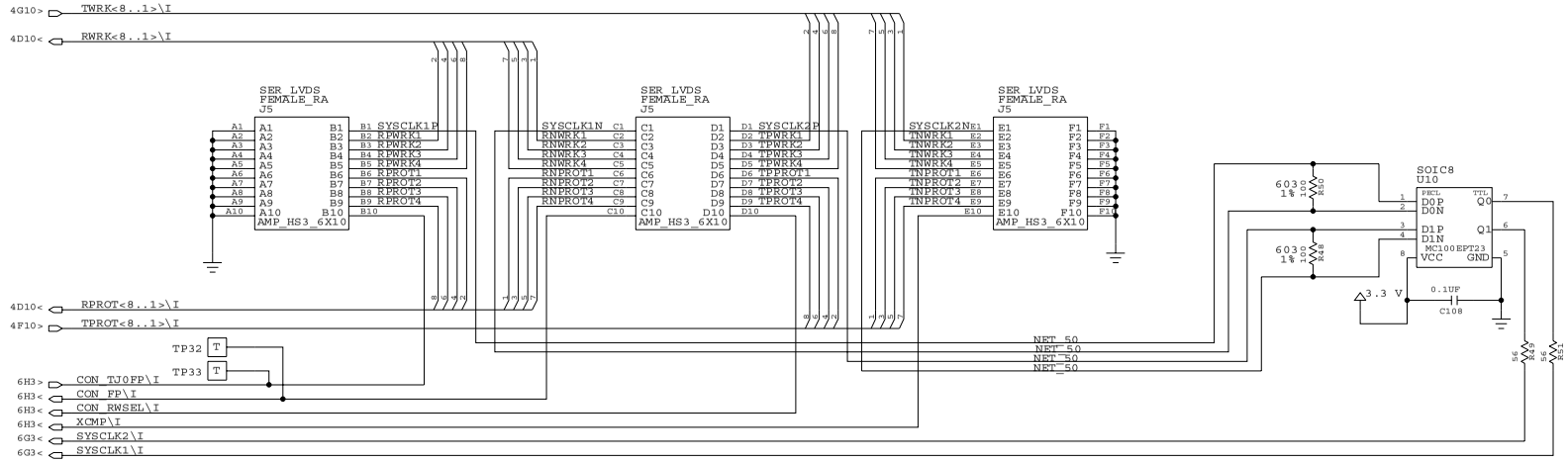
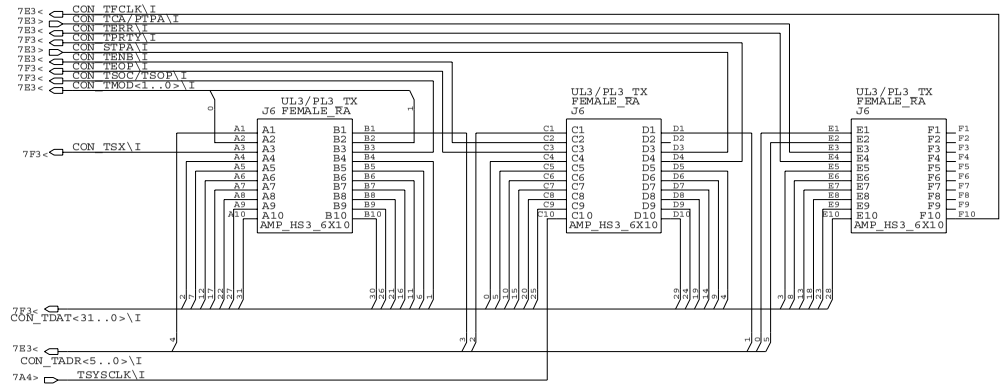
LAST_MODIFIED=Tue Feb 13 09:51:48 2001

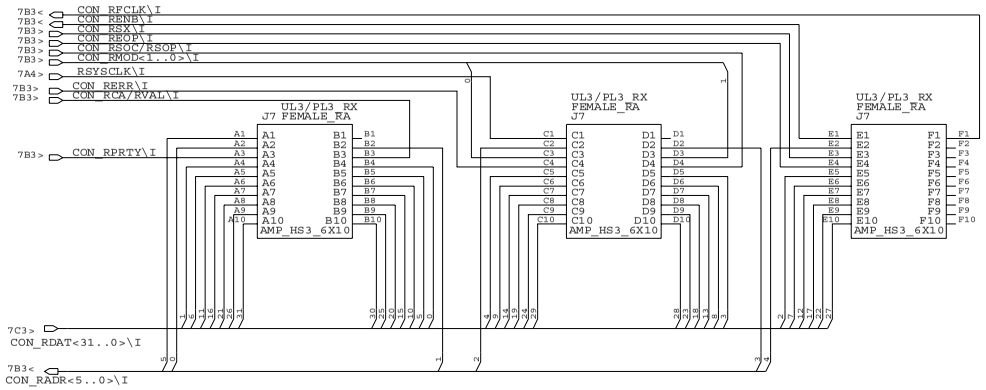
PMC-Sierra, Inc.

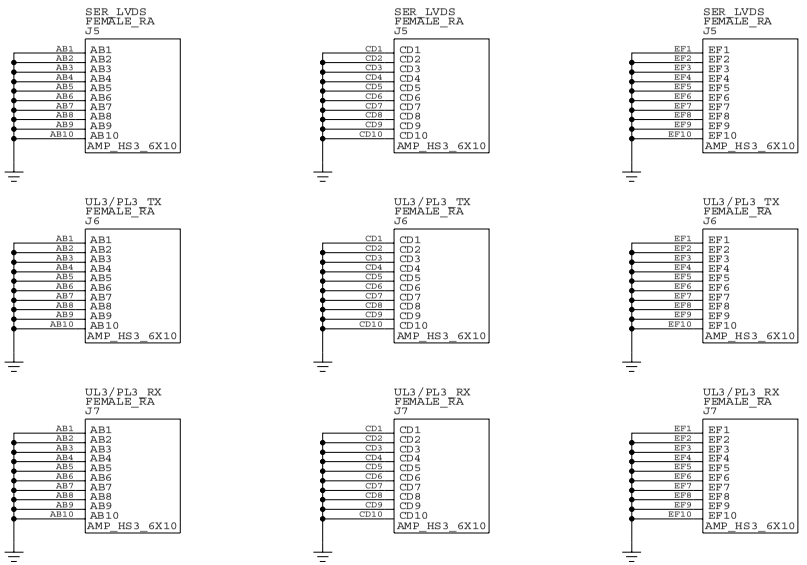
DOCUMENT NUMBER: PMC-2000207 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/27
TITLE: S/UNI MACH48 REFERENCE DESIGN FPGA PROGRAMMING	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA RS	PAGE:8 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR









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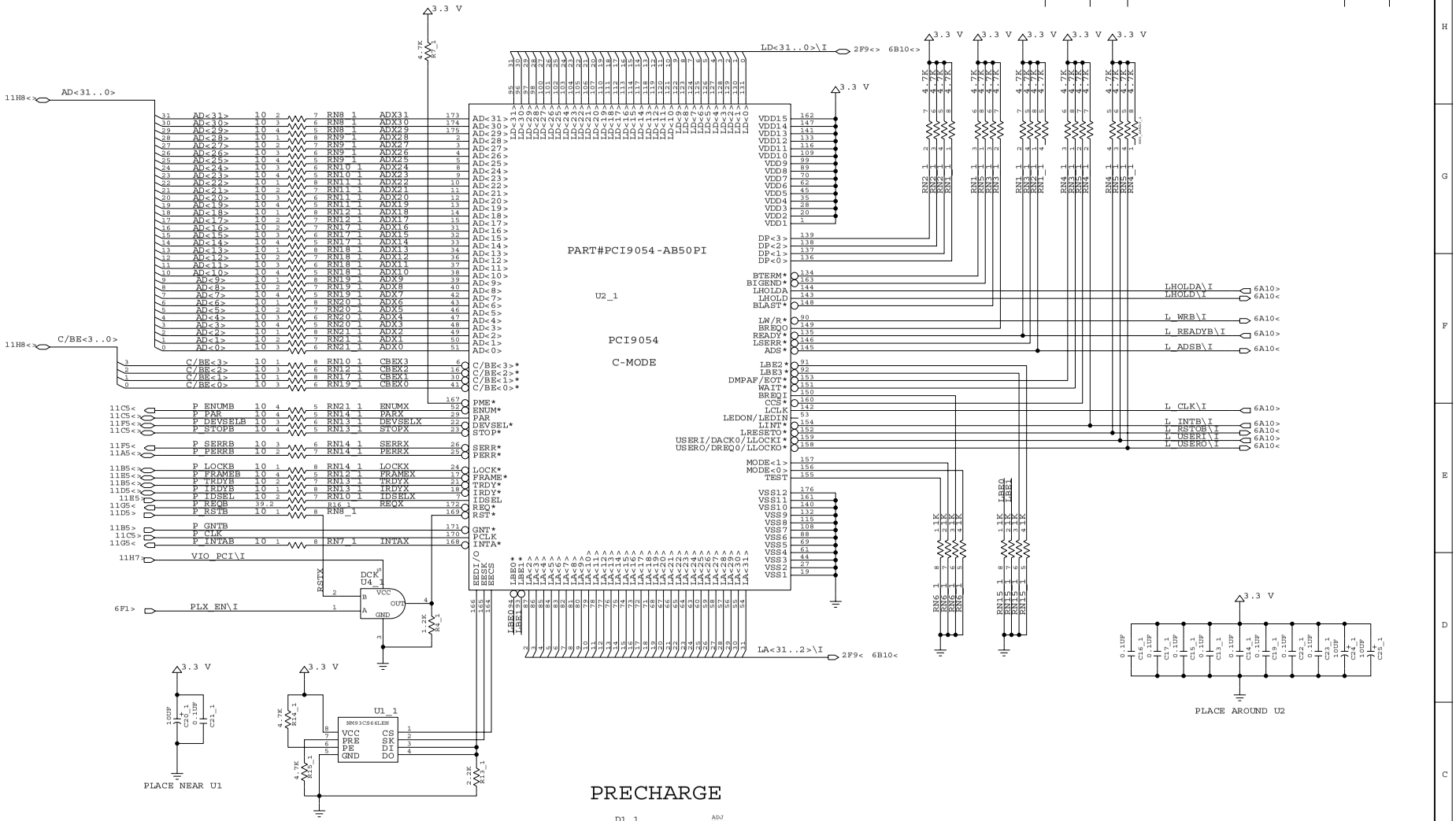
LAST_MODIFIED=Tue Feb 13 09:51:30 2001

PMC-Sierra, Inc.

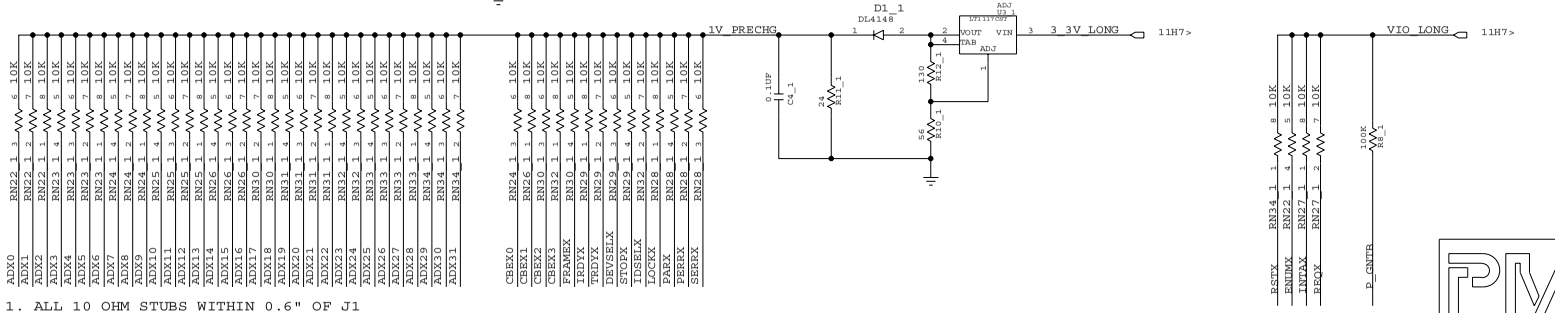
DOCUMENT NUMBER: PMC-2000207 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 00/06/27
TITLE: S/UNI MACH48 REFERENCE DESIGN SYSTEM INTERFACE	REVISION NUMBER: 1
ENGINEER: RS	PAGE:9 OF 12

CPCI BRIDGE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



PRECHARGE



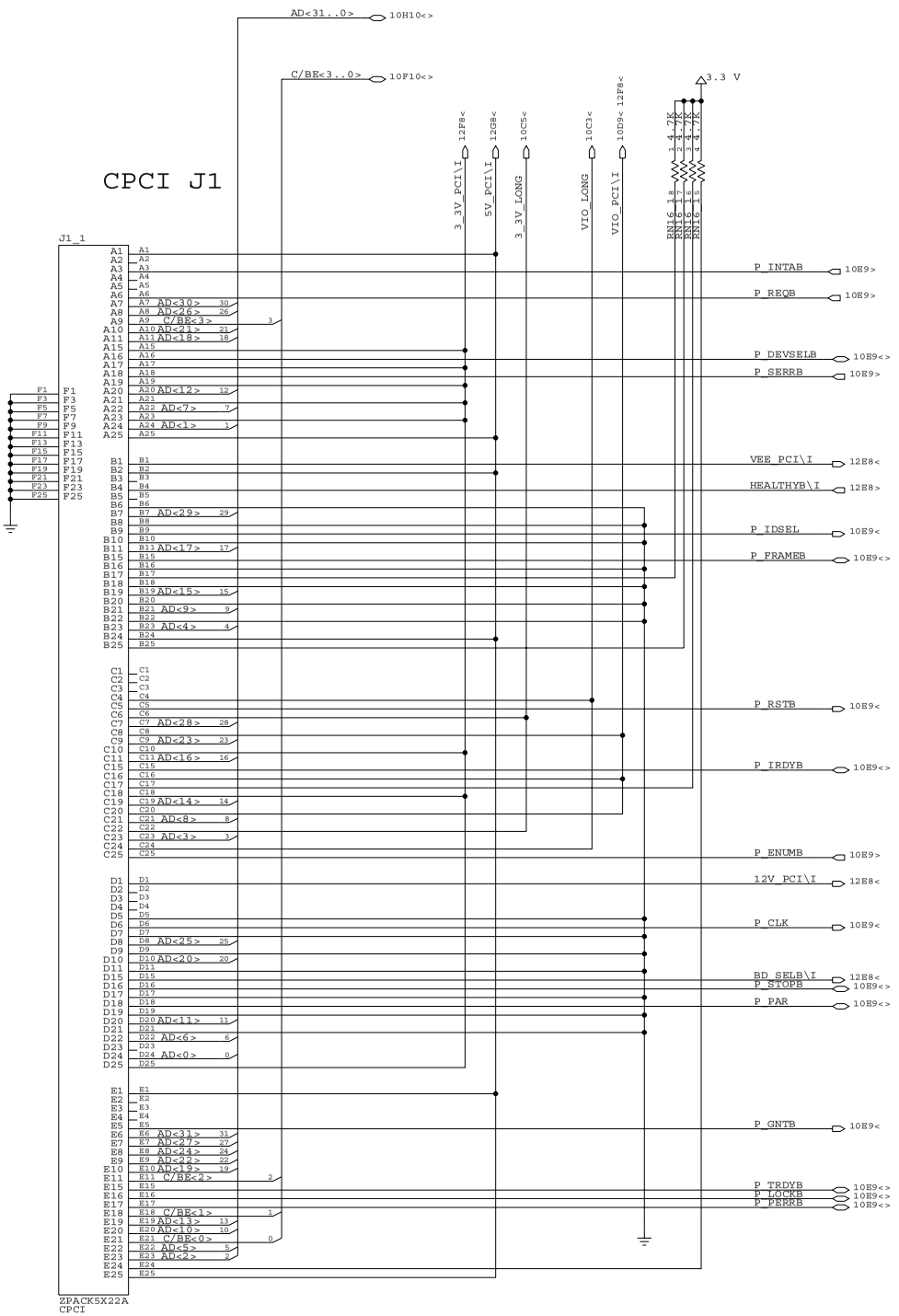
NOTES:
1. ALL 10 OHM STUBS WITHIN 0.6" OF J1
2. ALL PCI SIGNAL TRACES < 1.5" EXCEPT P_CLK
3. P_CLK TRACE MUST BE 2.5" +/- 0.1"
4. CPCI BUS TRACES ARE 65 OHM.
5. 39 OHM STUB RESISTOR ON REQB PLACED NEAR BRIDGE PIN

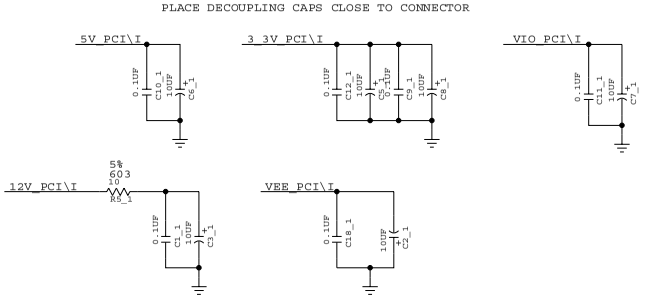
DRAWING:
TITLE=CPCI_BLOCK
ABBREV=CPCI_BLOCK
LAST_MODIFIED=Tue Feb 13 09:51:20 2001

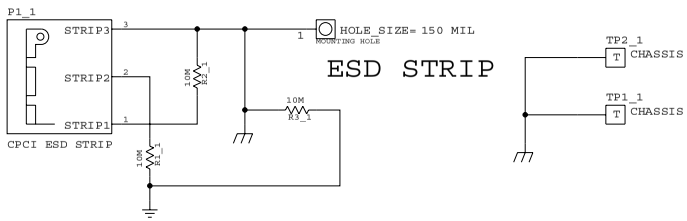
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000207 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 00/06/27
TITLE: S/UNI MACH48 REFERENCE DESIGN CPCI_BLOCK	REVISION NUMBER: 1
ENGINEER: RS	PAGE:10 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







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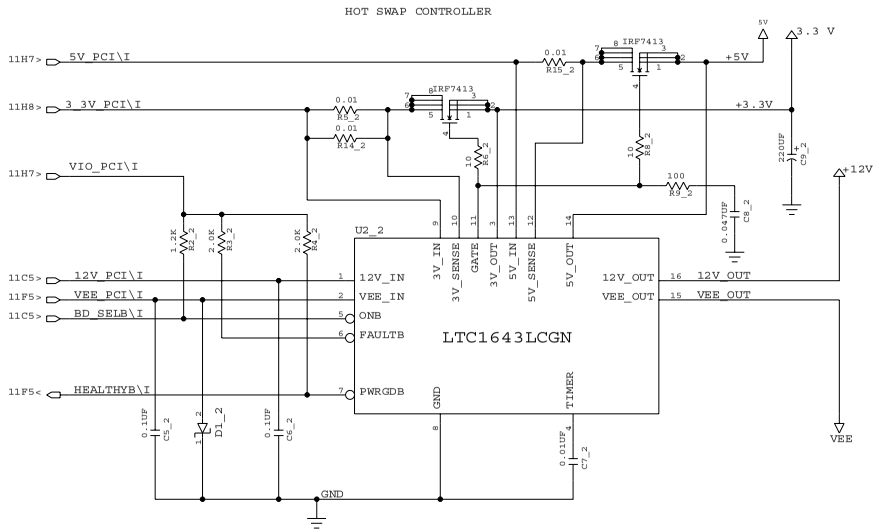
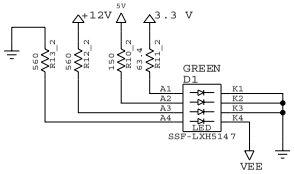
TITLE=CPCI_BLOCK
ABBREV=CPCI_BLOCK
LAST_MODIFIED=Tue Feb 13 09:51:24 2001

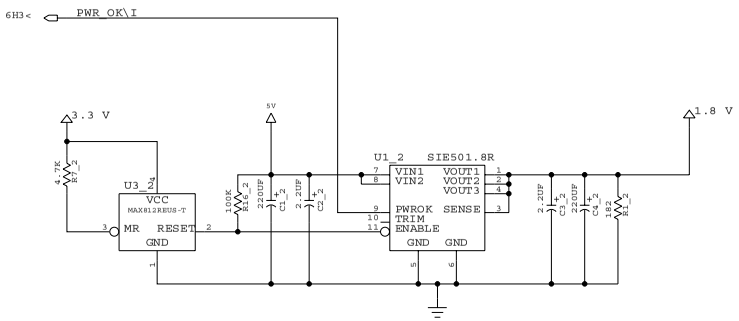
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000207 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 00/06/27
TITLE: S/UNI MACH48 REFERENCE DESIGN CPCI CONNECTOR	REVISION NUMBER: 1
ENGINEER: RS	PAGE:11 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







DRAWING:
TITLE=POWER_BLOCK
ABBREV=PCIPWRBLOCK
LAST_MODIFIED=Tue Feb 13 09:51:26 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000207 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/27
TITLE: S/UNI MACH48 REFERENCE DESIGN POWER BLOCK	REVISION NUMBER: 1
ENGINEER: RS	PAGE:12 OF 12

10 LAYOUT

11 BILL OF MATERIALS

Table 6 Bill of Materials

NO.	Part Number	Manufacturer	Ref Des	Description	Qty
1	PI49FCT3807DQ	PERICOM	U23	IC 3.3V 1:10 CMOS CLOCK DRIVER QSOP20 D GRADE	1
2	SN74AHC1G08DCKR	TI	U4_1	IC SINGLE 2-INPUT POSITIVE AND GATE	1
3	120673-1	AMP	J5-J7	Z-PACK 6 ROW HS3 BACKPLANE CONNECTOR, RIGHT ANGLE RECEPTACLE	3
4	ECU-V1H103KBV	PANASONIC	C7_2	CAP CERAMIC X7R 0603 50V 0.01UF	1
5	ECU-V1H473KBW	PANASONIC	C8_2	CAP CERAMIC X7R 1206 50V 0.047UF	1
6	ECJ-1VB1C104K	PANASONIC	C1, C10_1, C11_1, C12_1, C13_1, C14_1, C15_1, C16_1, C17_1, C18_1, C19_1, C1_1, C21_1, C22_1, C23_1, C3, C28, C32-C34, C36-C38, C40, C43-C49, C4_1, C50-C59, C5_2, C60-C69, C6_2, C70-C103, C108, C112, C114-C123, C137-C152, C155, C9_1	CAP CERAMIC X7R 0603 16V 0.1UF	118
7	GRM42-2X5R106K10	MURATA	C2	CAP CERAMIC X5R 1210 10V 10UF	1
8	ECS-H1CC106R	PANASONIC	C20_1, C24_1, C25_1, C2_1, C3_1, C5_1, C6_1, C7_1, C8_1	CAP TANCAPC 16V 20% 10UF	9
9	ECS-T0JY106R	PANASONIC	C29, C30, C35, C107, C109-C111, C124-C136, C153	CAP TANCAPA 6.3V 20% 10UF	21
10	ECS-H1VC225R	PANASONIC	C2_2, C3_2	CAP TANCAPC 35V 20% 2.2UF	2
11	ECE-V1AA221P	PANASONIC	C1_2, C4_2, C9_2	CAP ELECTRO VA SMD 10V 20% 220UF	3
12	DL4148MS	MICROSEMI	D1_1	DIODE RECT 150MA 75V SMT MINIMELF	1
13	PZC36SAAN	SULLINS ELECTRONICS	J1, J3, J12	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	3
14	PZC36DAAN	SULLINS	J2	CONN HEADER 2 ROW 0.1"X0.1" 2X16	1

NO.	Part Number	Manufacturer	Ref Des	Description	Qty
15	PZC36DAAN	SULLINS ELECTRONICS	J13	CONN HEADER STRAIGHT 6POS MALE .1" DUAL ROW 3X2	1
16	S1011-36-ND	SULLIN	J8	HEADER 8 POS 1 ROW 100 MIL SPACING	1
17	IRF7413	INTERNATIONA L RECTIFIER	Q1_2, Q2_2	IC POWER MOSFET	2
18	LM1085IS-ADJ	NATIONAL SEMI	U14	REGULATOR VARIABLE MICROPOWER LOW DROPOUT ADJUSTABLE	1
19	LT1117CST	LINEAR TECHNOLOGIES	U3_1	REGULATOR ADJUSTABLE SOT223 800MA OUTPUT	1
20	LTC1643LCGN	LINEAR TECHNOLOGY	U2_2	IC CPCI HOT SWAP CONTROLLER	1
21	PM7390	PMC-SIERRA	U7	MULTI SERVICE ACCESS DEVICE FOR CHANNELIZED INTERFACES	1
22	MAX812REUS-T	MAXIM	U3_2	IC VOLTAGE MONITOR WITH MANUAL RESET INPUT 2.63V SOT143	1
23	MB3100H-77.76MHZ	MMD COMPONENTS	Y1	OSC HCMOS/TTL HALF SIZE 8 PIN 77.76MHZ 100PPM	1
24	MC100EPT23D	MOTOROLA	U10	IC DUAL PECL/TTL TRNSLTR. 3.3V, SOIC8	1
25	614-93-308-31-012	MILL MAX	U1_1	SOCKET FOR PART# NM93CS66LEN	1
26	MMD MB3100HH-100.000M HZ	?	U20	<PLEASE USE FROM APPS.LIB LIBRARY OSC_CMOS_BETA>	1
27	EP2645TTS-44.736M	ECLIPTEK	Y2	OSCILLATOR, 44.736MHZ, 3.3V, 50PPM	1
28	DIGIKEY -- CKN4002-ND	?	SW1	RIGHT ANGLE PCB MOUNT SPST PUSH BUTTOM	1
29	PCI9054-AB50PI	PLX TECHNOLOGY	U2_1	IC PCI-TO-LOCAL BUS	1
30	PI3C16212	PEROCOM	U2-U6, U8, U13, U15	IC 3.3V, HIGH BANDWITH, 24 BIT BUS EXCHANGE SWITCH	8
31	QS4A201Q	IDT/QUALITY	U1	IC TWO-BY-TWO ANALOG CROSS POINT SWITCH	1
32	ERJ-6GEY0R00V	PANASONIC	R30-R32, R36	RES 0805 1/10W 5% ZERO OHM	4
33	WSL2512-R01-1	VISHAY	R14_2, R15_2, R5_2	RES 2512 1W 1% 0.01 OHM	3
34	ERJ-3GSYJ122V	PANASONIC	R2_2, R3, R4_1	RES 0603 1/16W 5% 1.2K OHM	3
35	ERJ-3GSYJ100V	PANASONIC	R5_1, R6_2, R8_2	RES 0603 1/16W 5% 10 OHM	3
36	ERJ-3EKF1000V	PANASONIC	R37, R48, R50, R9_2	RES 0603 1/16W 1% 100 OHM	4

NO.	Part Number	Manufacturer	Ref Des	Description	Qty
37	ERJ-3GSYJ104V	PANASONIC	R16_2, R8_1	RES 0603 1/16W 5% 100K OHM	2
38	ERJ-8GEYJ106V	PANASONIC	R1_1, R2_1, R3_1	RES 1206 1/8W 5% 10M OHM	3
39	ERJ-3EKF1300V	PANASONIC	R12_1	RES 0603 1/16W 1% 130 OHM	1
40	ERJ-3GSYJ151V	PANASONIC	R10_2	RES 0603 1/16W 5% 150 OHM	1
41	ERJ-3EKF1820V	PANASONIC	R1_2	RES 0603 1/16W 1% 182 OHM	1
42	ERJ-3GSYJ202V	PANASONIC	R3_2, R4_2	RES 0603 1/16W 5% 2.0K OHM	2
43	ERJ-3GSYJ222V	PANASONIC	R13_1	RES 0603 1/16W 5% 2.2K OHM	1
44	ERJ-6GEYJ240V	PANASONIC	R11_1	RES 0805 1/10W 5% 24 OHM	1
45	ERJ-3EKF3161V	PANASONIC	R34	RES 0603 1/16W 1% 3.16K OHM	1
46	ERJ-3GSYJ330V	PANASONIC	R1, R40, R41, R43, R62, R118	RES 0603 1/16W 5% 33 OHM	6
47	ERJ-3EKF39R2V	PANASONIC	R16_1	RES 0603 1/16W 1% 39.2 OHM	1
48	ERJ-3GSYJ472V	PANASONIC	R14_1, R15_1, R2, R29, R35, R38, R39, R42, R45-R47, R52, R53, R55-R57, R60, R61, R7_1, R7_2, R82-R84, R122-R125	RES 0603 1/16W 5% 4.7K OHM	27
49	ERJ-3GSYJ560V	PANASONIC	R10_1, R49, R51	RES 0603 1/16W 5% 56 OHM	3
50	ERJ-3GSYJ561V	PANASONIC	R12_2, R13_2	RES 0603 1/16W 5% 560 OHM	2
51	ERJ-3EKF63R4V	PANASONIC	R11_2	RES 0603 1/16W 1% 63.4 OHM	1
52	DIGI-KEY -- P<VALUE>CCT-ND	?	R33	?	1
53	PANASONIC -- EXB-V8V100JV	?	RN10_1, RN11_1, RN12_1, RN13_1, RN14_1, RN17_1, RN18_1, RN19_1, RN20_1, RN21_1, RN7_1, RN8_1, RN9_1	?	13
54	PANASONIC -- EXB-V8V101JV	?	RN87, RN115	?	2
55	PANASONIC -- EXB-V8V103JV	?	RN22_1, RN23_1, RN24_1, RN25_1, RN26_1, RN27_1, RN28_1, RN29_1, RN30_1, RN31_1, RN32_1, RN33_1, RN34_1	?	13

NO.	Part Number	Manufacturer	Ref Des	Description	Qty
56	PANASONIC -- EXB-V8V102JV	?	RN15_1, RN6_1	?	2
57	PANASONIC -- EXB-V8V330JV	?	RN35-RN58, RN60-RN63, RN95, RN96, RN103	?	31
58	PANASONIC -- EXB-V8V472JV	?	RN16_1, RN1_1, RN2_1, RN3_1, RN4_1, RN59, RN5_1, RN76-RN85, RN104-RN11 4	?	28
59	SIE501.8R	IPD CONVERTERS	U1_2	REGULATOR 5.0V TO 1.8V 6A, 100MV MAX RIPPLE CONVERTER	1
60	SSF-LXH5147LGD	LUMEX	D1, D3	LED QUAD GREEN HORIZONTAL	2
61	SSF-LXH5147LID	LUMEX	D2	LED QUAD RED HORIZONTAL	1
62	N/A	N/A	TP1-TP19, TP1_1, TP20-TP29, TP2_1, TP30-TP33	CONNECTOR HEADER STRAIGHT SINGLE .1"	35
63	540-99-020-17-400 000	MILL MAX MANUFACTURING	U9, U12	SOCKET FOR IC XC1701L_PC20C	2
64	XC4036XLA-08HQ240	XILINX	U11	USE FROM APPS_LIB LIBRARY	1
65	ZM4742A	DIODES INC	D1_2	ZENER DIODE 12.0V 5% 1.0W SURFACE MOUNT	1
66	352068-1	AMP	J1_1	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	1

NOTES

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