PM5357

S/UNI-622-POS

SATURN USER NETWORK INTERFACE (622-POS)

REFERENCE DESIGN ERRATA

ISSUE 1: DECEMBER 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	December, 2000	This document contains errata information corresponding to the issue 2 of Reference Design document PMC-1981070. This fixes minor documentation errors, improvements and application hints.

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1 ISSUE 1 ERRATA

This issue 1 contains errata applied to the Issue 2 PMC-1981070, S/UNI-622-POS Reference Design. The issue 2 Reference Design and issue 1 errata supersede all prior editions and versions.

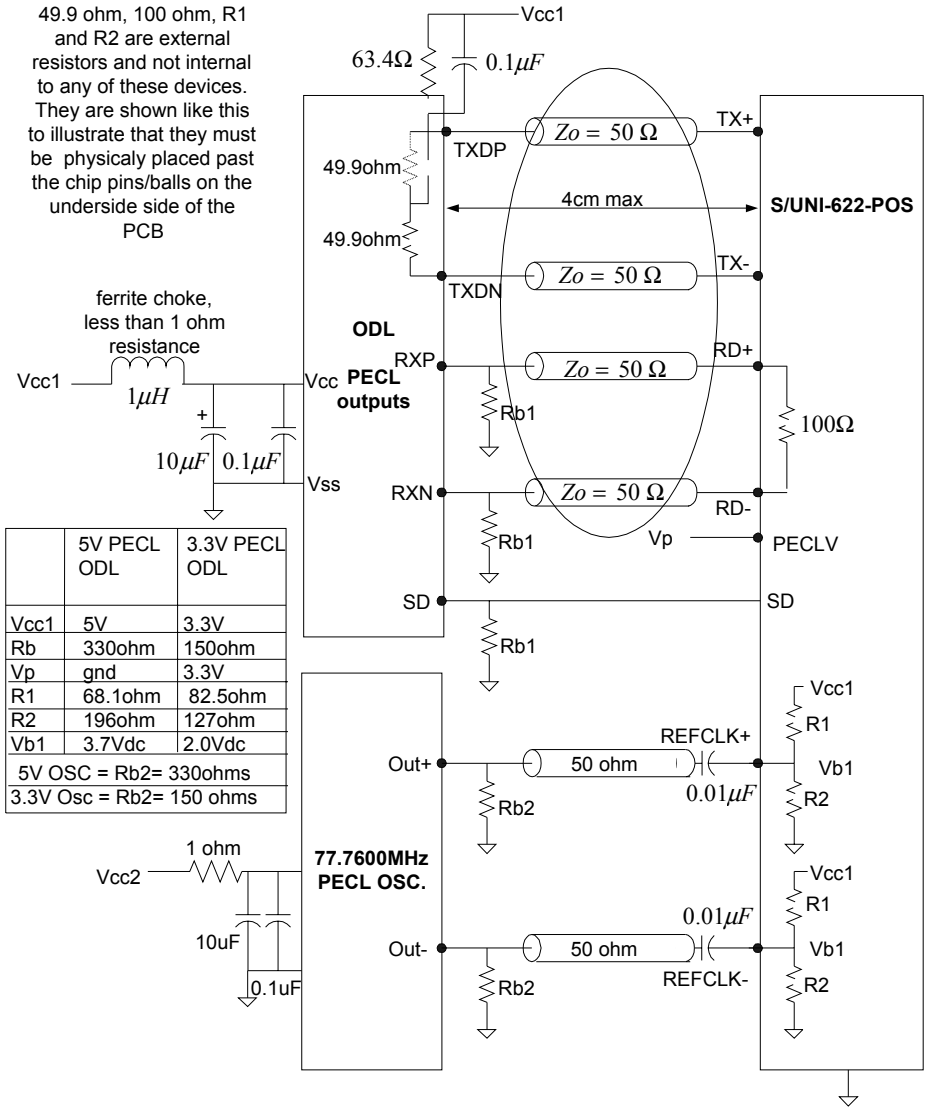
2 REFERENCE DESIGN DOCUMENTATION DISCREPANCIES:

2.1 Trace Impedance should be 50Ohms not 100 ohms in Figure 16

The controlled trace impedance for the RXD+/- and TXD+/- were wrongly labeled as being 100 ohms each in Figure 16 of the reference design document. In Figure 1: Trace Impedance Correction, the circled traces are shown correctly as being 50 ohms each (100 ohms differential).

Figure 1: Trace Impedance Correction

Figure 16: Mixing PECL 5V and 3.3V ODL and 77MHz Oscillator



	5V PECL ODL	3.3V PECL ODL
Vcc1	5V	3.3V
Rb	330ohm	150ohm
Vp	gnd	3.3V
R1	68.1ohm	82.5ohm
R2	196ohm	127ohm
Vb1	3.7Vdc	2.0Vdc
5V OSC = Rb2= 330ohms		
3.3V Osc = Rb2= 150 ohms		

2.2 Change the 5V 77.76MHz Oscillator to a low Jitter type

In section 16, Rev 3 BOM (Bill of Materials), page 2, under item OSC_PECL_77.76MHZ., 200ppm, column Manufacturer, remove the 5V type Saronix 99T27M. In it's place, insert (add) the following low jitter oscillator:

Saronix PECL SONET oscillator with low jitter output, (3.5ps rms and 1ps cycle to cycle). Series SEL2400/SEL3400.

PECL3401AA-77.76 77.76 MHz, 20ppm, 0-70 C, 5V (for WAN applications)

PECL3401B-77.76 77.76 MHz, 50ppm, 0-70 C, 5V (for LAN applications)

2.3 C47 clarification in the BOM

C47 in the BOM on page 1 of section 16 is listed as a 0.1uF X7R. It should be listed as a 10uF, 10V Tantalum.

2.4 Vcc to XC1701L should be 3.3 V and not 5V

The XC1701L PROMS on page 6 of 8 of Revision 3 schematics are 3.3V type and they are connected to a 3.3V FPGA. VCC of U9, U12, U16, and U17 should be connected to 3.3VD and not to Vcc as shown. Also, R1, R2 and C1on this page should be connected to 3.3VD and not Vcc

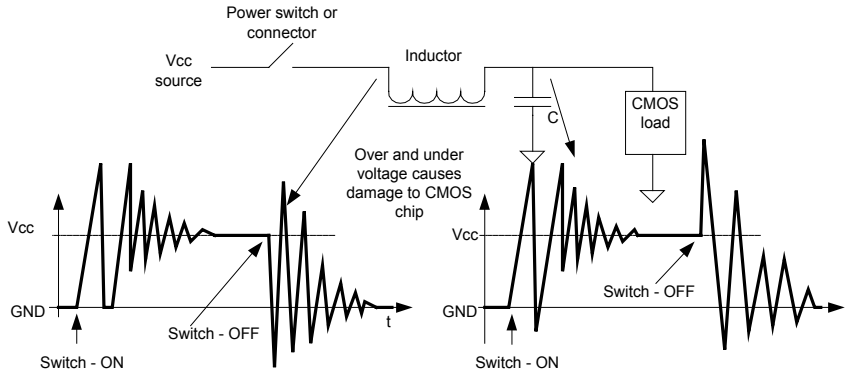
3 APPLICATION NOTES:

3.1 Caution on using Inductors to filter power supplies.

Sometimes inductors are used to filter power supplies to CMOS semiconductors and to reduce currents in hot-card insert applications. In such cases, care must be exercised to prevent damage to CMOS IC's. When power is applied to LC circuits, the ringing at the load and line side can cause voltages that exceed the chips maximum ranges and cause permanent damage to the device. Also on power down, such as hot card insertion and extraction, the voltage spikes induced by the inductor can cause permanent device damage and cause sparking at the connector/switch thus reducing component life. See figures below for more detail.

Because the LC forms a tank circuit, the resultant ringing voltage could be greater than Vcc and lower than ground on both sides of the inductor as shown in Figure 2: Inductor Transients may damage CMOS circuits.

Figure 2: Inductor Transients may damage CMOS circuits

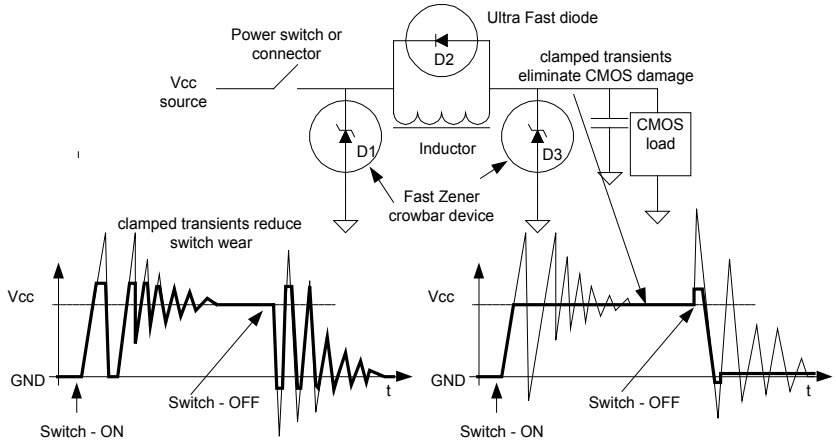


In Figure 2: Inductor Transients may damage CMOS circuits, D2 acts to commute the inductor voltage generated when power is abruptly removed from the primary side of the inductor. The voltage across the inductor is clamped by D2 to max 0.7V in the reverse direction.

D1 acts to prevent the primary side from high voltages which may cause arcing across the switch.

D3 acts to prevent the secondary side from over voltage by clamping action of the zener type device. Also, the under voltage is clamped to –0.7 V.

Figure 3: Inductor Transients Clamped by Diodes



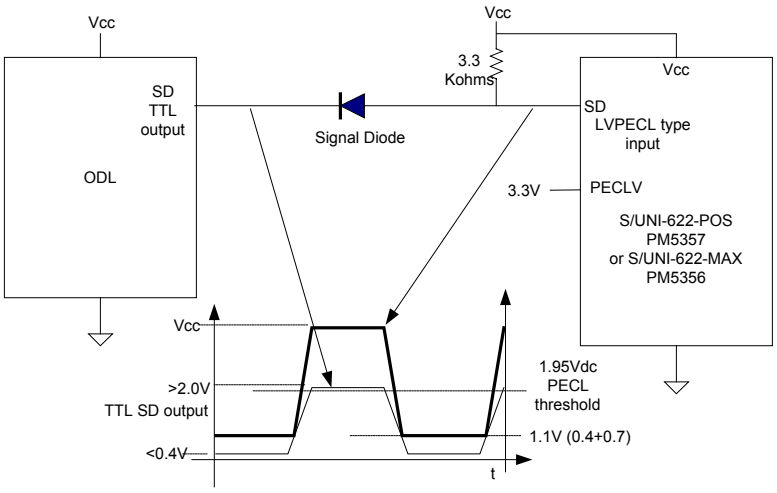
3.2 Connecting a TTL SD from ODL to SD PECL type input of S/UNI-622-POS

The SD input of the POS has a much bigger dynamic range than the standard true PECL receiver. Also the SD signal switches so infrequently that it can be considered as a DC signal. The figure below shows how to connect a TTL level signal to a single ended PECL input using a standard signal diode and a pullup resistor. TTL outputs typically are less than 0.4V for a low and more than 2.0V for a logic high. TTL drivers can sink a lot more current than they can source.

When the ODL's TTL SD output is low (<0.4V), current is drawn through the 3.3K resistor and the diode is forward biased. The voltage on the anode side of the diode now will be less than 1.1V (ground plus 0.4V plus the diode drop of 0.7 V). A 1.1V is lower than the 1.95V LVPECL threshold and will be recognized as a low.

When the TTL SD output switches high, theoretically its output will be greater than 2.4 V. The diode will be off and the voltage on the anode side of the diode will be higher than 2.4V+0.7V = 3.1V which is well above than 1.95V required for a LVPECL high.

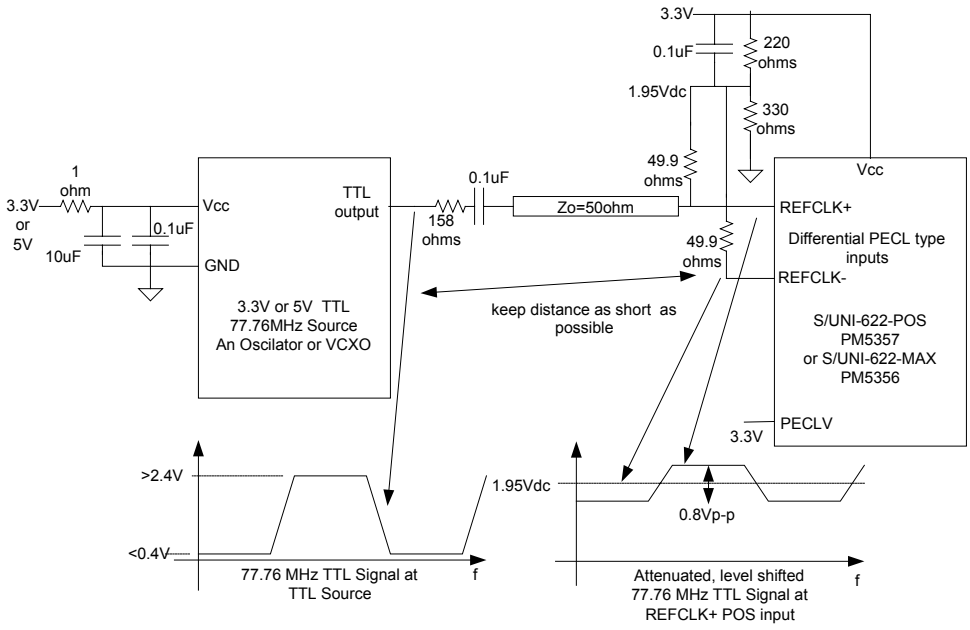
Figure 4: TTL to PECL SD input of S/UNI-622-POS



3.3 Interfacing a TTL single ended 77.76MHz Oscillator Interface to REFCLK+/- PECL inputs

In some cases, a PECL oscillator or VCXO may be substituted for a cheaper TTL type. The circuit below will interface a single ended TTL signal to the PECL-like inputs of the S/UNI's differential REFCLK+/- inputs. Filter the power supply well to the TTL clock source as any power supply noise may frequency modulate the output. Depending on the current draw, use a small 1 ohm resistor to keep the voltage drop (IR) across the resistor as low as possible.

Figure 5: TTL to Single ended PECL Interface



The TTL signal has to be attenuated from about 2.4Vdc p-p about to 0.8 Vp-p. This is done as a simple resistor divider using the 158 ohms and 49.9 ohms.

Then we have to ac couple to level shift so that the 0.8V signal is centered around 1.95Vdc, which is the sweet spot of the PECL like differential receivers of the S/UNI device.

The single ended signal is terminated into the 49.9 (50 ohm) resistor to reduce reflections and thus jitter. The REFCLK- input is biased at the mid point of the LVPECL at 1.95 V. So the input at REFCLK+ will swing above and below this voltage at REFCLK-. Do not use a TTL to PECL converter chip as it will generate too much jitter for this application.

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