

The NJ88C33 is a synthesiser circuit fabricated on Zarlink Semiconductor's 1.4 micron CMOS process, assuring very high performance. It is I²C compatible and can also be programmed at up to 5MHz. It contains a 16-bit R counter, a 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for the loop driver to improve control voltage range to the VCO when operating at low supply voltages.

FEATURES

- Easy to Use
- Low Power Consumption (15mW)
- Single Supply 2.5V to 5.5V
- Digital Phase Comparator with Current Source Outputs
- Serial (I²C Compatible) Programming, 5MHz max
- Channel Loading in 8 μ s
- 150MHz Input Frequency Without Prescaler at 4.5V (52MHz at 2.7V)
- Standby Modes
- Use of Two-Modulus Prescaler is Possible

APPLICATIONS

- Cordless Telephones (CT2, DECT)
- Cellular Telephones (GSM, PCN, ETACS)
- Hand Held Marine Radios
- Sonarbuoys
- Video Clock generators

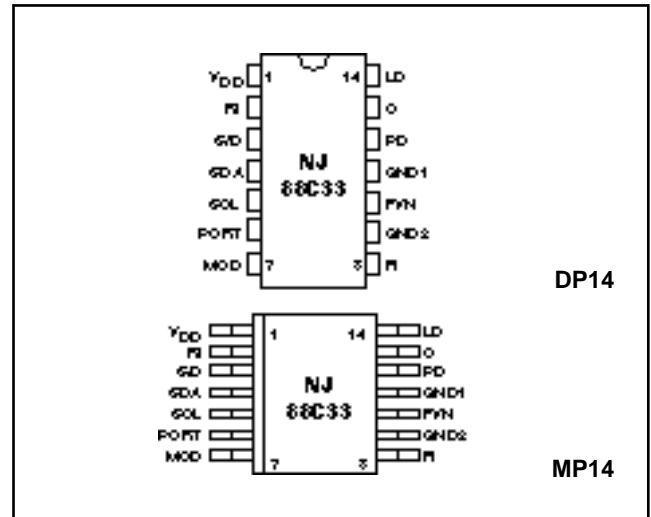


Fig.1 Pin connections (not to scale) - top views

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V to 7V
Input voltage, V_{IM1}	-0.3 to $V_{DD} + 0.3V$
Output voltage on pin 13, V_{IM2}	- V_{DD} to 0V
Storage temperature, T_{stg}	-55°C to +125°C

ORDERING INFORMATION

NJ88C33 MA DP (Industrial - Plastic DIL package)

NJ88C33 MA MP (Industrial - Miniature Plastic DIL package)

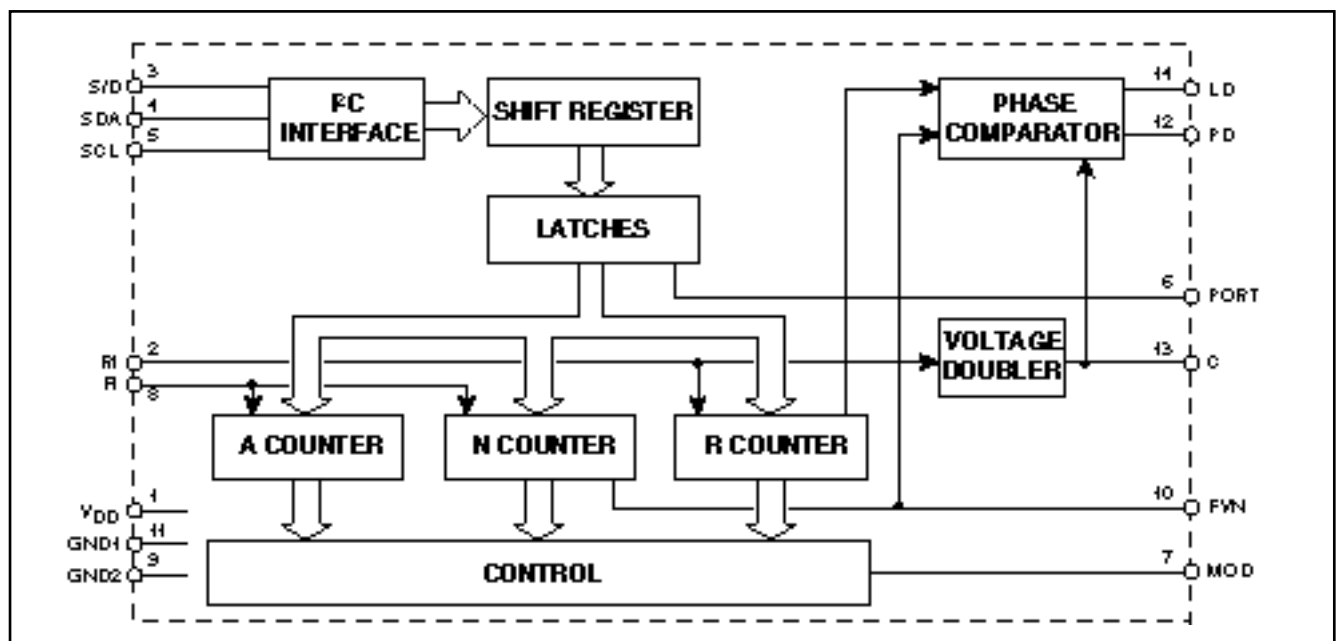


Fig.2 Simplified block diagram of NJ88C33

NJ88C33

PIN DESIGNATIONS

Pin No.	Pin Name	Description
1	V _{DD}	Supply voltage (normally 5V or 3V).
2	RI	Reference frequency input from an accurate source, normally a crystal oscillator. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
3	S/D	Single/dual modulus operating mode selection input. Single modulus operation is selected by driving the pin low. 'High' selects dual modulus mode.
4	SDA	I ² C bus data input pin. It is also an open-drain output for generating I ² C bus acknowledge pulses.
5	SCL	I ² C bus clock input. It can be clocked at up to 5MHz.
6	PORT	Output control pin, which can be programmed via the I ² C bus. It can be connected to the S/D pin to select single or dual modulus mode under bus control.
7	MOD	Modulus control pin. It is high in single modulus mode but switches in dual modulus operation. In dual modulus mode, MOD remains low during operation of the A counter until A=0; MOD then remains high until N=0, when both counters are reloaded. It can be programmed via the I ² C bus as an open-drain or push-pull output.
8	FI	Frequency input from a VCO or prescaler. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
9	GND2	Dedicated ground for the FI input buffer. It should be connected to the VCO ground or the prescaler ground, if used. Any noise on this pin will affect the performance of the VCO loop.
10	FVN	Open-drain output from the N counter.
11	GND1	Ground supply pin (global).
12	PD	Tristate current output from the phase detector. The polarity of the output can be programmed via the I ² C bus.
13	C	Voltage doubler output. The operation of the doubler can be controlled via the I ² C bus. In applications where the voltage doubler is switched off, this pin should be connected to GND1; a reservoir capacitor should be connected from this pin to GND1 for applications where it is switched on.
14	LD	Open-drain lock detect output - requires integration if used.

OPERATING RANGE

Test conditions (unless otherwise stated):

PLL locked, RI = 10MHz

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V _{DD}	2.5	5	5.5	V	FI = 50MHz, V _{FI} = 150mVrms, N,R > 1000 without voltage doubler, V _{DD} = 5V, T _{amb} = 25°C
Ambient temperature	T _{amb}	-40		+85	°C	
Supply current						
Single modulus	I _{DD}		2.1	3.0	mA	
Dual modulus	I _{DD}		2	3.0	mA	
Standby mode	I _{DD}			1	µA	FI = 50MHz, V _{FI} = 150mVrms, preamp off, divider off, V _{DD} = 5V, T _{amb} = 25°C
Standby mode	I _{DD}		1.0	1.5	mA	FI = 50MHz, V _{FI} = 150mVrms, preamp on, divider off, V _{DD} = 5V, T _{amb} = 25°C

Fig.3 Functional block diagram

NJ88C33

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

$$V_{DD} = 4.5V \text{ to } 5.5V, T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$$

INPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signals SDA, SCL, S/D						
Input voltage high	V_{IH}	$0.7V_{DD}$		V_{DD}	V	$V_{IN} = V_{DD} = 5.5V$
Input voltage low	V_{IL}	0		$0.3V_{DD}$	V	
Input capacitance	C_i			10	pF	
Input current	I_{IN}			10	μA	
Input signal RI						
Input frequency	f_{max}	100		52	MHz	Sinewave input Note 1, 2
Input voltage	V_{Irms}				mV	
Input capacitance	C_i			10	pF	$V_{IN} = V_{DD} = 5.5V$
Input current	I_{IN}			10	μA	
Input signal FI						
Input frequency	f_{max}	50		52	MHz	Dual modulus operation Sinewave input Note 1, 2
Input voltage	V_{Irms}				mV	
Input capacitance	C_i			10	pF	$V_{IN} = V_{DD} = 5.5V$
Input current	I_{IN}			10	μA	
Input signal FI						
Input frequency	f_{max}	30		150	MHz	Single modulus operation Sinewave input FI = 0-70MHz Note 1, 2 FI = 70-120MHz Note 1, 2 FI = 120-150MHz Note 1, 2
Input voltage	V_{Irms}				mV	
	V_{Irms}				mV	$V_{IN} = V_{DD} = 5.5V$
	V_{Irms}				mV	
Input capacitance	C_i	100			pF	
Input current	I_{IN}	200			μA	

Note.1Lowest noise floor achieved at 10dB above this level with I²C bus operating. The source impedance should be less than 2k .

Note.2DC coupled input amplitude $V_{IRMS} > 0.8V_{DD}$.

OUTPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Signals SDA, LD						
Output voltage low	V_{OL}			0.4	V	Open drain, $I_{OL} = 3mA$
Output Signal PD						
High current mode (see Fig.4)	I_{HU}	1.9	2.5	3.1	mA	$C_L = 400pF$, tristate output $0 < V_{PD} < 4.5$, $V_{DD} = 5V$, $T = 25^{\circ}C$ Note 1 $0.4 < V_{PD} < 5$, $V_{DD} = 5V$, $T = 25^{\circ}C$ Note 1 $0 < V_{PD} < 4.6$, $V_{DD} = 5V$, $T = 25^{\circ}C$ Note 1 $0.4 < V_{PD} < 5$, $V_{DD} = 5V$, $T = 25^{\circ}C$ Note 1 $T_{amb} = -25^{\circ}C \text{ to } +60^{\circ}C$
Low current mode	I_{LD}	-1.9	-2.5	-3.1	mA	
	I_{LU}	0.475	0.625	0.775	mA	
Tristate	I_{LZ}	-0.475	-0.625	-0.775	mA	
	I_Z		50		nA	
Output Signal FVN						
Output voltage low	V_{OL}			0.4	V	Open drain output $I_{OL} = 1mA$ $C_L = 30pF$
Output low pulse width	t_{WL}			1/FI		
Output Signals MOD, PORT						
Output voltage high	V_{OH}	$V_{DD}-0.4$			V	Push-pull output $I_{OH} = 0.5mA$ $I_{OL} = 0.5mA$
Output voltage low	V_{OL}			0.4	V	
Output Signal LD						
Output voltage low	V_{OL}			0.4	V	Open drain output $I_{OL} = 3mA$, $C_L = 30pF$ Loop locked Loop not locked FVN = FI/N $f_C = RI/R$
Output low pulse width	t_{WL}		10	$1/FVN$ $1/f_C$	ns	

Note.1Temperature coefficient for current is typically $-0.7\%/^{\circ}C$

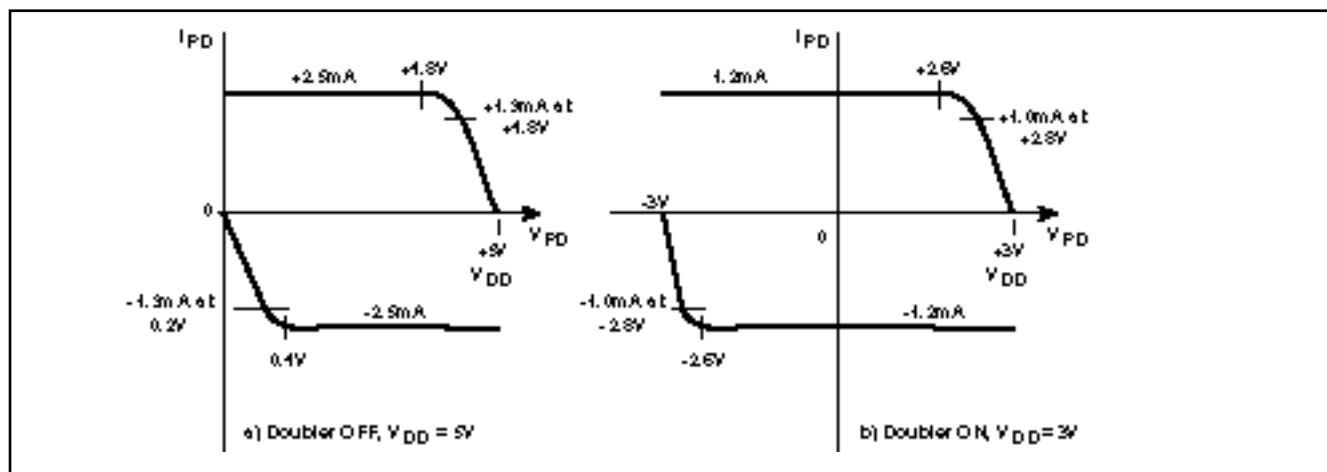


Fig. 4 Typical output signal PD, high current mode

VOLTAGE DOUBLER $V_{DD} = 3V$

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Pin C Output voltage	V_C V_C	$-V_{DD}$ $-V_{DD}$		$-V_{DD} + 0.8V$ $-V_{DD} + 1.5V$	V V	$f_{VD} = 2MHz, I_{OC} = 0\mu A, V_{DD} = 3V$ $f_{VD} = 2MHz, I_{OC} = 100\mu A, V_{DD} = 3V$
Current Consumption	I_D			100	μA	$f_{VD} = 2MHz, I_{OC} = 0\mu A, V_{DD} = 3V$

TIMING INFORMATION

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signal RI Input frequency Input frequency Rise time Fall time Slew rate	f_{max} f_{max} t_R t_F t_F	0 0 3		52 10 1.5 1.5	MHz MHz μs μs V/ μs	$V_{DD} = 2.7V$
Input Signal FI Input frequency Input frequency Rise time Fall time Slew rate	f_{max} f_{max} t_R t_F t_F	0 0 3		52 20 1.5 1.5	MHz MHz μs μs V/ μs	Dual modulus $V_{DD} = 2.7V$
Input Signal FI Input frequency Input frequency Rise time Fall time Slew rate	f_{max} f_{max} t_R t_F t_F	0 0 3		150 52 1.5 1.5	MHz MHz μs μs V/ μs	Single modulus $V_{DD} = 2.7V$
Output Signal PORT Rise time Fall time	t_R t_F			1 1	μs μs	$C_L = 30pF$ $C_L = 30pF$
Output Signal FVN Fall time	t_F		20		ns	$C_L = 30pF$
Output Signal MOD Rise time Fall time Delay time (L H) Delay time (H L)	t_R t_F t_{DLH} t_{DHL}			10 10 15 15	ns ns ns ns	$C_L = 30pF$ $C_L = 30pF$ $C_L = 30pF$ Measured from +Ve edge of FI $C_L = 30pF$ Measured from +Ve edge of FI

PHASE COMPARATOR

The phase comparator produces current pulses of duration equal to the difference in phase between the comparison frequency ($f_c = R1/R$), and f_{VN} , the divided-down VCO frequency ($F1/N$).

When status bit 4 is set high the positive polarity mode of the output PD is selected. When f_c leads f_{VN} the PD output goes high; when f_{VN} leads f_c it goes low. Similarly, selecting the negative polarity mode of PD by programming bit 4 of the status register low causes PD to have the inverse polarity. The loop filter integrates the current pulses to produce a voltage drive to the VCO.

No pulses are produced when locked. The lock detect output, LD, produces a logic '0' pulse equal to the phase difference between f_c and f_{VN} .

When the phase difference between f_c and f_{VN} is too small to be resolved by the phase detector then no current pulses are produced. In this region the loop does not reduce the close-in noise on the VCO output. This can be overcome using a very high value resistor to leak a few nanoAmps of current from the filter and keep the loop on the edge of the region.

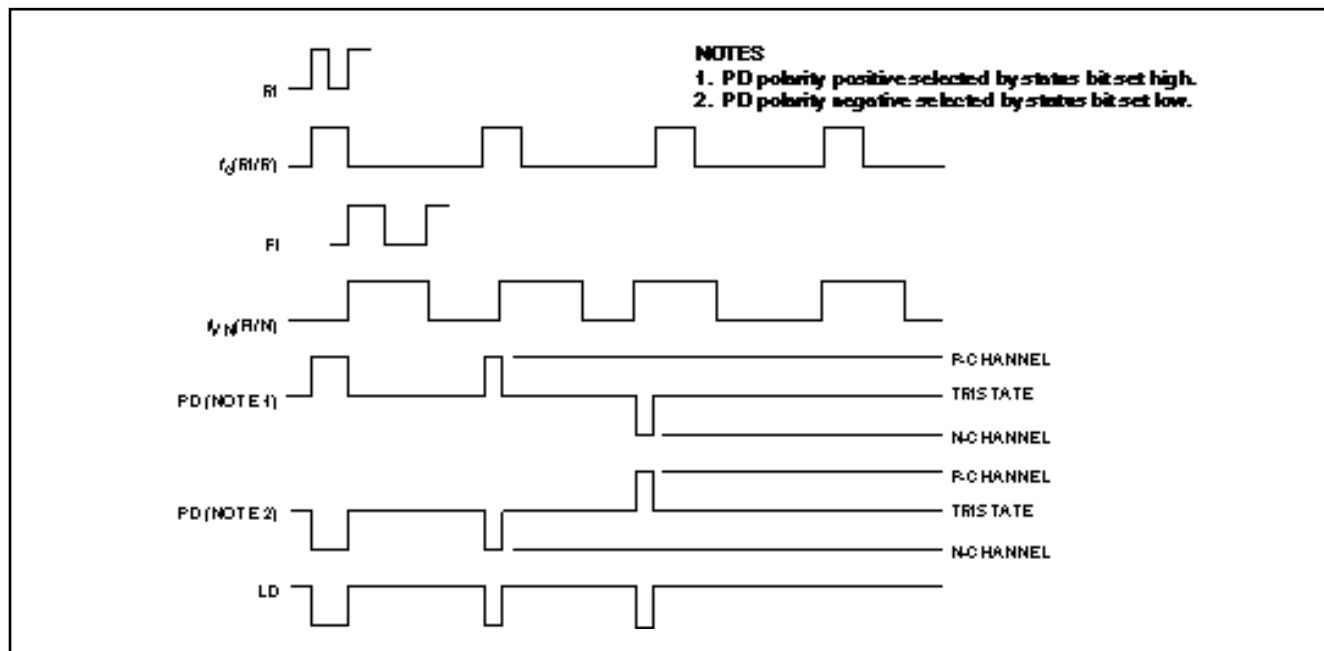


Fig. 5 Phase comparator phase diagram

PROGRAMMING

Transmission Protocol

I²C programming messages consist of an address byte followed by a sub-address byte followed by 1, 2 or 3 bytes of data. Bit 7 of the address byte must match the setting of the S/D pin for the address to be recognised. This allows for separate addressing of two NJ88C33 synthesisers on the same bus. The sub-address should be set to select the correct registers to be programmed and should be followed by the appropriate number of data bytes. Registers are not programmed until the complete message protocol has been checked.

Each message should commence with a START condition and end with a STOP condition unless followed immediately by another transfer, when the STOP condition may be omitted.

Data is transferred from the shift register to the latches on a STOP condition or by a second START condition.

A START condition is indicated by a falling edge on the Serial Data line, SDA, when the Serial Clock line, SCL, is high.

A rising edge on SDA when SCL is high indicates a STOP condition as shown in Fig.6.

Data on SDA is clocked into the NJ88C33 on the rising edge of SCL. The NJ88C33 acknowledges each byte transferred to it by pulling the SDA line low for one cycle of SCL after the last bit has been received.

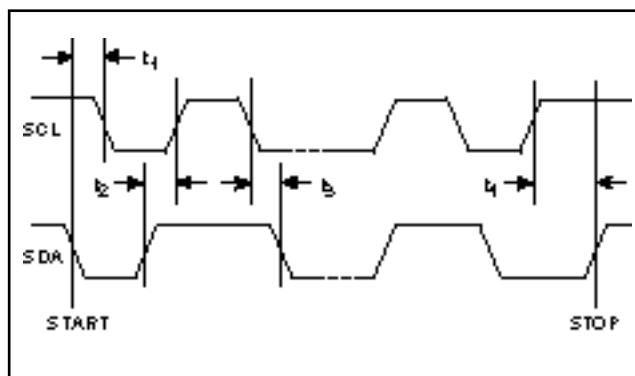


Fig. 6 I²C timing diagram

I2C TIMING INFORMATION

VDD = 4.5V to 5.5V, Tamb = -40°C to +85°C

Parameter	Symbol	Value		Unit
		Min.	Max.	
Serial clock frequency	f_{SCL}		5	MHz
SCL hold after START	t_1	200		ns
Data set-up time	t_2	20		ns
Data hold after SCL low	t_3	0		ns
SCL set-up before STOP	t_4	20		ns

NJ88C33

APPLICATION CIRCUITS

Single Modulus

In this mode, the NJ88C33 synthesiser can be used with or without a fixed modulus prescaler. The R counter is programmed with a value to produce a comparison frequency f_c . When the N counter is changed by 1 the loop is no longer in lock and the phase detector output produces current pulses to bring the loop back into lock. These pulses are integrated by the loop filter to produce the VCO voltage drive. When the VCO loop is locked, $FI/N=f_c$ i.e., the VCO frequency is $N \times f_c$.

Using a prescaler with a division ratio P, the smallest VCO output frequency step is Pf_c and the VCO frequency is PNf_c .

If a low pass filter is connected to the lock detect output as shown and sampled by the microprocessor, the proximity of the synthesiser loop to lock can be evaluated.

The A counter is not used in this mode.

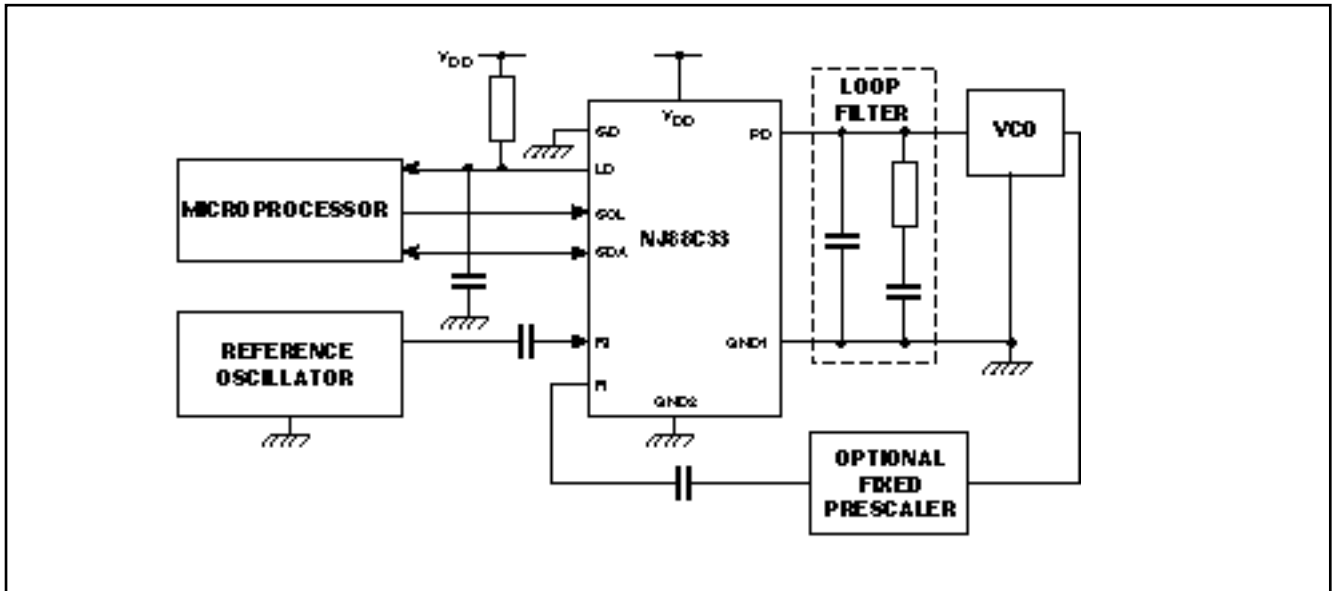


Fig. 7 Single modulus application

Dual Modulus

This mode allows much higher frequencies to be used in conjunction with a prescaler but maintains the step size, f_c . In this mode, a dual modulus prescaler (with ratios P and P + 1) must be used with the NJ88C33. The A counter controls the MOD output, which is used to select the division ratio of the prescaler.

When the A counter is non-zero, the MOD output is low and goes high when the A counter has counted down to zero. MOD remains high until the N counter reaches zero, when both counters are re-loaded. Thus, the prescaler divides by P for N-A cycles and by P + 1 for A cycles of FI. The VCO frequency is given by $PNf_c + Af_c$.

Note that programming A = 0 produces a count of 128 cycles.

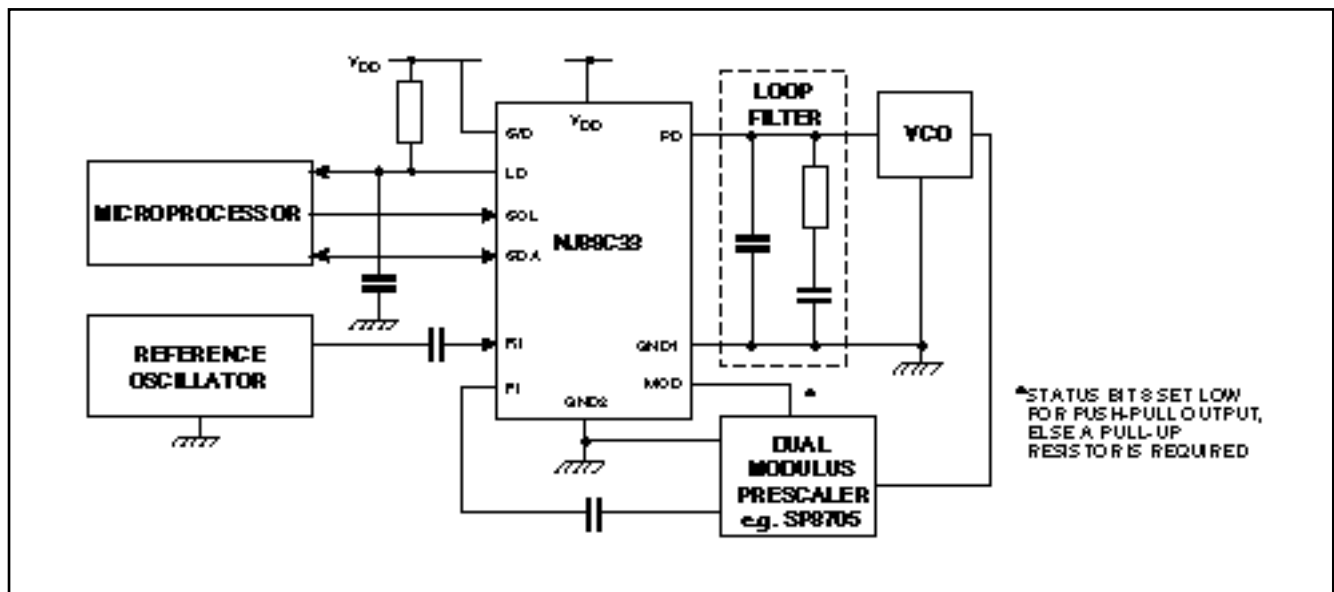


Fig. 8 Dual modulus application

VCO Driving Without Voltage Doubler

To switch off the voltage doubler, bit 7 of the status register is programmed low. This will reduce current consumption and minimise noise. The voltage doubler output C should be connected to GND1 as connection to GND2 would induce noise in the VCO loop.

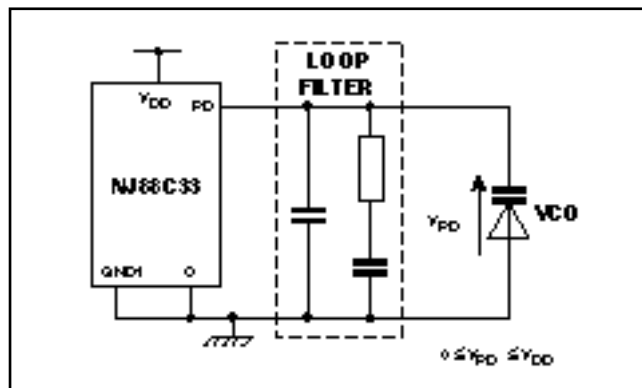


Fig. 9 Driving a VCO without voltage doubler

VCO Driving With Voltage Doubler

The voltage doubler is switched on by setting bit 7 of the status register high. It is recommended that a reservoir capacitor of at least 1μF be connected from C to GND1.

The voltage doubler is designed to boost VCO drive in low voltage applications.

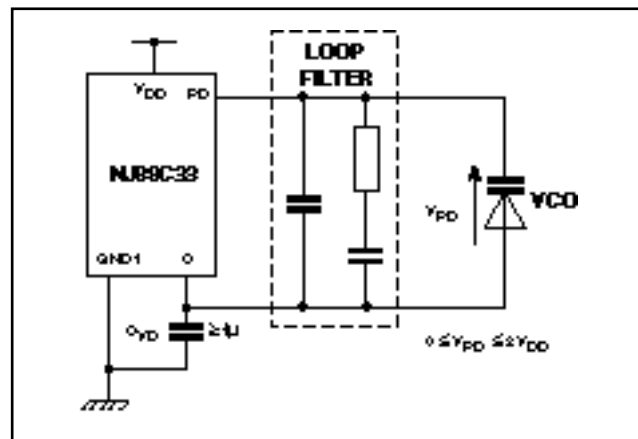


Fig. 10 Driving a VCO using the voltage doubler

Further Applications Information

A stand-alone programmer card and an evaluation board are available for evaluating the NJ88C33. The programmer card allows two sets of variables to be programmed into both the divider and status registers during alternate programming cycles, at either the standard I²C bus rate of 100kHz or at 2MHz.

Initialisation is with either a manual push-button or by an external logic level pulse; a synchronisation output is provided to allow a quick assessment of 'step' and 'settle' responses to be made.

The NJ88C33 evaluation board (Fig. 11) demonstrates the preferred layout technique - providing a reference oscillator, a 60 to 80MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-hopping loops.

Application Note: AN94, 'Using the NJ88C33 PLL Synthesiser' explains the design equations and demonstrates the use of the device, and is available from your local Zarlink Semiconductor customer service centre.

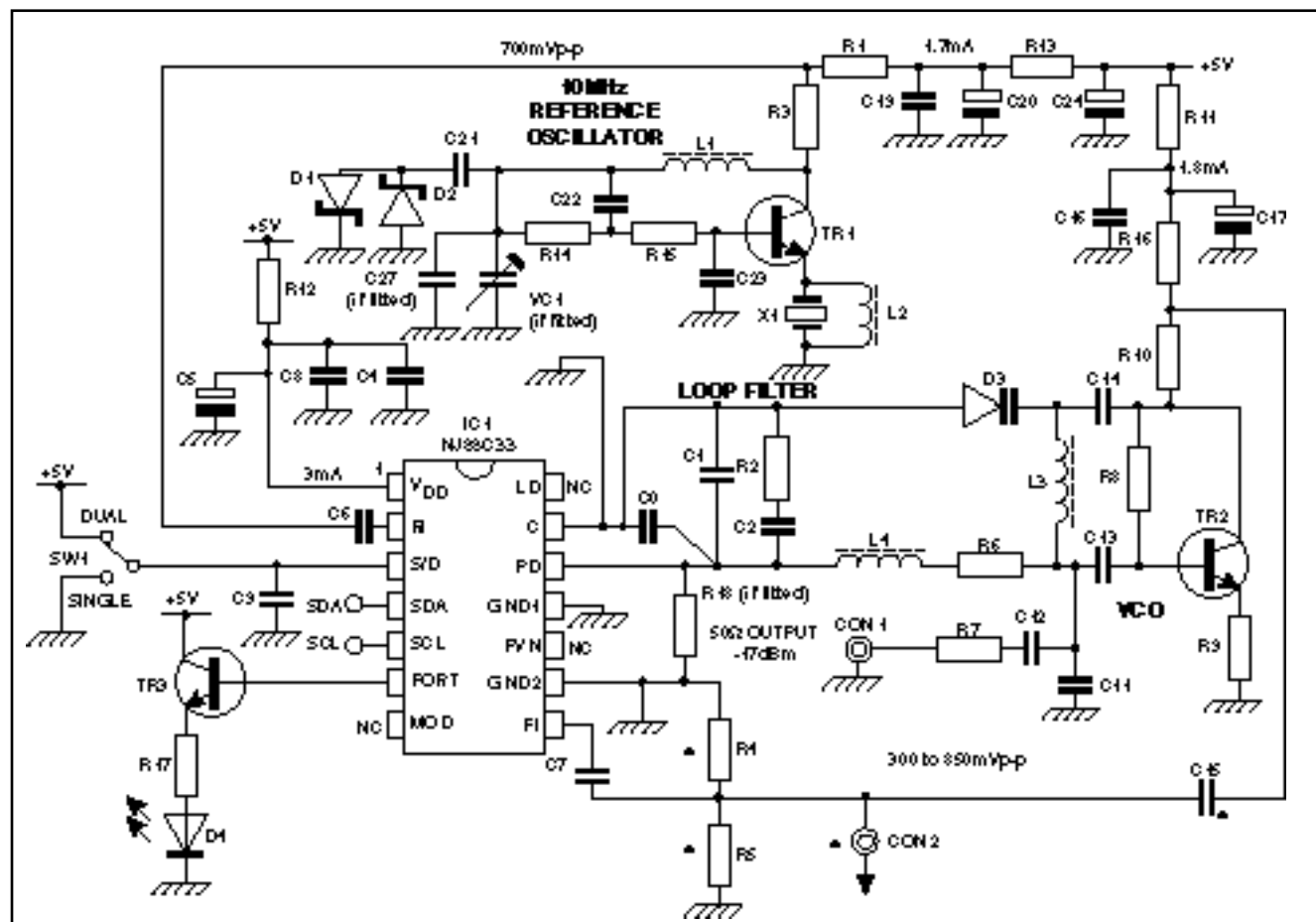


Fig. 11 Typical applications circuit

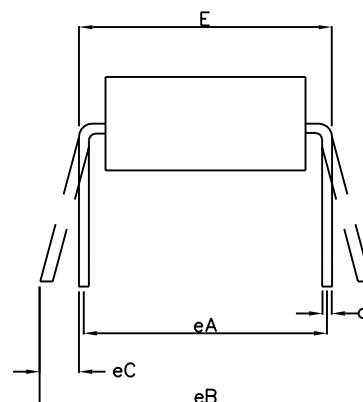
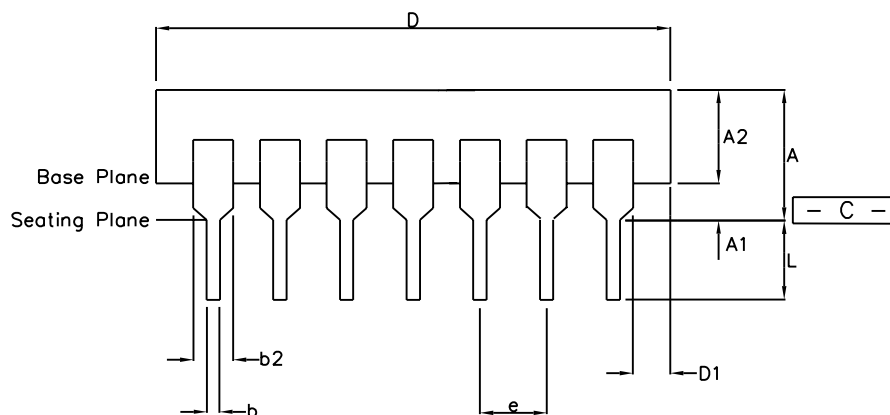
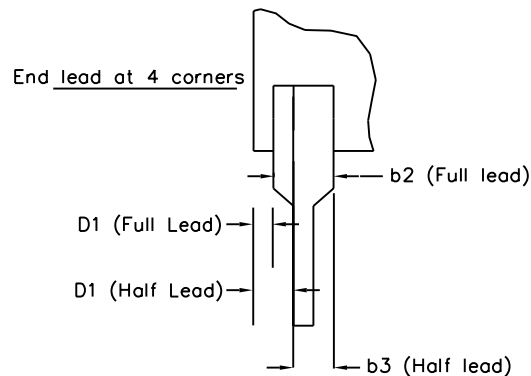
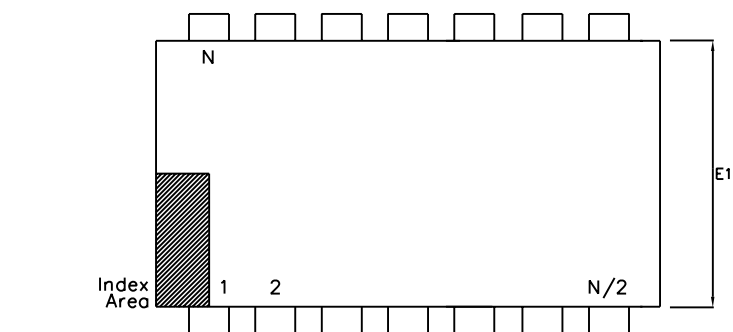
* Insert C15, delete R4 and R5 if CON2 is to be used to monitor the VCO. Delete C15 insert R4 and R5 if CON is to provide an external source, otherwise short C15 and delete R4, R5 and CON2.

COMPONENT LIST FOR FIG. 11

Capacitors				Resistors		Inductors		Miscellaneous	
C0	1nF 10%	C17	22μF/35V Elect.	R1	270	L1	15μH 10%	IC1	NJ88C33
C1	100nF 10%	C19	10nF 10%	R2	470	L2	220μH 10%	X1	10.00MHz 5ppm series
C2	1μF Tant.	C20	22μF/35V Elect.	R3	330	L3	180nH 20%	SW1	Miniature slide switch
C4	10nF 10%	C21	10nF 10%	R4	100	L4	470μH 10%	CON1	SMC socket
C5	22μF/35V Elect.	C22	10nF 10%	R5	100	Diodes		CON2	SMC socket
C6	10nF 10%	C23	22pF 5% NPO	R6	1k			PCB	C33ISS2
C7	1nF 10%	C24	22μF/35V Elect.	R7	120	Transistors			
C8	1nF 10%	C27	22pF 5% NPO	R8	27k			D1	1N6263 Schottky
C9	1nF 10%	VC1	3p5-22p	R9	Link			D2	1N6263 Schottky
C11	150pF 5% NPO			R10	1k			D3	BBY40 varicap
C12	1nF 10%			R11	10	D4	5mm red LED		
C13	1nF 10%			R12	10				
C14	2p7 ± 0.5pF NPO			R13	10				
C15	10nF 10%			R14	22k				
C16	10nF 10%			R15	2.7k	TR1	BFS17 RF NPN		
				R16	330R	TR2	BFS17 RF NPN		
				R17	100	TR3	2N3904 Switching		
				R18	33M				

NOTES

1. With the exception of electrolytics, all capacitors are surface mount types.
2. All resistors are 0.25W, ±2%.
3. C0, C1, C2, C11, C12, C13 and C14 must be low leakage types.
4. R18 may be required to optimise VCO close in noise performance.



	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54	BSC	0.100	BSC
eA	7.62	BSC	0.300	BSC
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	14		14	
Conforms to Jedec MS-001AA Issue D				

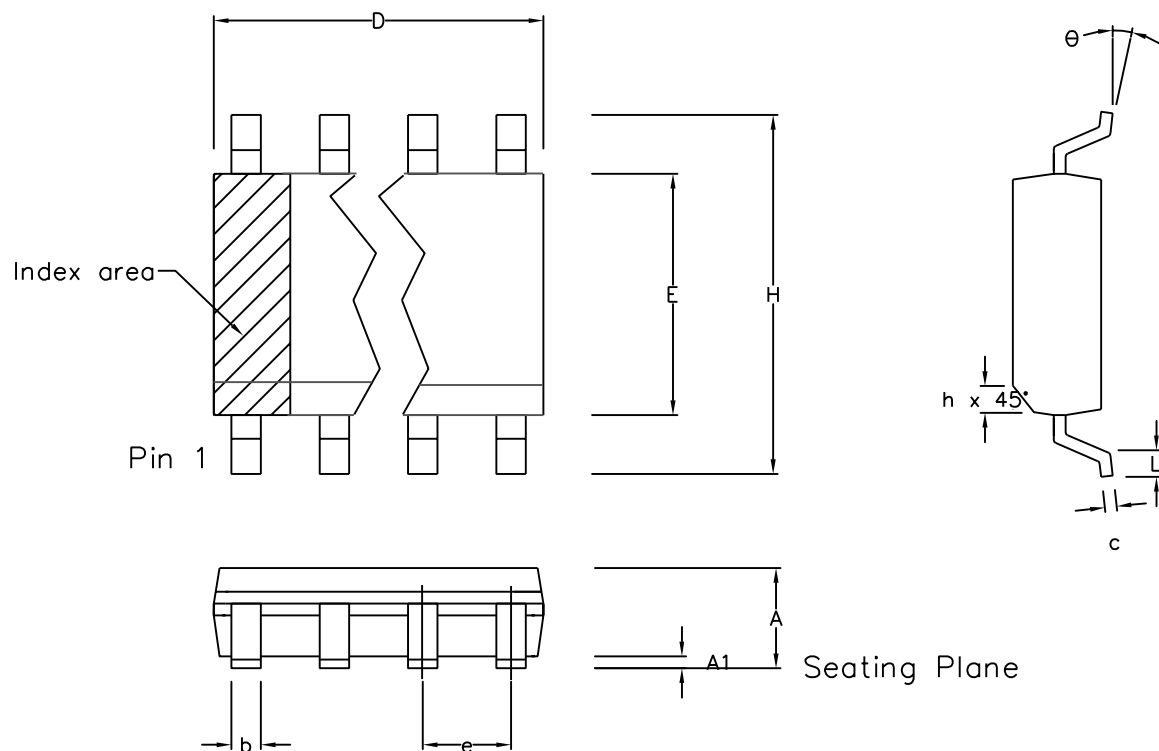
Notes:

1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum - C -
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: -
Plymouth/Swindon drawing # 418/ED/39502/002

© Zarlink Semiconductor 2002 All rights reserved.					Package Code DA	
ISSUE	1	2			Previous package codes DP / E	Package Outline for 14 lead PDIP
ACN	202539	212482				
DATE	23May97	5Apr02				GPD00344
APPRD.						





	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
O	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

© Zarlink Semiconductor 2002 All rights reserved.						Package Code DC	
ISSUE	1	2	3	4	5	Previous package codes MP / S	Package Outline for 14 lead SOIC (0.150" Body Width)
ACN	6745	201937	202596	203707	212430		
DATE	7Apr95	27Feb97	12Jun97	9Dec97	25Mar02		GPD00011
APPRD.							





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