MX27C256

256K-BIT [32K x 8] CMOS EPROM

FEATURES

- 32K x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 45/55/70/90/100/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 30mA
- Standby current: 100uA
- Package type:
  - 28 pin ceramic DIP, plastic DIP, plastic SOP
  - 32 pin PLCC
  - 28 pin 8 x 13.4mm TSOP(I)

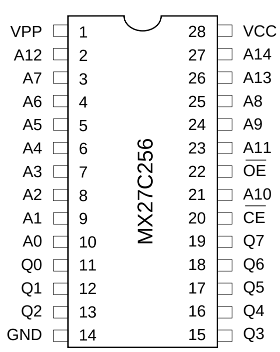
GENERAL DESCRIPTION

The MX27C256 is a 5V only, 256K-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 32K by 8 bits, operates from a single + 5volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming from outside the system, existing EPROM programmers may be used. The MX27C256 supports intelligent fast programming algorithm which can result in programming time of less than ten seconds.

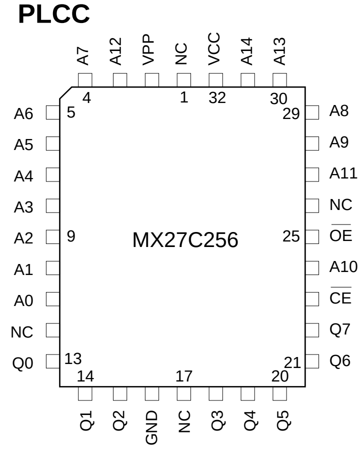
This EPROM is packaged in industry standard 28 pin dual-in-line packages, 32 lead PLCC, 28 lead SOP, and 28 lead TSOP(I) packages.

PIN CONFIGURATIONS

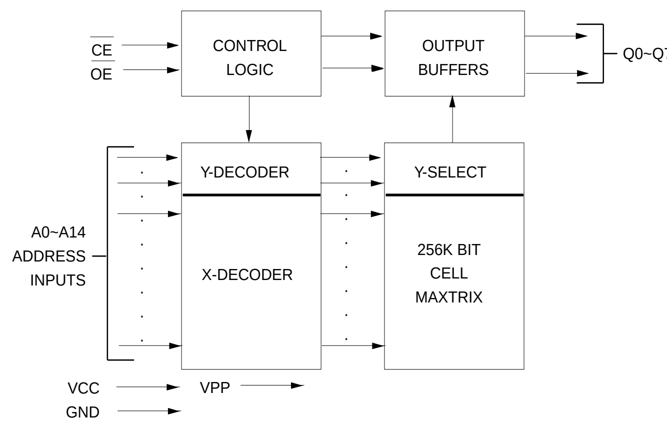
CDIP/PDIP/SOP



PLCC



BLOCK DIAGRAM



8 x 13.4mm 28-TSOP(I)

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A14	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C256

The MX27C256 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm2 is required to completely erase a MX27C256. This dosage can be obtained by exposure to an ultraviolet lamp - wavelength of 2537 Angstroms (Å) - with intensity of 12,000 uW/cm2 for 15 to 20 minutes. The MX27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C256, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C256

When the MX27C256 is delivered, or it is erased, the chip has all 256K bits in the "ONE" or HIGH state. "ZEROs" are loaded into the MX27C256 through the procedure of programming.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP. When programming an MXIC EPROM, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{OE}$ = VIH (Algorithm is shown in Figure 1). The programming is achieved by applying a single TTL low level 100us pulse to the $\overline{CE}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C256s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C256 may be common. A TTL low-level program pulse applied to an MX27C256 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V and $\overline{OE}$ HIGH will program that MX27C256. A high-level $\overline{CE}$ input inhibits the other MX27C256s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{CE}$ and $\overline{OE}$ at VIL, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C256.

To activate this mode, the programming equipment must force 12.0 ± 0.5 (VH) on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C256, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q7) defined as the parity bit.

READ MODE

The MX27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27C256 has a CMOS standby mode which reduces the maximum Vcc current to 100 uA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C256 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

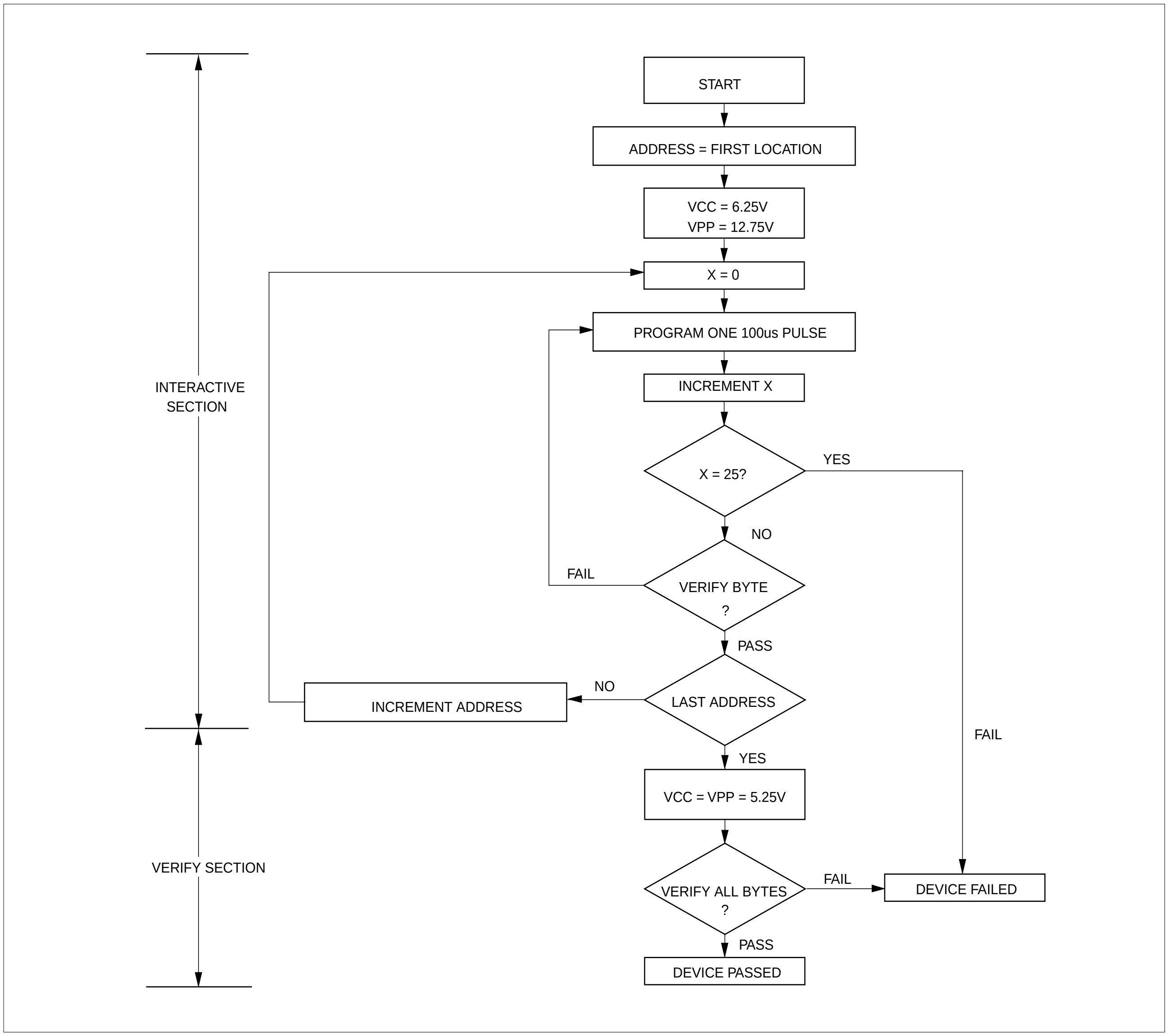
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between Vcc and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

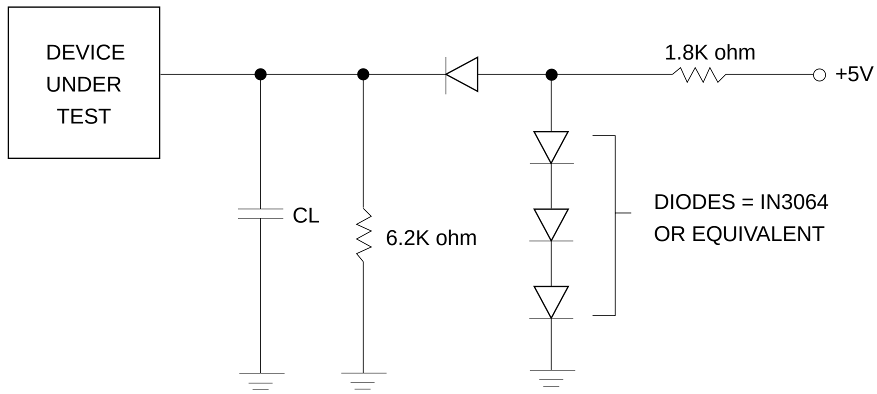
	PINS					
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	VCC	High Z
Program	VIL	VIH	X	X	VPP	DIN
Program Verify	VIH	VIL	X	X	VPP	DOUT
Program Inhibit	VIH	VIH	X	X	VPP	High Z
Manufacturer Code(3)	VIL	VIL	VIL	VH	VCC	C2H
Device Code(3)	VIL	VIL	VIH	VH	VCC	10H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL
3. A1 - A8 = A10 - A14 = VIL(For auto select)
4. See DC Programming characteristics for VPP voltage during programming.

FIGURE 1. FAST PROGRAMMING FLOW CHART

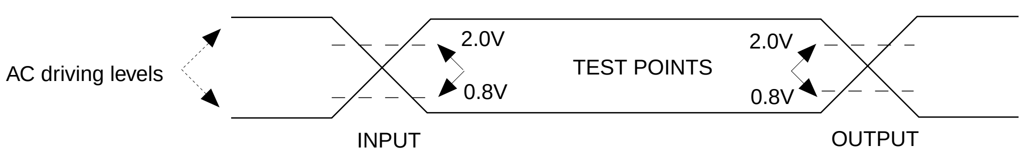


SWITCHING TEST CIRCUITS

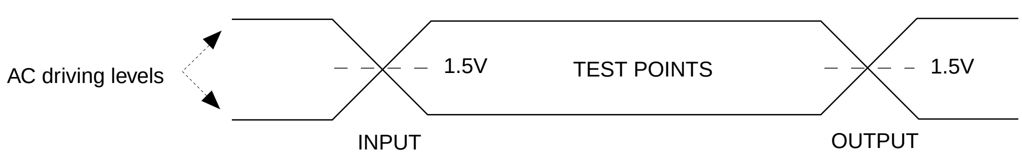


CL = 100 pF including jig capacitance(30pF for 45/55/70ns parts)

SWITCHING TEST WAVEFORMS



AC TESTING: AC driving levels are 2.4V/0.4V for commercial grade, 3.0V/0V for industrial grade.
Input pulse rise and fall times are ≤ 10ns.



AC TESTING: (1) AC driving levels are 3.0V/0V for both commercial grade and industrial grade.
Input pulse rise and fall times are ≤ 10ns.
(2) For MX27C256-45, MX27C256-55, MX27C256-70.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
NOTICE:
Specifications contained within the following tables are subject to change.

DC/AC Operating Conditions for Read Operation

		MX27C256						
		-45	**-55**	**-70**	**-90**	**-10**	**-12**	**-15**
Operating Temperature	Commercial	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
	Industrial	-45°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ±10%	5V ± 10%	5V ± 10%

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	uA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		30	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		10	uA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
VPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS

SYMBOL	PARAMETER	27C256-45 MIN.	27C256-45 MAX.	27C256-55 MIN.	27C256-55 MAX.	27C256-70 MIN.	27C256-70 MAX.	27C256-90 MIN.	27C256-90 MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		45		55		70		90	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		45		55		70		90	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		22		30		35		40	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	16	0	20	0	20	0	25	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		0		ns	

SYMBOL	PARAMETER	27C256-10 MIN.	27C256-10 MAX.	27C256-12 MIN.	27C256-12 MAX.	27C256-15 MIN.	27C256-15 MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		100		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		100		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		45		50		55	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	30	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25ºC ± 5℃

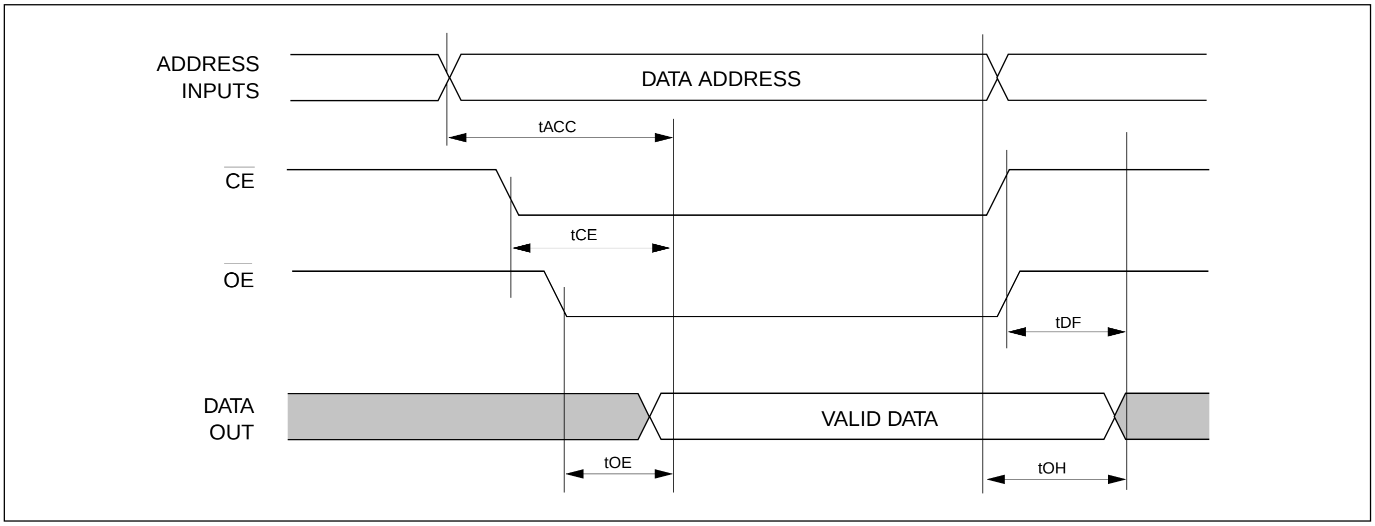
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current(Program & Verify)		40	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Fast Programming Supply Voltage	6.00	6.50	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25ºC ± 5℃

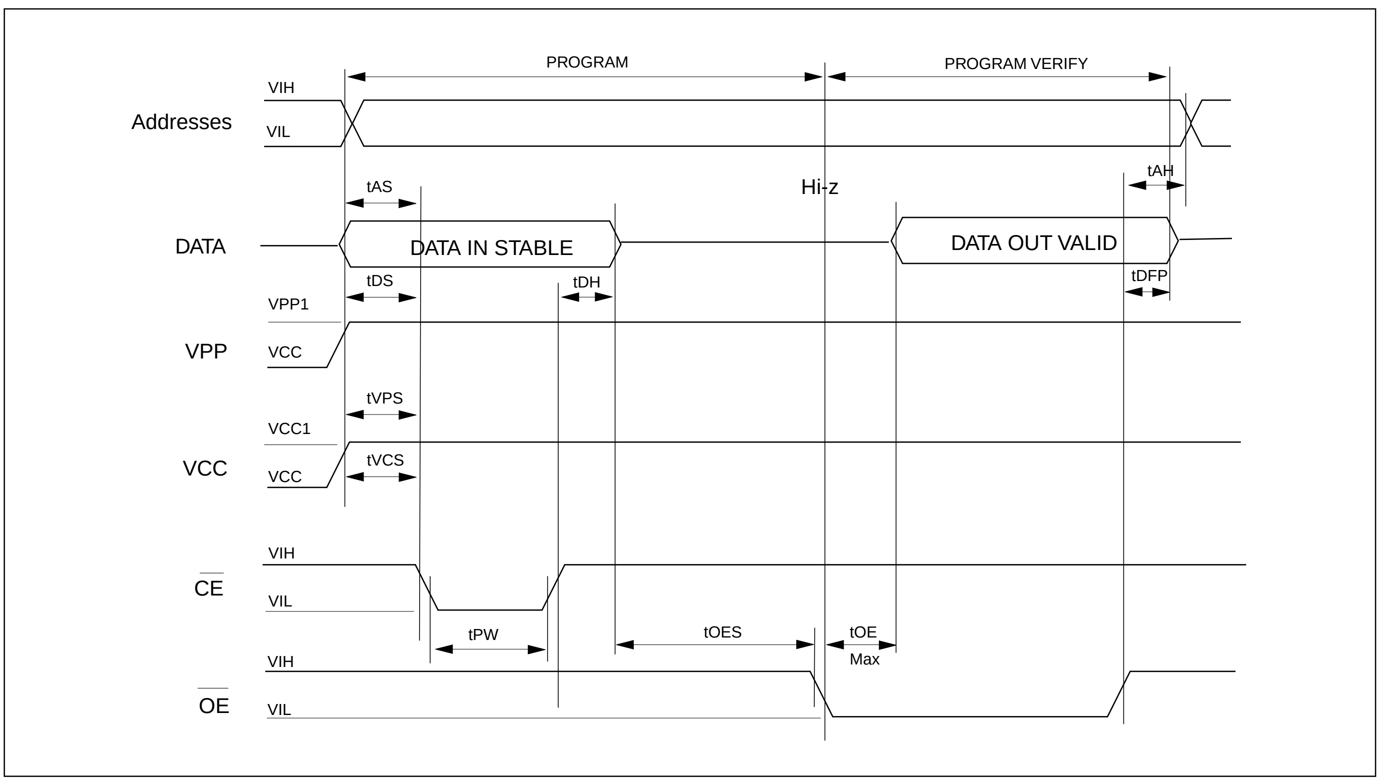
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time	2.0		us	
tOES	$\overline{\text{OE}}$ Setup Time	2.0		us	
tDS	Data Setup Time	2.0		us	
tAH	Address Hold Time	0		us	
tDH	Data Hold Time	2.0		us	
tDFP	Output Enable to Output Float Delay	0	130	ns	
tVPS	VPP Setup Time	2.0		us	
tVCS	VCC Setup Time	2.0		us	
tOE	Data Valid from $\overline{\text{OE}}$		150	ns	
tPW	$\overline{\text{PGM}}$ Program Pulse Width	95	105	us	

WVEFORMS

READ CYCLE



FAST PROGRAMMING ALGORITHM WAVEFORM



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX27C256DC-45	45	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DC-55	55	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DC-70	70	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DC-90	90	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DC-10	100	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DC-12	120	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DC-15	150	30	100	0℃ to 70℃	28 Pin DIP
MX27C256DI-45	45	30	100	-40℃ to 85℃	28 Pin DIP
MX27C256DI-55	55	30	100	-40℃ to 85℃	28 Pin DIP
MX27C256DI-70	70	30	100	-40℃ to 85℃	28 Pin DIP
MX27C256DI-90	90	30	100	-40℃ to 85℃	28 Pin DIP
MX27C256DI-10	100	30	100	-40℃ to 85℃	28 Pin DIP
MX27C256DI-12	120	30	100	-40℃ to 85℃	28 Pin DIP
MX27C256DI-15	150	30	100	-40℃ to 85℃	28 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX27C256MC-45	45	30	100	0℃ to 70℃	28 Pin SOP
MX27C256PC-45	45	30	100	0℃ to 70℃	28 Pin DIP
MX27C256QC-45	45	30	100	0℃ to 70℃	32 Pin PLCC
MX27C256TC-45	45	30	100	0℃ to 70℃	28 Pin TSOP(I)
MX27C256MC-55	55	30	100	0℃ to 70℃	28 Pin SOP
MX27C256PC-55	55	30	100	0℃ to 70℃	28 Pin DIP
MX27C256QC-55	55	30	100	0℃ to 70℃	32 Pin PLCC
MX27C256TC-55	55	30	100	0℃ to 70℃	28 Pin TSOP(I)
MX27C256MC-70	70	30	100	0℃ to 70℃	28 Pin SOP
MX27C256PC-70	70	30	100	0℃ to 70℃	28 Pin DIP
MX27C256QC-70	70	30	100	0℃ to 70℃	32 Pin PLCC
MX27C256TC-70	70	30	100	0℃ to 70℃	28 Pin TSOP(I)
MX27C256MC-90	90	30	100	0℃ to 70℃	28 Pin SOP
MX27C256PC-90	90	30	100	0℃ to 70℃	28 Pin DIP
MX27C256QC-90	90	30	100	0℃ to 70℃	32 Pin PLCC
MX27C256TC-90	90	30	100	0℃ to 70℃	28 Pin TSOP(I)
MX27C256MC-10	100	30	100	0℃ to 70℃	28 Pin SOP
MX27C256PC-10	100	30	100	0℃ to 70℃	28 Pin DIP
MX27C256QC-10	100	30	100	0℃ to 70℃	32 Pin PLCC
MX27C256TC-10	100	30	100	0℃ to 70℃	28 Pin TSOP(I)

PLASTIC PACKAGE(Continued)

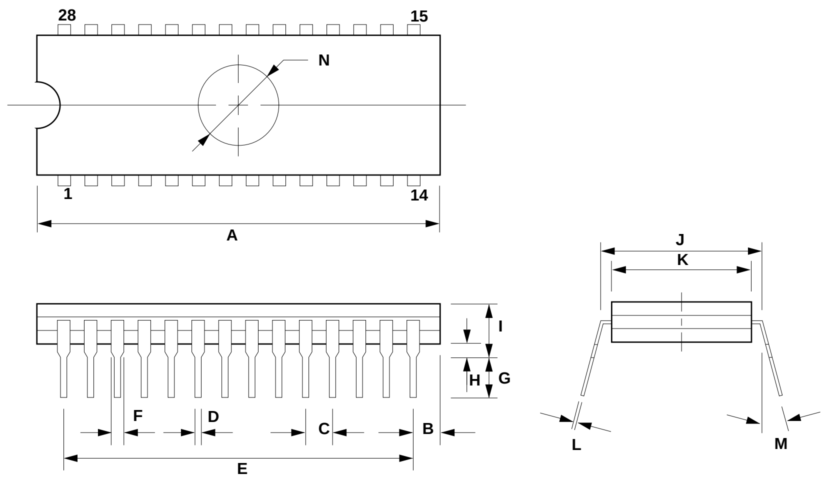
PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX27C256MC-12	120	30	100	0°C to 70°C	28 Pin SOP
MX27C256PC-12	120	30	100	0°C to 70°C	28 Pin DIP
MX27C256QC-12	120	30	100	0°C to 70°C	32 Pin PLCC
MX27C256TC-12	120	30	100	0°C to 70°C	28 Pin TSOP(I)
MX27C256MC-15	150	30	100	0°C to 70°C	28 Pin SOP
MX27C256PC-15	150	30	100	0°C to 70°C	28 Pin DIP
MX27C256QC-15	150	30	100	0°C to 70°C	32 Pin PLCC
MX27C256TC-15	150	30	100	0°C to 70°C	28 Pin TSOP(I)
MX27C256MI-45	45	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-45	45	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-45	45	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-45	45	30	100	-40°C to 85°C	28 Pin TSOP(I)
MX27C256MI-55	55	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-55	55	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-55	55	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-55	55	30	100	-40°C to 85°C	28 Pin TSOP(I)
MX27C256MI-70	70	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-70	70	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-70	70	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-70	70	30	100	-40°C to 85°C	28 Pin TSOP(I)
MX27C256MI-90	90	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-90	90	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-90	90	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-90	90	30	100	-40°C to 85°C	28 Pin TSOP(I)
MX27C256MI-10	100	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-10	100	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-10	100	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-10	100	30	100	-40°C to 85°C	28 Pin TSOP(I)
MX27C256MI-12	120	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-12	120	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-12	120	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-12	120	30	100	-40°C to 85°C	28 Pin TSOP(I)
MX27C256MI-15	150	30	100	-40°C to 85°C	28 Pin SOP
MX27C256PI-15	150	30	100	-40°C to 85°C	28 Pin DIP
MX27C256QI-15	150	30	100	-40°C to 85°C	32 Pin PLCC
MX27C256TI-15	150	30	100	-40°C to 85°C	28 Pin TSOP(I)

PACKAGE INFORMATION

28-PIN CERDIP(MSI) WITH WINDOW (600 mil)

ITEM	MILLIMETERS	INCHES
A	37.69 max	1.485 max
B	1.85 ± .30	.073 ± .012
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	33.02	1.300
F	1.40 ± .05	.055 ± .002
G	3.43 ± .38	.135 ± .015
H	.96 ± .43	.038 ± .017
I	4.87	.198
J	15.48 ± .13	.610 ± .005
K	13.38 ± .38	.527 ± .015
L	.25 ± .13	.010 ± .005
M	0 ~ 15°	0 ~ 15°
N	ø7.11	ø.280

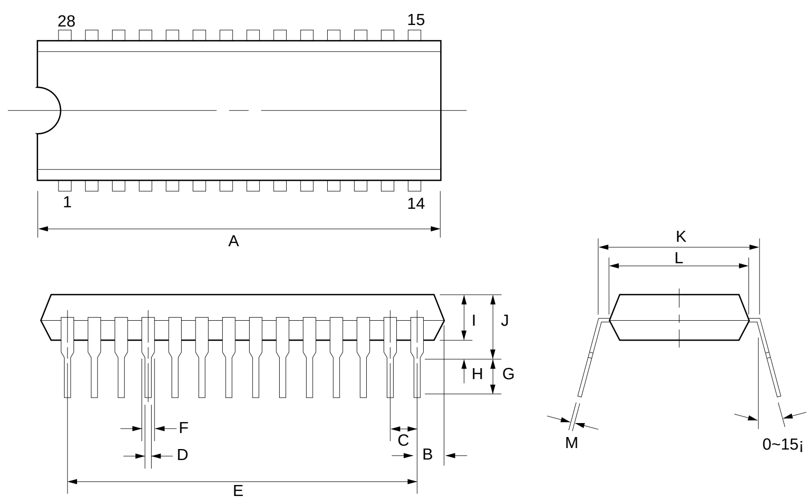
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



28-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	37.34 max	1.470 max
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	32.99	1.300
F	1.52 [Typ.]	.060 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.84 ± .25	.545 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.

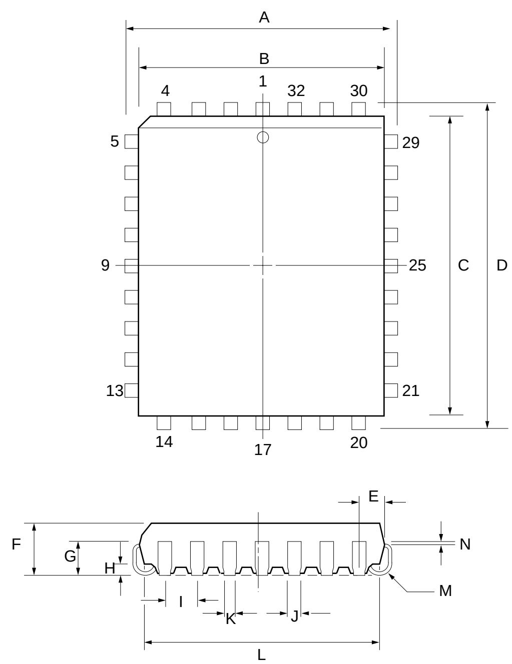


PACKAGE INFORMATION(Continued)

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	.71	.028
G	3.30 ± .25	.130 ± .010
H	2.03 ± .13	.080 ± .005
I	.51 ± .13	.020 ± .005
J	1.27 [Typ.]	.050 [Typ.]
K	.46 [REF]	.018 [REF]
L	.46 [REF]	.018 [REF]
M	10.40/12.94 (W) (L)	.410/.510 (W) (L)
N	.89 R	.035 R
O	.25	.010

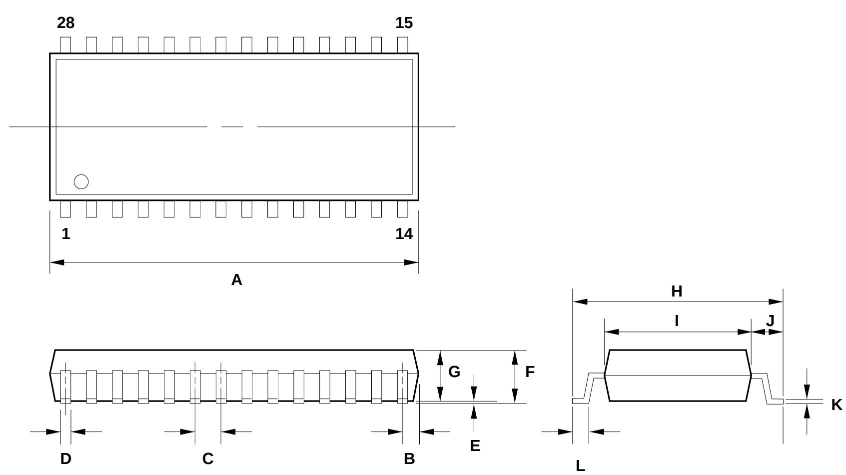
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



28-PIN PLASTIC SOP(330 mil)

ITEM	MILLIMETERS	INCHES
A	18.11 max.	.713 max.
B	1.194 max	.047 max
C	1.27 [TP]	.050 [TP]
D	.41 [Typ.]	.016 [Typ.]
E	.10 min.	.004 min.
F	2.84 max.	.112 max.
G	2.49 ± .13	.098 ± .005
H	11.81 ± .31	.465 ± .012
I	8.41 ± .13	.331± .005
J	1.70 ± .20	.067 ± .008
K	.25 [Typ.]	.010 [Typ.]
L	.762	.03

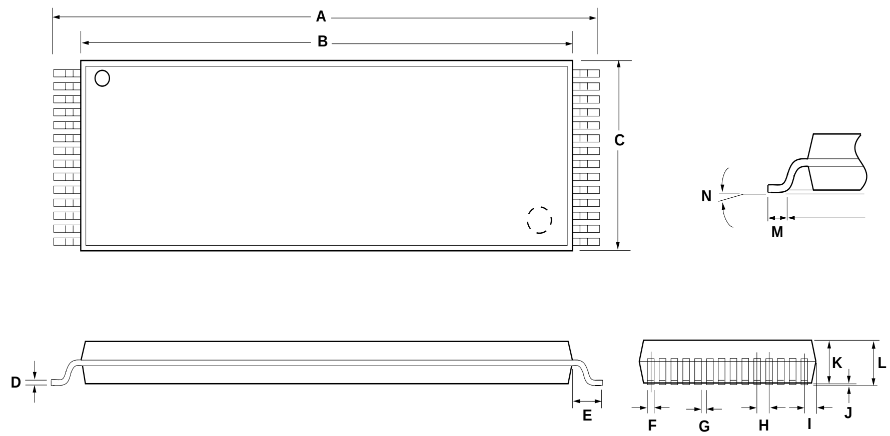
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



8 x 13.4mm 28-PIN PLASTIC TSOP

ITEM	MILLIMETERS
A	13.4 ± .2
B	11.8 ± .1
C	8.0 ± .1
D	.15 ± .01
F	.2 ± .03
H	.55 [Typ.]
I	.425 [Typ.]
J	.05 [Min.]
K	1.00 ± .05
L	1.25 [Max.]
M	.05 ± .20
N	O° ~ 5°

NOTE: Each lead centerline is located within .25 mm of its true position [TP] at maximum material condition.



Revision History

Revision No.	Description	Date
5.0	1) Reduce operating current from 40mA to 30mA.	6/16/1997
	2) Add 28-TSOP(I) and 28-SOP packages offering.	
	3) Eliminate Interactive Programming Mode.	
5.1	1) IPP1 100uA ----> 10uA	7/17/1997

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