

The SP4666 is a selectable division ratio high speed divider capable of replacing separate fixed ratio ECL prescalers with a single part in applications with alternative  $\div 64$  and  $\div 256$  division requirements.

A switched low pass filter with  $-3\text{dB}$  points at  $5.3\text{MHz}$  and  $15.6\text{MHz}$  is connected before the output stage to reduce the harmonic content to a very low level.

### FEATURES

- Switched Low Pass Filter for Very Low Output Radiation
- Low Supply Current
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection †

† ESD precautions must be observed

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$	+7V
Input voltage	2.5V p-p
Storage temperature	$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating temperature range	$0^{\circ}\text{C}$ to $+80^{\circ}\text{C}$

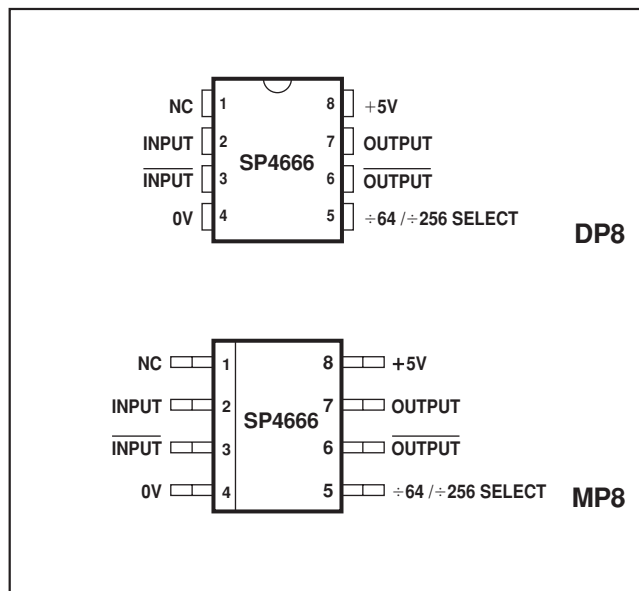


Fig 1. Pin connections - top view

### ORDERING INFORMATION

SP4666 NA DP  
SP4666 NA MP

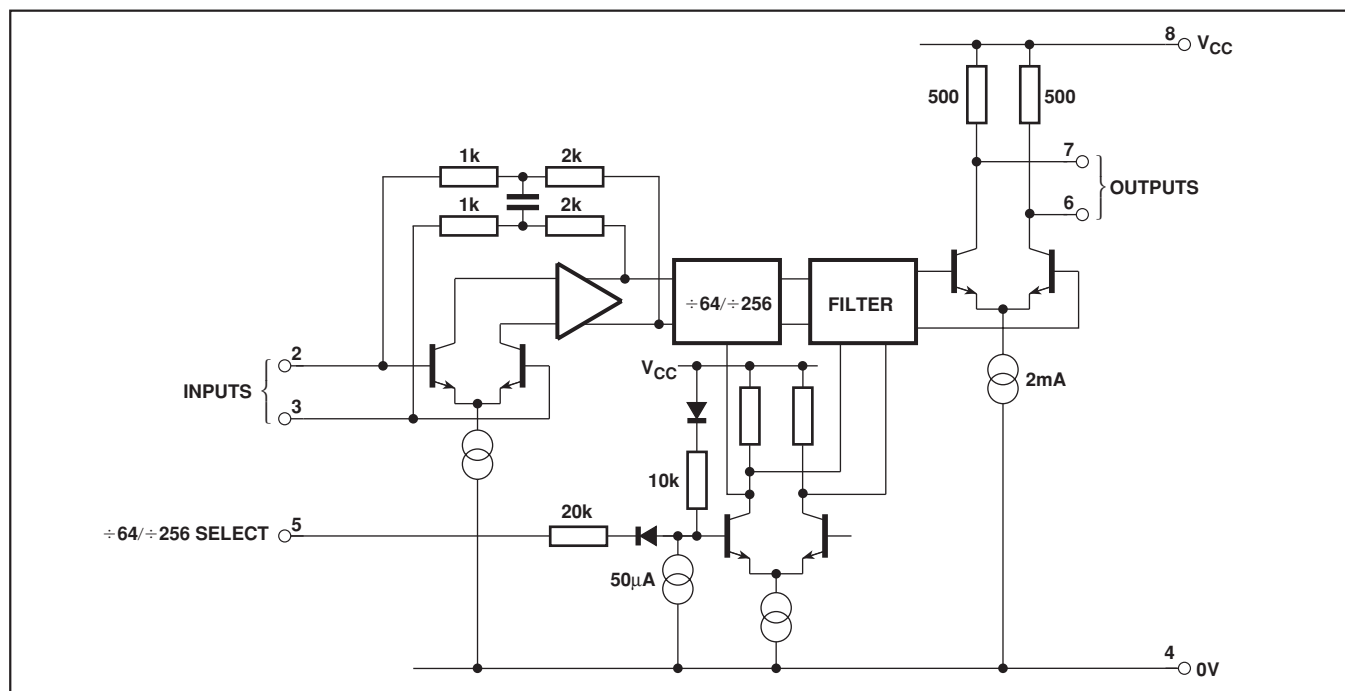


Fig. 2 SP4666 block diagram

## SP4666

### ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

$T_{AMB} = 0^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$  (Test circuit see Fig. 3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, $I_{CC}$	8		23	30	mA	$V_{CC} = +5\text{V}$
Input sensitivity	2,3					RMS sinewave (50 $\Omega$ system)
50MHz			2.5	10	mV	
200MHz to 1050MHz			0.5	5	mV	
1050MHz to 1300MHz				10	mV	
Input overload	2,3	500			mV	
Input impedance	2,3		50		$\Omega$	See Fig. 6
			2		pF	
Output voltage with 12pF load	6,7	0.8	1		V p-p	$\div 64$ mode, $f_{IN} = 100\text{MHz}$
		0.8	1		V p-p	$\div 256$ mode, $f_{IN} = 100\text{MHz}$
		0.4	0.5		V p-p	$\div 64$ mode, $f_{IN} = 1000\text{MHz}$
		0.7	0.9		V p-p	$\div 256$ mode, $f_{IN} = 1000\text{MHz}$
		0.25	0.35		V p-p	$\div 64$ mode, $f_{IN} = 1300\text{MHz}$
		0.6	0.7		V p-p	$\div 256$ mode, $f_{IN} = 1300\text{MHz}$
Output impedance	6,7		500		$\Omega$	
Output imbalance	6,7		0.1		V	
Voltage for $\div 256$ operation	5			0.5	V	
Voltage for $\div 64$ operation	5	3.5			V	See note 1
Sink current for $\div 256$ operation	5			250	$\mu\text{A}$	$V_{pin5} = 0\text{V}$

#### NOTES

- Pin 5 has an internal pull-up and may be left open-circuit for  $\div 64$  operation.
- The difference between the maximum input sensitivity and minimum overload voltage is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

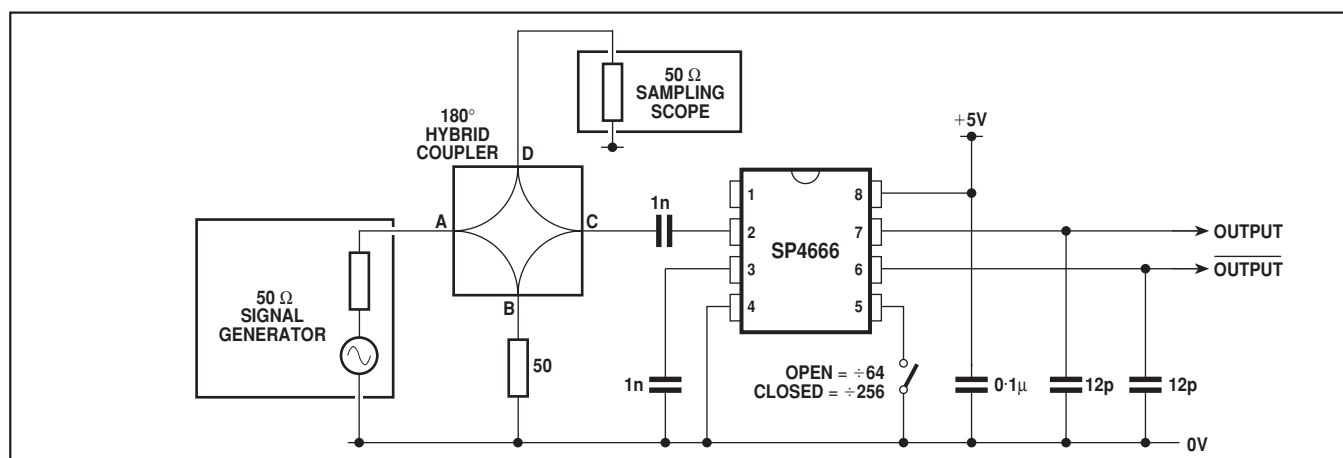


Fig. 3 Test circuit

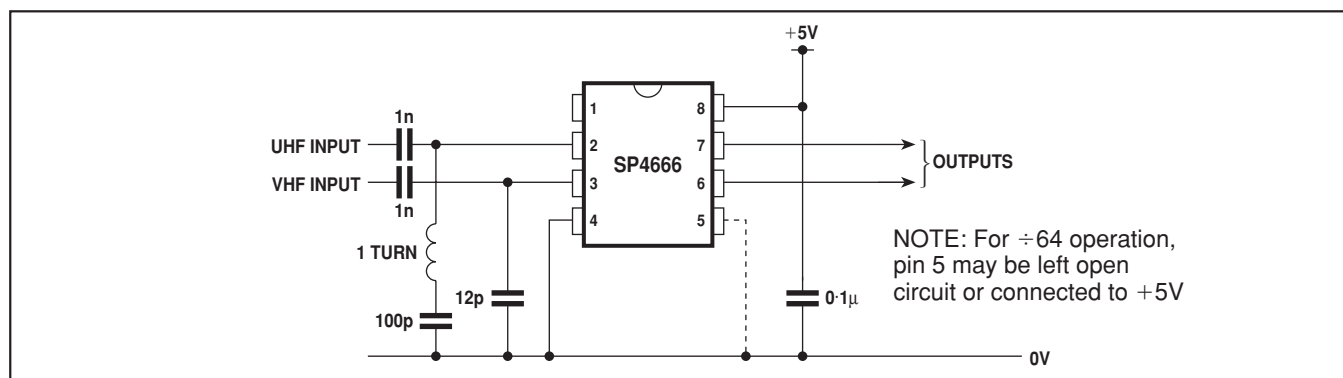


Fig. 4 Application circuit

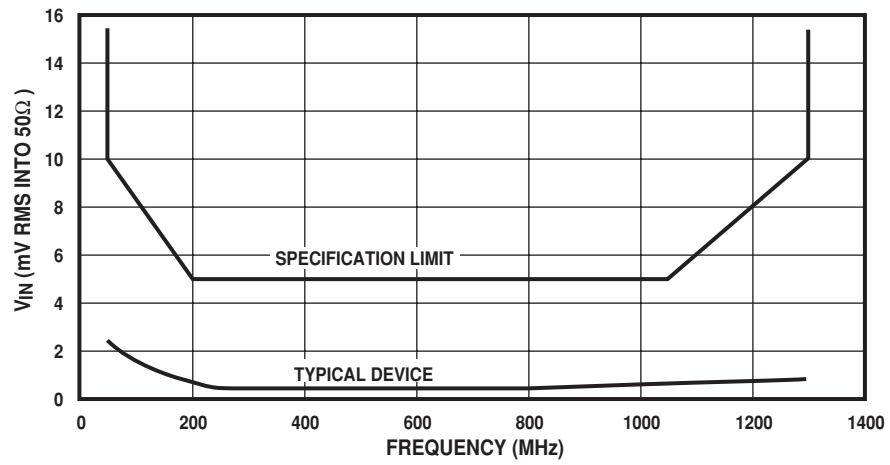


Fig. 5 Typical input sensitivity

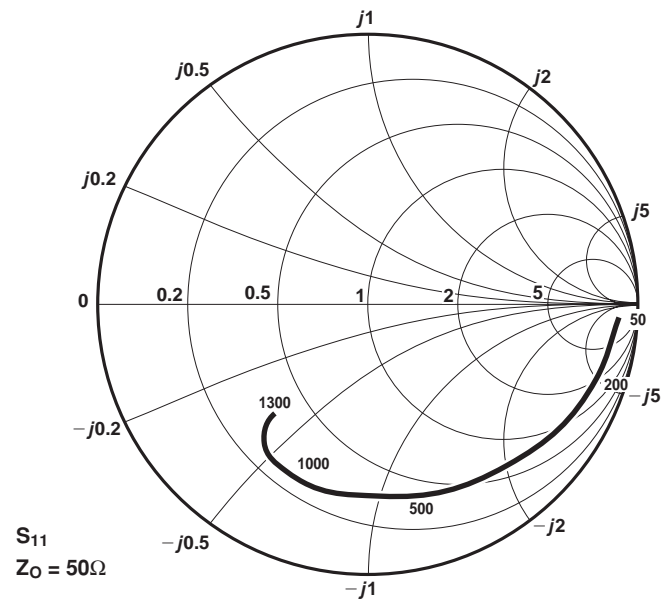


Fig. 6 Typical input impedance (frequencies in MHz)



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