

-12A, -100V, P-Channel Enhancement Mode Power MOS Field Effect Transistor

December 2001

Features

- -12A, -100V
- $r_{DS(ON)} = 0.3\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Ordering Information

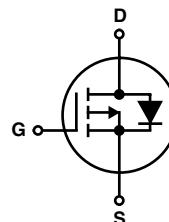
PART NUMBER	PACKAGE	BRAND
2N6897	TO-204AA	2N6897

NOTE: When ordering, include the entire part number.

Description

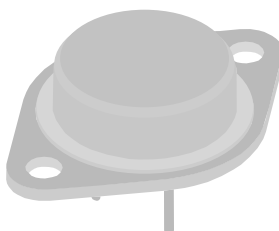
The 2N6897 is an P-Channel enhancement mode silicon gate power MOS field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This device can be operated directly from an integrated circuit.

Symbol



Packaging

JEDEC TO-204AA



2N6897

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	2N6897	UNITS
Drain to Source Voltage	BV_{DSS}	V
Drain to Gate Voltage ($R_{GS} = 1\text{M}\Omega$)	V_{DGR}	V
Continuous Drain Current		
RMS Continuous	I_D	A
Pulsed Drain Current	I_{DM}	A
Gate to Source Voltage	V_{GS}	V
Maximum Power Dissipation		
$T_C = 25^\circ\text{C}$	P_D	W
Above $T_C = 25^\circ\text{C}$, Derate Linearly		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	$^\circ\text{C}$
Maximum Lead Temperature for Soldering (At distance 1/8 in. (3.17mm) from seating plane for 10s max)	T_L	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$	-100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 0.25\text{mA}$	-2	-	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80\text{V}$	-	-	1	μA
Zero-Gate Voltage Drain Current $T_C = 125^\circ\text{C}$		$V_{DS} = -80\text{V}$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	100	nA
Drain to Source On-Voltage (Note 1)	$V_{DS(ON)}$	$I_D = 7.6\text{A}, V_{GS} = -10\text{V}$	-	-	2.28	V
		$I_D = 12\text{A}, V_{GS} = -10\text{V}$	-	-	-4.8	V
Static Drain to Source On Resistance (Note 1)	$r_{DS(ON)}$	$I_D = 7.6\text{A}, V_{GS} = -10\text{V}$	-	-	0.3	Ω
Static Drain to Source On Resistance $T_C = 125^\circ\text{C}$ (Note 1)		$I_D = 7.6\text{A}, V_{GS} = 10\text{V}$	-	-	0.465	Ω
Forward Transconductance (Note 1)	g_{fs}	$I_D = 7.6\text{A}, V_{DS} = -10\text{V}$	2	-	8	S
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}$ $f = 0.1\text{MHz}$	400	-	1500	pF
Output Capacitance	C_{OSS}		200	-	700	pF
Reverse-Transfer Capacitance	C_{RSS}		60	-	240	pF
Turn-On Delay Time	$t_{d(ON)}$	$I_D = 7.6\text{A}, V_{DS} = -50\text{V}$ $R_{GEN} = R_{GS} = 15\Omega,$ $V_{GS} = -10\text{V}$	-	-	60	ns
Rise Time	t_r		-	-	175	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	275	ns
Fall Time	t_f		-	-	175	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	-	1.25	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage (Note 1)	V_{SD}	$I_{SD} = 12\text{A}$	0.8	-	1.6	V
Diode Reverse Recovery Time	t_{rr}	$I_F = 4\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	-	-	500	ns

NOTE:

- Pulsed: pulse duration = 300 μs , max, duty cycle = 2%.

Typical Performance Curves Unless Otherwise Specified

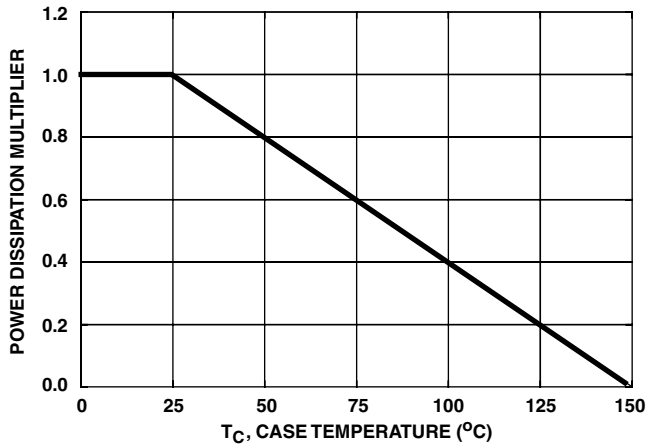


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

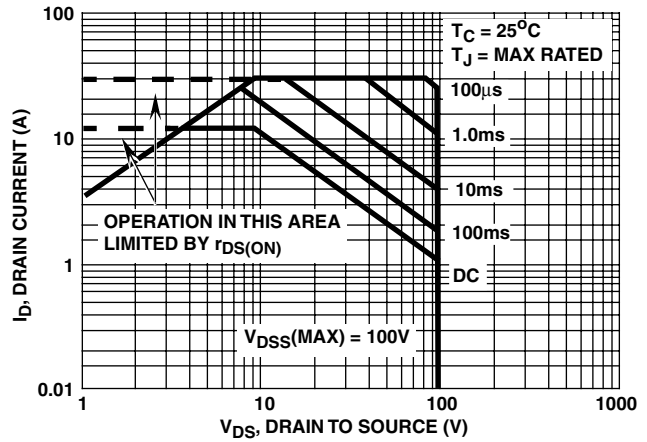


FIGURE 16. MAXIMUM OPERATING AREAS CURVE

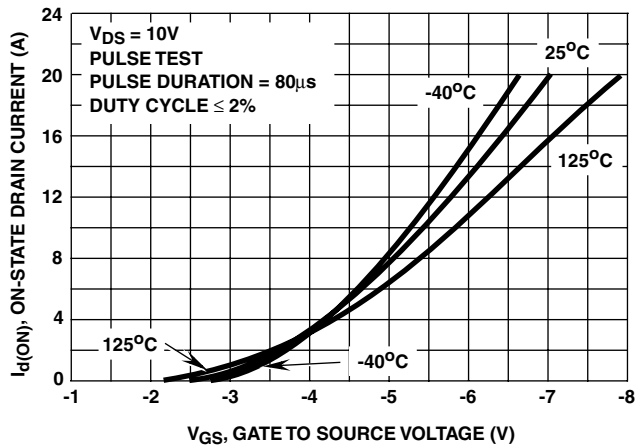


FIGURE 17. TRANSFER CHARACTERISTICS

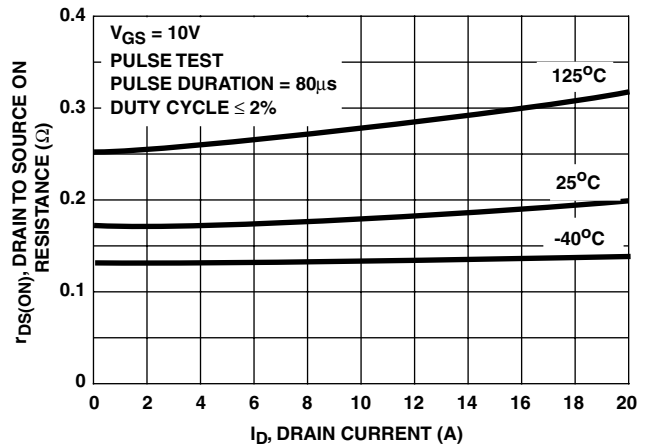


FIGURE 18. DRAIN TO SOURCE ON RESISTANCE AS A FUNCTION OF DRAIN CURRENT

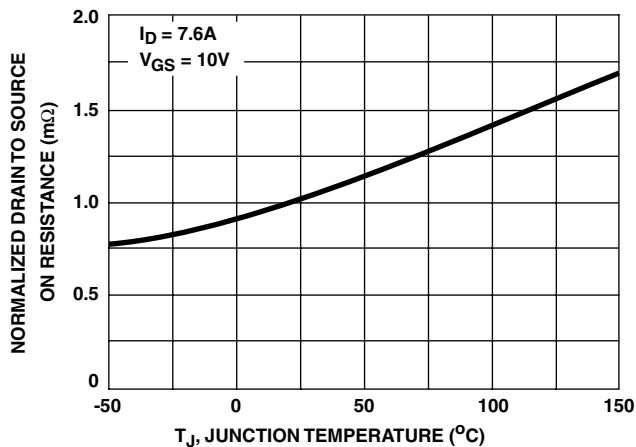


FIGURE 19. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

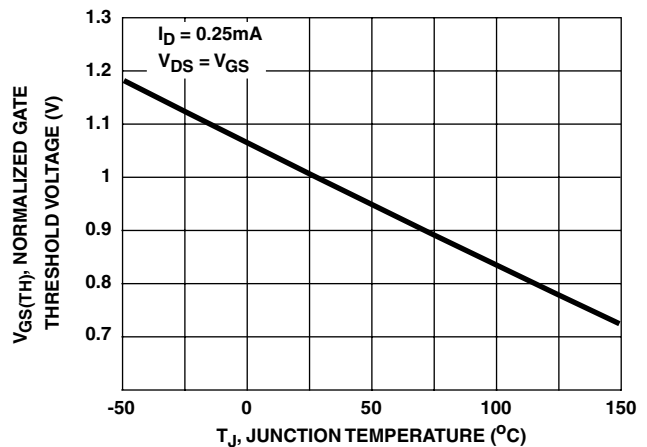


FIGURE 20. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

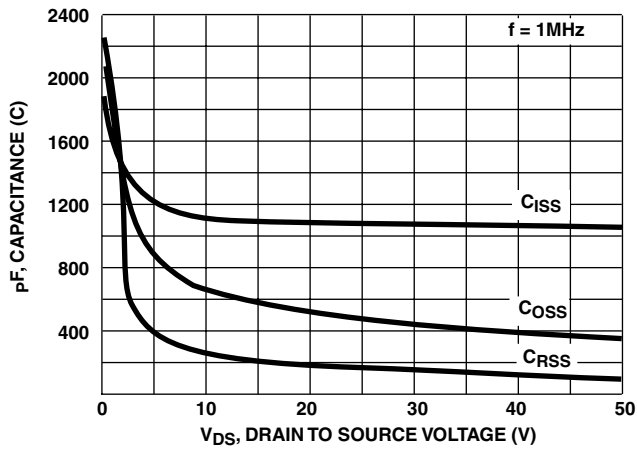
Typical Performance Curves Unless Otherwise Specified (Continued)


FIGURE 21. CAPACITANCE vs VOLTAGE

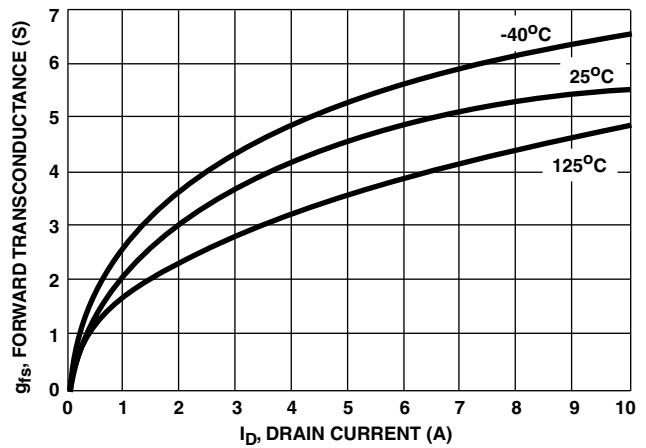


FIGURE 22. FORWARD TRANSCONDUCTANCE AS A FUNCTION OF DRAIN CURRENT

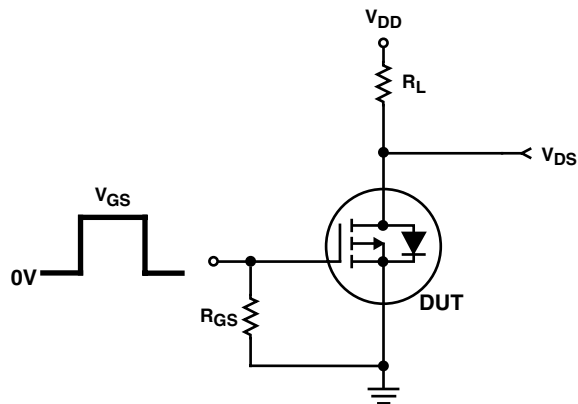
Test Circuit and Waveforms


FIGURE 23. RESISTIVE SWITCHING TEST CIRCUIT

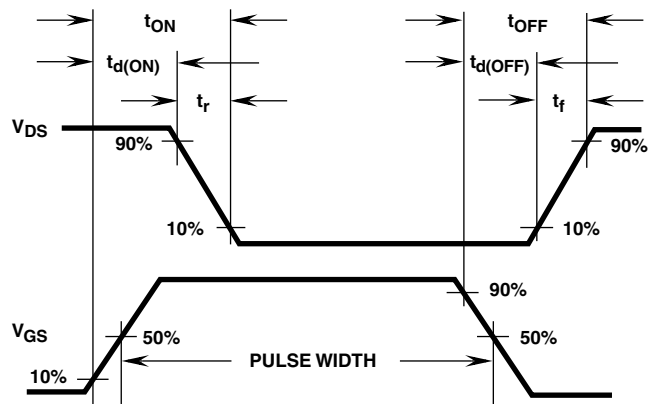


FIGURE 24. RESISTIVE SWITCHING WAVEFORMS

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