

2SJ363

Silicon P Channel MOS FET

Application

Low frequency power switching

Features

- Low on-resistance
- Low drive current
- 4 V gate drive device can be driven from 5 V source

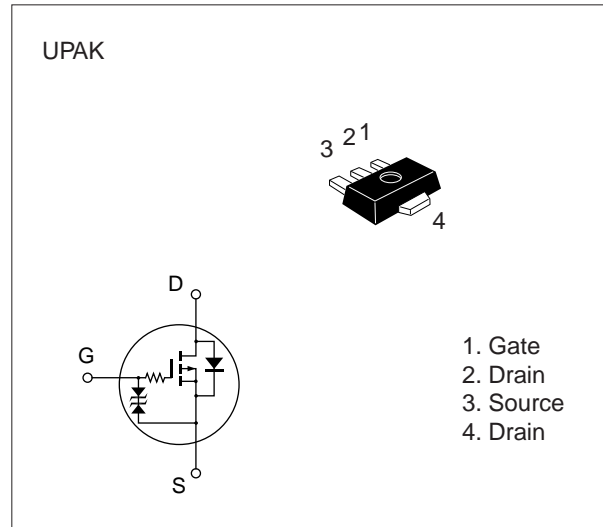


Table 1 Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-2	A
Drain peak current	$I_{D(\text{pulse})}^*$	-4	A
Body-drain diode reverse drain current	I_{DR}	-2	A
Channel dissipation	P_{ch}^{**}	1	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 100 \mu\text{s}$, duty cycle $\leq 10\%$

** Value on the alumina ceramic board (12.5 x 20 x 0.7mm)

*** Marking is "PY".

Table 2 Electrical Characteristics ($T_a = 25^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10\text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 10\text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -24\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -100\text{ }\mu\text{A}$, $V_{DS} = -10\text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.6	0.75	Ω	$I_D = -1\text{ A}$ $V_{GS} = -4\text{ V}^*$
		—	0.35	0.45	Ω	$I_D = -1\text{ A}$ $V_{GS} = -10\text{ V}^*$
Forward transfer admittance	$ y_{fs} $	1.4	2.0	—	S	$I_D = -1\text{ A}$ $V_{DS} = -10\text{ V}^*$
Input capacitance	C_{iss}	—	2.1	—	pF	$V_{DS} = -10\text{ V}$
Output capacitance	C_{oss}	—	100	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	0.25	—	pF	$f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	1.65	—	μs	$I_D = -1\text{ A}$
Rise time	t_r	—	8	—	μs	$V_{GS} = -10\text{ V}$
Turn-off delay time	$t_{d(off)}$	—	25.9	—	μs	$R_L = 30\text{ }\Omega$
Fall time	t_f	—	14.9	—	μs	

