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# 2SJ486

Silicon P Channel MOS FET  
Low Frequency Power Switching

# HITACHI

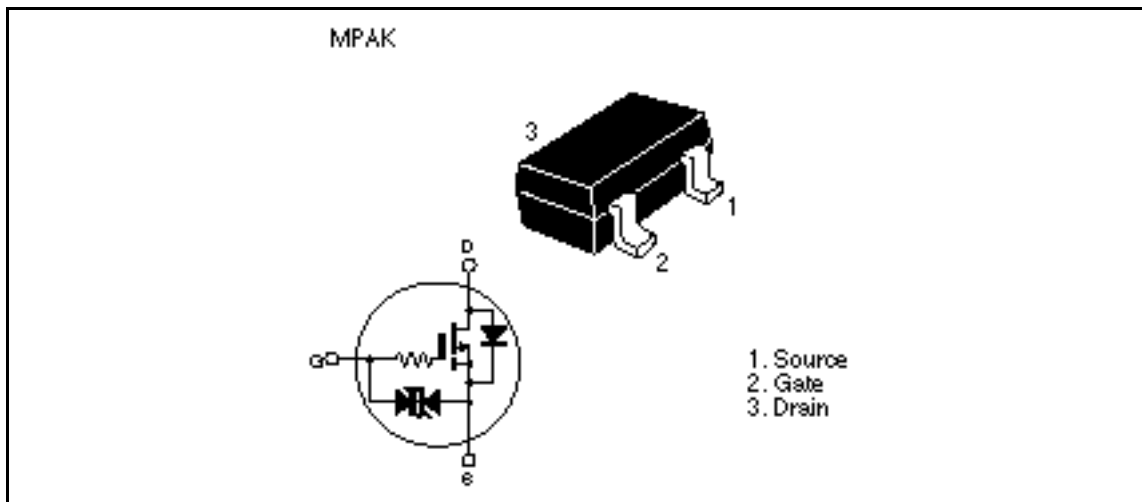
ADE-208-512 A  
2nd. Edition

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## Features

- Low on-resistance  
 $R_{DS(on)} = 0.5$  typ. (at  $V_{GS} = -4V$ ,  $I_D = -100$  mA)
- 2.5V gate drive devices.
- Small package (MPAK).

## Outline



## 2SJ486

### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	±10	V
Drain current	$I_D$	-0.3	A
Drain peak current	$I_{D(pulse)}^{*1}$	-0.6	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

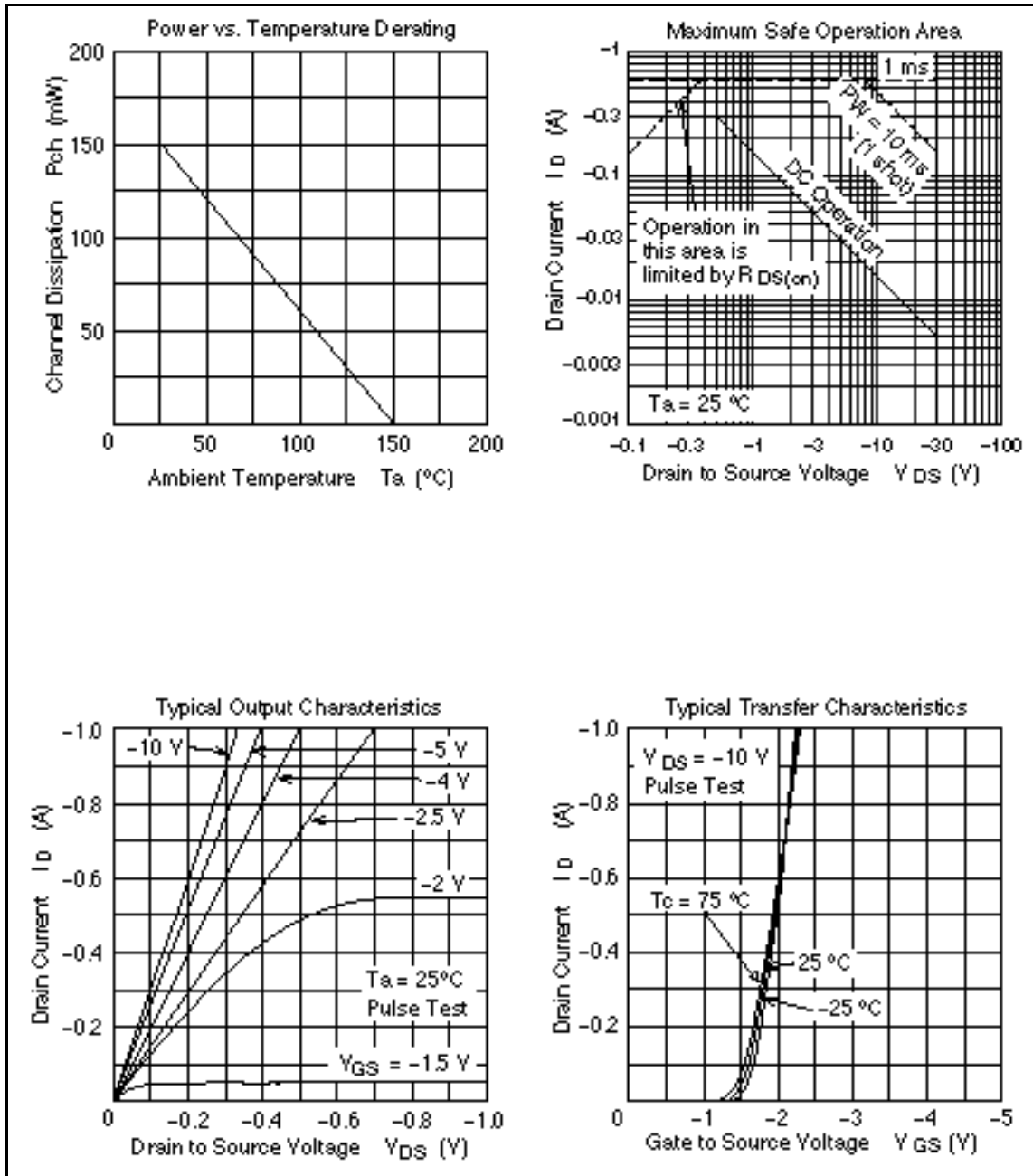
Note: 1. PW 10µs, duty cycle 1 %

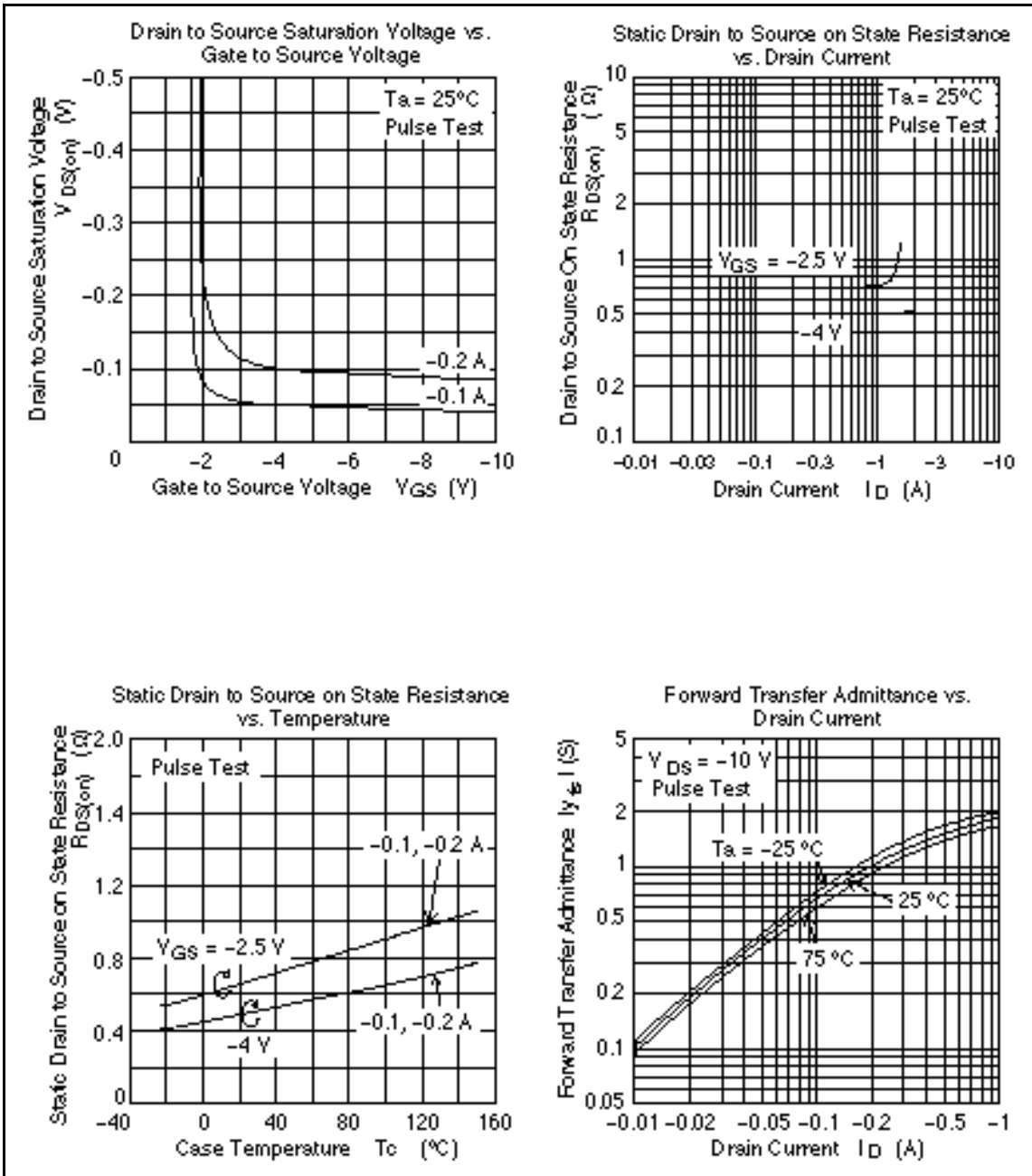
### Electrical Characteristics (Ta = 25°C)

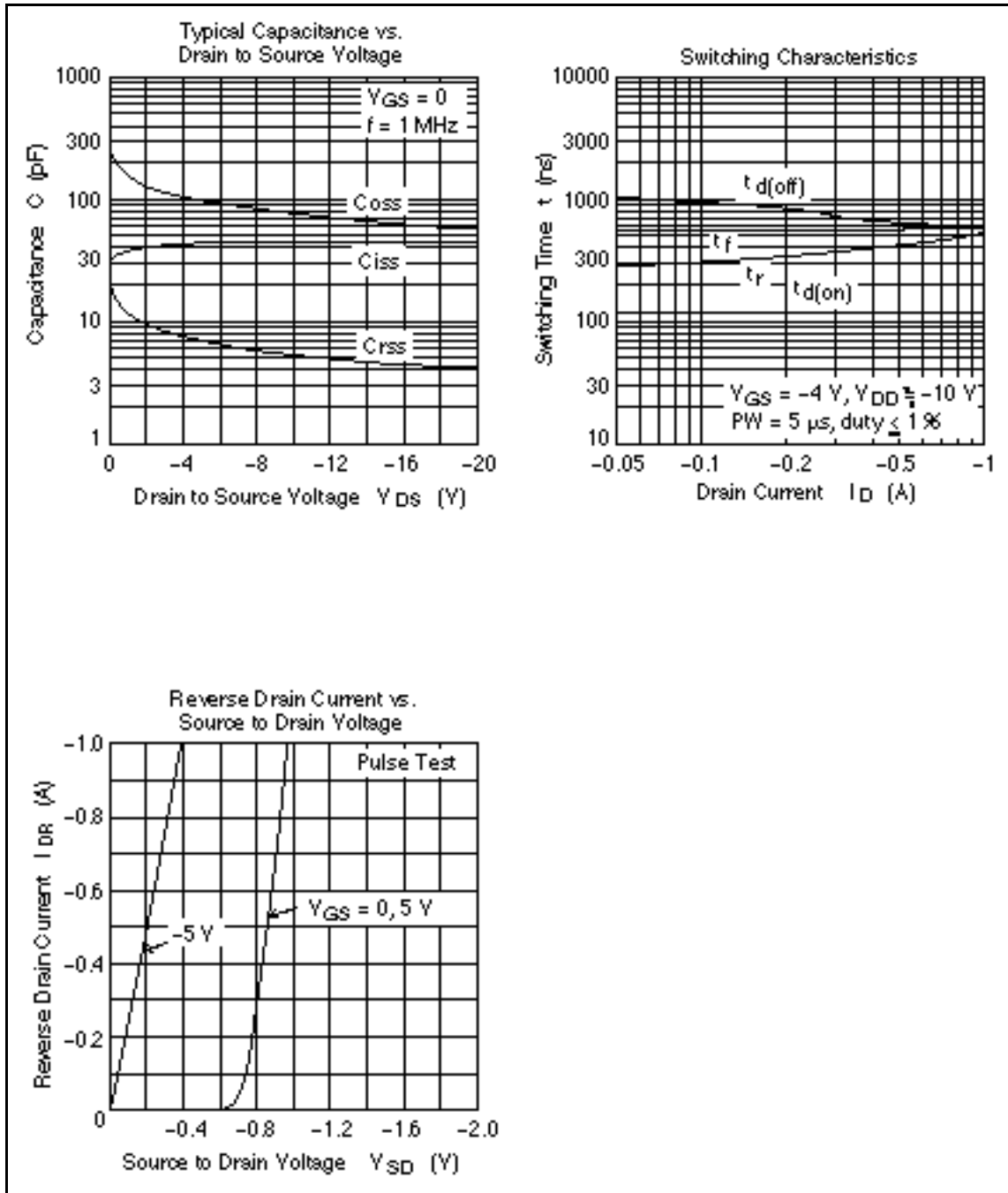
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10\mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100\mu A, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1.0	µA	$V_{DS} = -30 V, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5.0	µA	$V_{GS} = \pm 6.5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.5	—	-1.5	V	$I_D = -10\mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.5	0.65		$I_D = -100 mA$ $V_{GS} = -4 V^{*1}$
	$R_{DS(on)}$	—	0.7	1.2		$I_D = -40 mA$ $V_{GS} = -2.5 V^{*1}$
Forward transfer admittance	$ y_{fs} $	0.4	0.65	—	S	$I_D = -100 mA$ $V_{DS} = -10 V^{*1}$
Input capacitance	$C_{iss}$	—	45	—	pF	$V_{DS} = -10 V$
Output capacitance	$C_{oss}$	—	76	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	5.4	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	120	—	ns	$V_{GS} = -4 V$
Rise time	$t_r$	—	340	—	ns	$I_D = -150 mA$
Turn-off delay time	$t_{d(off)}$	—	850	—	ns	$R_L = 66.6$
Fall time	$t_f$	—	550	—	ns	

Notes: 1. Pulse test  
2. Marking is "ZU-".

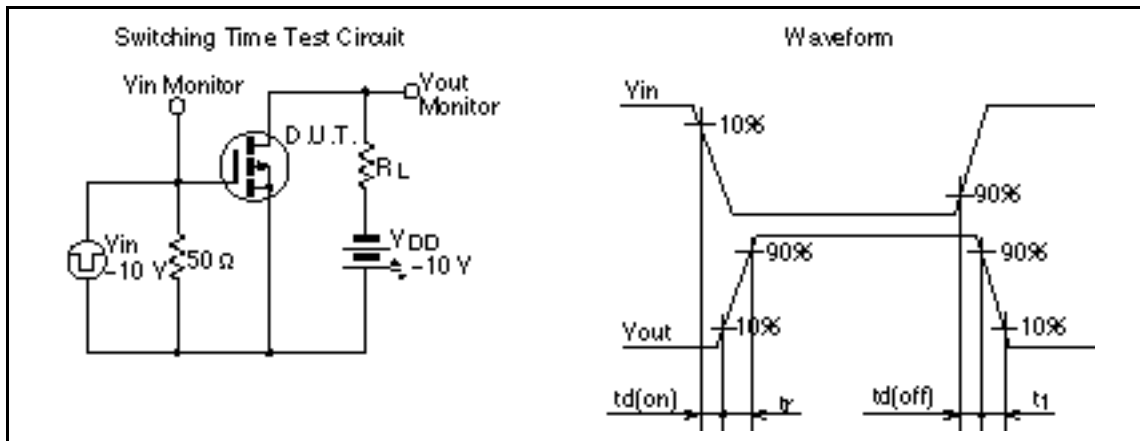
Main Characteristics





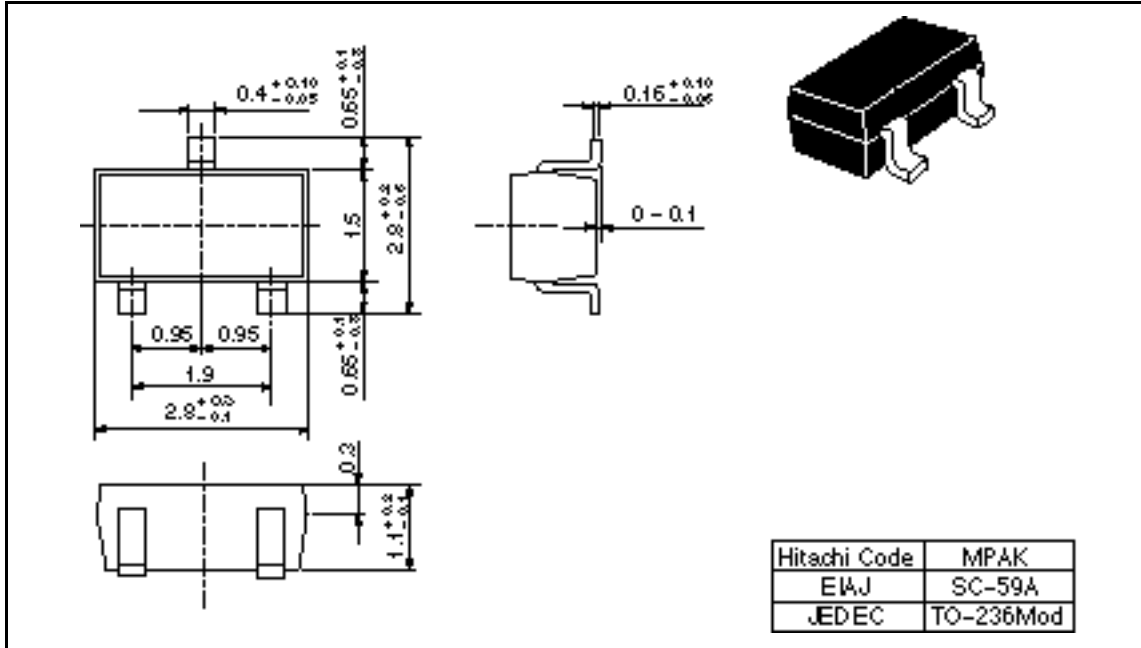


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Package Dimensions

Unit: mm



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