

Dual 90MHz 6-Bit Analog to Digital Converter

Preliminary Information

DS4067 - 1.4 May 1996

The VP213 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP213 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC and digital I/O that can be interfaced to either +5V or +3V. The VP213 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- TTL Clock/Data Interface
- 1 Volt Analog Input Range
- Internal ADC Reference
- Digital I/O's compatible with +5V or +3V logic
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP213A CG MP1S (Commercial - 28 pin plastic SO)

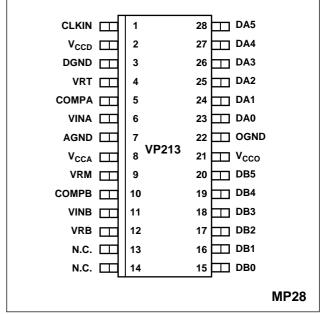


Fig.1 Pin connections - top view (wide body)

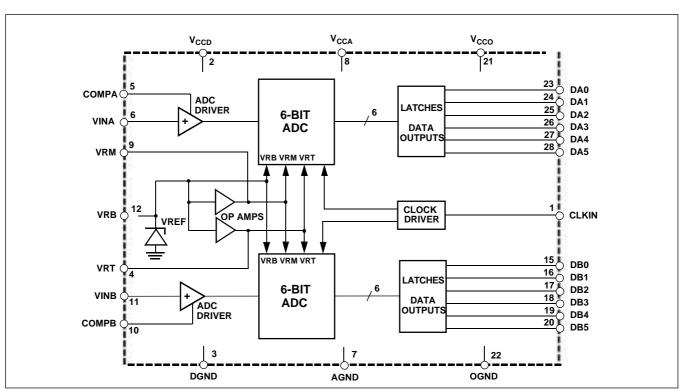


Fig.2 System block diagram

VP213

ABSOLUTE MAXIMUM RATINGS

THERMAL CHARACTERISTICS

DC supply voltage (V_{CCA} , V_{CCD} , V_{CCO}) -0.3 to+7V Analog input voltage (VIN) -0.3 to V_{CC} +0.3V Digital inputs (CLKIN) V_{CC} Digital output current (loh, lol, lsc) -20 to +20mA Ambient operating temperature (Tamb) 0°C to +70°C Storage temperature (Tstorage) -55°C to +125°C

THERMAL RESISTANCES

Junction to case(jc) 32°C/W

Junction to ambient(ja) 84°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25° C, $V_{CCA/D/O} = +5V$, full temperature range = 0° C to $+70^{\circ}$ C **DC CHARACTERISTICS** All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Min.	Value Typ.	Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	_	_	±0.5	LSB	
,		Full	4	-	_	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	_	_	±0.5	LSB	
		Full	4	_	_	±0.5	LSB	
No missing codes		Full	4		Guarantee			
Power supply								
Analog supply voltage	V_{CCA}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	V _{CCD}	Full	4	4.75	5.0	5.25	V	
Output supply voltage	V _{CCO}	Full	4	4.75	5.0	5.25	V	
Analog supply current	Alcc	+25°C	1 1	14	19	26	mA	
Analog supply current	Aicc	Full	4	_	-	_	mA	
Digital supply current	DI.	+25°C	1	34	42	51	mA	
Digital supply current	DI _{CC}			34	42	31		
0	01	Full	4	-	-	-	mA	
Output supply current	Olcc	+25°C	1	3	11	15	mA	
		Full	4	-	-	-	mA	
Power dissipation	PD	+25°C	1	260	360	460	mW	
Analog input								
Input range	V _{in}	Full	5	-	1.0	-	V	Pk to Pk
Input resistance	R _{in}	+25°C	1	20k	25k	30k		
Input capacitance	C _{in}	+25°C	5	-	4.0	-	pF	
Gain variation	G _V	+25°C	4	-	-	0.25	dB	Fin=300Hz to 20MHz
Gain matching	G	+25°C	1	_	_	0.25	dB	Fin=15.36MHz
Input -3dB bandwidth	G _m F3dB	+25°C	4	_	200	0.23	MHz	1 III-13.30IVII IZ
•	Aindc	+25°C	1	2.25	3.6	2.05	V	
Ain input voltage				3.35		3.85		
Comp output	Vcomp	+25°C	1	1.8	2.0	2.2	V	
CLKIN		_						
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V _{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	l _{ih}	+25°C	1	-	-	1	μΑ	$V_{CCD} = 5.25V$
		Full	4	-	-	-		$V_{in} = 2.7V$
Input current low	I _{il}	+25°C	1	-0.2	-0.35	-0.5	mA	$V_{CCD} = 5.25V$
·	"	Full	4	-	-	-		$V_{in} = 0.4V$
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	_	3.0	V	$V_{CCO} = 4.75V$
	- 011	Full	4		_	-	V	$I_{oh} = 400 \mu A$
Output voltage low	V _{ol}	+25°C	1	_	_	0.4	V	$V_{CCO} = 4.75V$
Juiput voitage iow	▼ ol	Full	4	_	_		V	$I_{ol} = 1mA$
Output current high	1	+25°C	1] -	-400	μA	$V_{CCO} = 4.75V$
Output current nigh	I _{oh}	Full	4	_	_	-400	μΑ -	1.700 = 4.70
Output current law		+25°C	1 1	_	<u> </u>	4		V _{CCO} = 4.75V
Output current low	l _{ol}			-	_	1	mA	VCCO = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Min.	Value Typ.	Max.	Units	Conditions
Reference voltage								
V _{ref} ladder bottom	VRB	+25°C	1	2.367	2.525	2.671	V	
V _{ref} ladder middle	VRM	+25°C	1	2.848	3.04	3.212	V	
V _{ref} ladder top	VRT	+25°C	1	3.337	3.55	3.763	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Min.	Value Typ.	Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	5.7	-	-	ns	
Clock low pulse width	$T_{pw}^{pn}0$	+25°C	4	5.7	-	-	ns	
Max. conversion rate	F _{max}	+25°C	1	90	-	-	MHz	
Data output setup time	T _{setup}	+25°C	4	4	6	8	ns	Cload=10pF
Data output hold time	Thold	+25°C	4	3	6	8	ns	Cload=10pF
Aperture delay	T _{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	T _{ad}	+25°C	4	-	0.25	0.5	ns	
Aperture jitter	T _{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance	-							
Differential non-linearity	DNL	+25°C	4	-0.95	-	+1.2	LSB	3
Integral non-linearity	INL	+25°C	4	-	-	±1	LSB	F _{CLK} =
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	90.11MHz
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	1
Effective No. of bits	ENOB	+25°C	1	5.0	5.6	-	bits	F _{IN} =
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	11.26MHz
Input offset	V _{os}	+25°C	1	-	±0.5	±1	LSB	
Error rate	BER	+25°C	5	-	10e ⁻⁸	-		

NOTES

1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the '011111' to '100000'B transition edge.

TEST LEVELS

Level 1 - 100% production tested.

Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.

Level 3 - Sample tested only.
Level 4 - Parameter is guaranteed by design and characterisation testing.

Level 5 - Parameter is typical value only.

Code	Input Voltage	Digital Output		
Code	1.0 Volt Full Scale	Binary		
00	Least positive valid input	000000		
01	-	000001		
•	•	•		
31	-	011111		
32	0	100000		
33	-	100001		
•	•	•		
62	-	111110		
63	Most positive valid input	111111		

Table 1: Output coding

VP213

PIN DESCRIPTIONS - 28 Pin Plastic SO Package

Pin	Name	Description				
1	CLKIN	TTL clock input				
2	V _{CCD}	Digital voltage supply for ADC's and input clock				
3	DGND	Digital ground				
4	VRT	Reference voltage- ladder top				
5	COMPA	Capacitor compensation - A channel				
6	VINA	Analog signal input - A channel				
7	AGND	Analog ground				
8	V_{CCA}	Analog voltage supply for drivers and references				
9	VRM	Reference voltage- ladder middle				
10	COMPB	Capacitor compensation - B channel				
11	VINB	Analog signal input - B channel				
12	VRB	Reference voltage- ladder bottom				
13	N.C.	Not connected				
14	N.C.	Not connected				
15	DB0	TTL digital output - channel B - LSB				
16	DB1					
17	DB2					
18	DB3					
19	DB4					
20	DB5	TTL digital output - channel B - MSB				
21	V _{cco}	Output voltage supply for TTL data outputs				
22	OGND	Output ground				
23	DA0	TTL digital output - channel A - LSB				
24	DA1					
25	DA2					
26	DA3					
27	DA4					
28	DA5	TTL digital output - channel A - MSB				

Table 2: Pin descriptions

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay

The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter

The sample to sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time

Data output timings are measured from the 50% threshold to the 50% threshold on the rising edge of the output clock.

Differential Non-linearity

The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

ENOB = SNR-1.76/6.02 o

ENOB = N-log2[rms error (actual)/rms error (ideal)]

where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.

Device Description

The VP213 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL compatible data outputs. The VP213 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

Analog Input

The analog inputs, (VIN_A,B) are A.C. coupled into the non-inverting input of the ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, VRM (3.00V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, bottom (VRB), middle (VRM) and top(VRT). VRB, VRM and VRT have been brought out to pins 12, 9 and 4 respectively and should be decoupled with 100nF capacitors close to the package pins.

ADC Circuit

The VP213 employs a 'flash' architecture consisting of a reference resistor chain, an array of 64 comparators, encoding logic and a 6-bit latch. The 63 reference levels generated by the resistor chain are compared with the analog output signal from the ADC driver amplifier using the comparator array. This produces a thermometer code which the encoding logic converts into a 6-bit word.

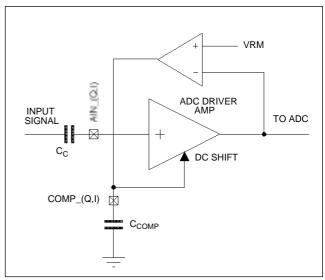


Fig.3 DC offset internal feedback loop

Digital Interface

The TTL data output pins, (DA0-DA5) and (DB0-DB5), have been optimized to interface with devices in close proximity to the VP213 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold times. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched on the rising edge of the input clock. Data is then presented to the TTL data outputs and latched on the falling edge of the input clock.

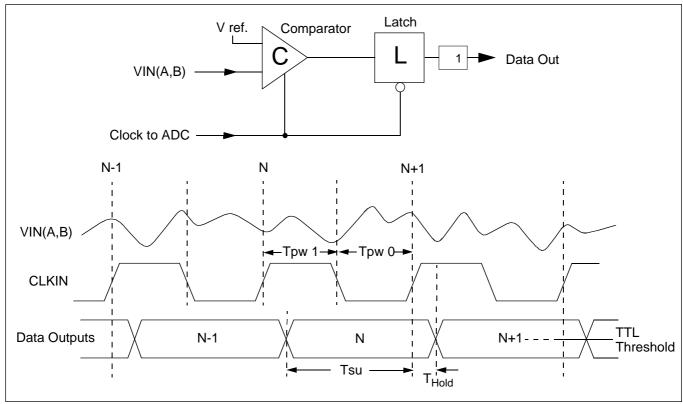


Fig.4 System timing diagram

Layout And Grounding

As with all high speed A to D converters, careful consideration must be given to the PCB layout. High performance can be obtained from the VP213 by tying all grounds to a solid low impedance ground plane. Separate analog and digital ground planes with a single common link under the device can also be used to help reduce the amount of digital noise fed back into the analog section of the

The VP213 should be decoupled with low impedance 100nF ceramic capacitors close to the package pins to avoid lead inductance effects and the decoupling on supply lines should further be improved by using a 47µF tantalum capacitor in parallel with a 100nF ceramic capacitor. If VCCA is derived from VCCD, a small inductor should be used to reduce digital noise on the analog power supply. Jitter and noise on clock input pins must be minimised. Long clock lines should therefore be avoided and all clock lines correctly terminated. Cross talk of digital signals to the analog inputs must also be prevented as sampling cross talk produces DC offsets on the sampled data, for this reason analog inputs should not be run next to clock or data lines. Device connections to the ground plane should be as short as possible.

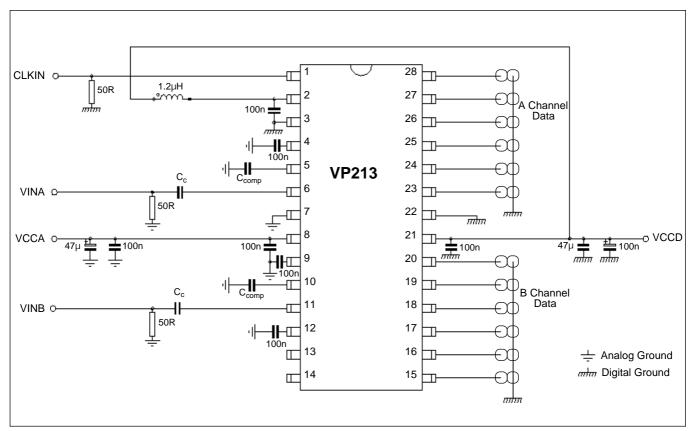


Fig.5 Applications diagram

Application Circuit

Fig.5 shows a typical applications circuit for the VP213. The supply connections are made using separate low noise digital and analog power supplies and VCCD is further isolated from VCCO using a 1.2µH inductor.

The COMPA and COMPB pins must be decoupled to reduce any ripple at low frequencies which may distort the ADC driver amplifier output, (see Fig.2.) The decoupling capacitor value is determined by the required low frequency performance of the system and can be obtained from the following equation.

$$C_{Comp} = \frac{75x10^{-6}}{F_{in} \times V_{Ripple}}$$

A ripple voltage 10mV is recommended for good system performance, e.g. If the analog input frequency F_{in}=

10KHz a value of $0.75\mu F$ is required for C_{Comp} . To ensure effective A.C. coupling at low input frequencies, the coupling capacitors on pins 6 and 11 can be calculated from the high pass filter corner frequency equation,

$$\frac{1}{2 \times \times RC}$$

where

F_c = Lower -3dB corner frequency (R = Input Resistance, 25K typ. - 20K min)



For more information about all Zarlink products visit our Web Site at

www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. trading as Zarlink Semiconductor or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I^2C components conveys a licence under the Philips I^2C Patent rights to use these components in an I^2C System, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Zarlink and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright 2002, Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE