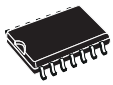
74LVQ74

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
  f_{MAX} = 250 MHz (TYP.) at V_{CC} = 3.3V
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:
  I_{CC} =2 µA (MAX.) at T_A=25°C
- LOW NOISE:
  V_{OLP} = 0.2 V (TYP.) at V_{CC} = 3.3V
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 12mA (MIN) at V_{CC} = 3.0V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY



SOP

TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVQ74M	74LVQ74MTR
TSSOP		74LVQ74TTR

DESCRIPTION

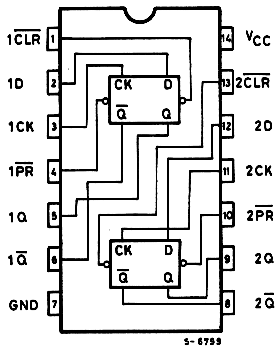
The 74LVQ74 is a low voltage CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and low noise 3.3V applications.

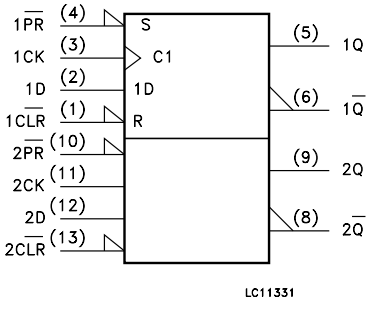
A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.

CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.

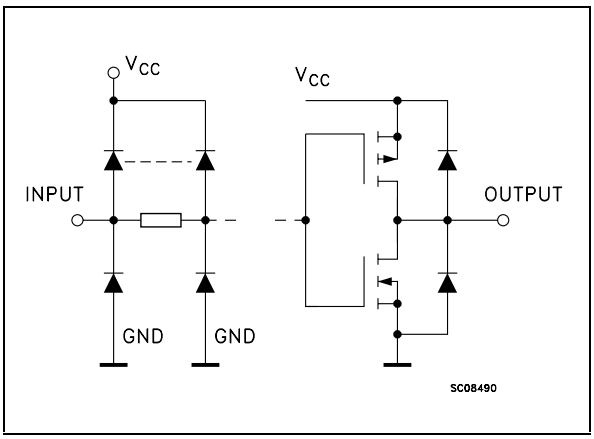
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

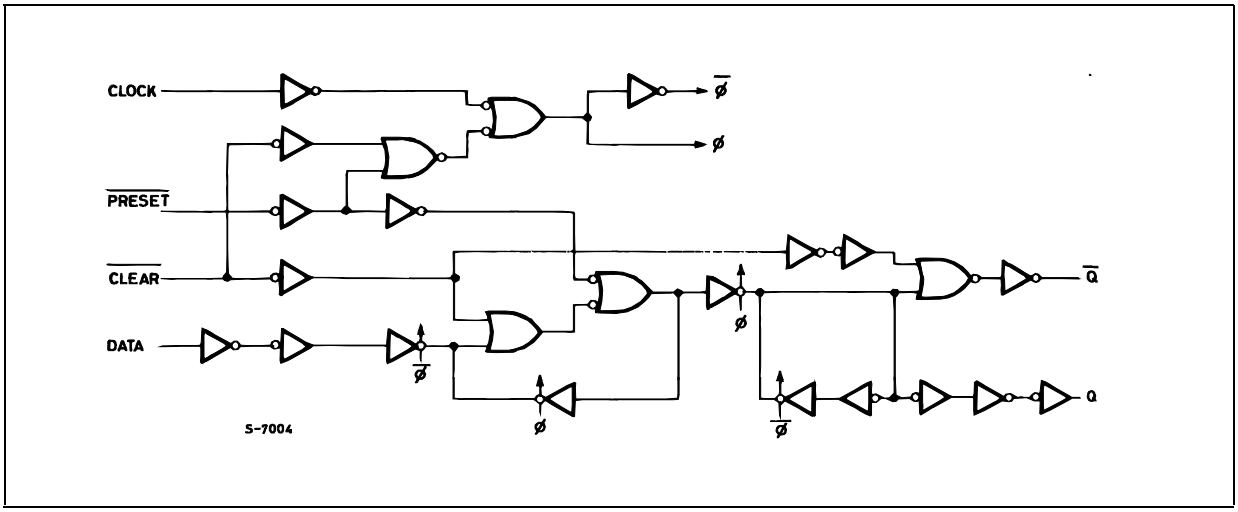
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, $2\overline{CLR}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW to HIGH, Edge Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐¬	L	H	
H	H	H	⌐¬	H	L	
H	H	X	¬⌐	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time V_{CC} = 3.0V (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	3.0 to 3.6		2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	3.0	I_O=-50 µA	2.9	2.99		2.9		2.9		V
			I_O=-12 mA	2.58			2.48		2.48		
			I_O=-24 mA				2.2		2.2		
V_{OL}	Low Level Output Voltage	3.0	I_O=50 µA		0.002	0.1		0.1		0.1	V
			I_O=12 mA		0	0.36		0.44		0.44	
			I_O=24 mA					0.55		0.55	
I_I	Input Leakage Current	3.6	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND			2		20		20	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	3.6	V_{OLD} = 0.8 V max				36		25		mA
I_{OHD}			V_{OHD} = 2 V min				-25		-25		mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75Ω

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.2	0.8					V
V_{OLV}				-0.8	-0.2						
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2							V
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					V

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q	2.7			7.7	12.0		14.0		16.0	ns
		3.3(*)			6.3	9.0		10.5		12.0	
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{PR}$ or $\overline{CLR}$ to Q	2.7			6.9	12.0		14.0		16.0	ns
		3.3(*)			5.8	9.0		10.5		12.0	
t_w	Pulse Width CK , HIGH or LOW	2.7		4.0	1.5		4.0		5.0		ns
		3.3(*)		3.0	1.5		3.0		4.0		
$t_{w(L)}$	Pulse Width $\overline{PR}$ or $\overline{CLR}$, LOW	2.7		4.0	1.5		4.0		5.0		ns
		3.3(*)		3.0	1.5		3.0		4.0		
t_s	Setup Time D to CK HIGH or LOW	2.7		4.0	-0.2		4.0		5.0		ns
		3.3(*)		3.0	-0.2		3.0		4.0		
t_h	Hold Time D to CK HIGH or LOW	2.7		2.0	0.2		2.0		2.0		ns
		3.3(*)		2.0	0.2		2.0		2.0		
t_{REM}	Recovery Time $\overline{PR}$ or $\overline{CLR}$ to Q	2.7		1.0	-1.0		1.0		1.0		ns
		3.3(*)		1.0	-1.0		1.0		1.0		
f_{MAX}	Maximum Clock Frequency	2.7		100	200		100		80		MHz
		3.3(*)		120	250		120		100		
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	2.7			0.2	1.0		1.0		1.0	ns
		3.3(*)			0.2	1.0		1.0		1.0	

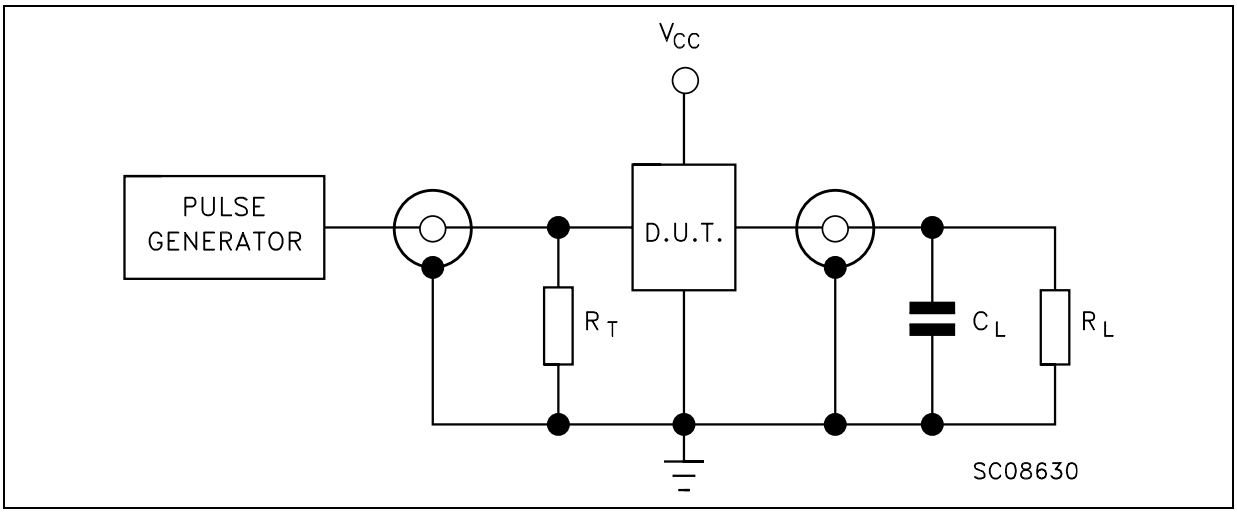
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			4						pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz		33						pF

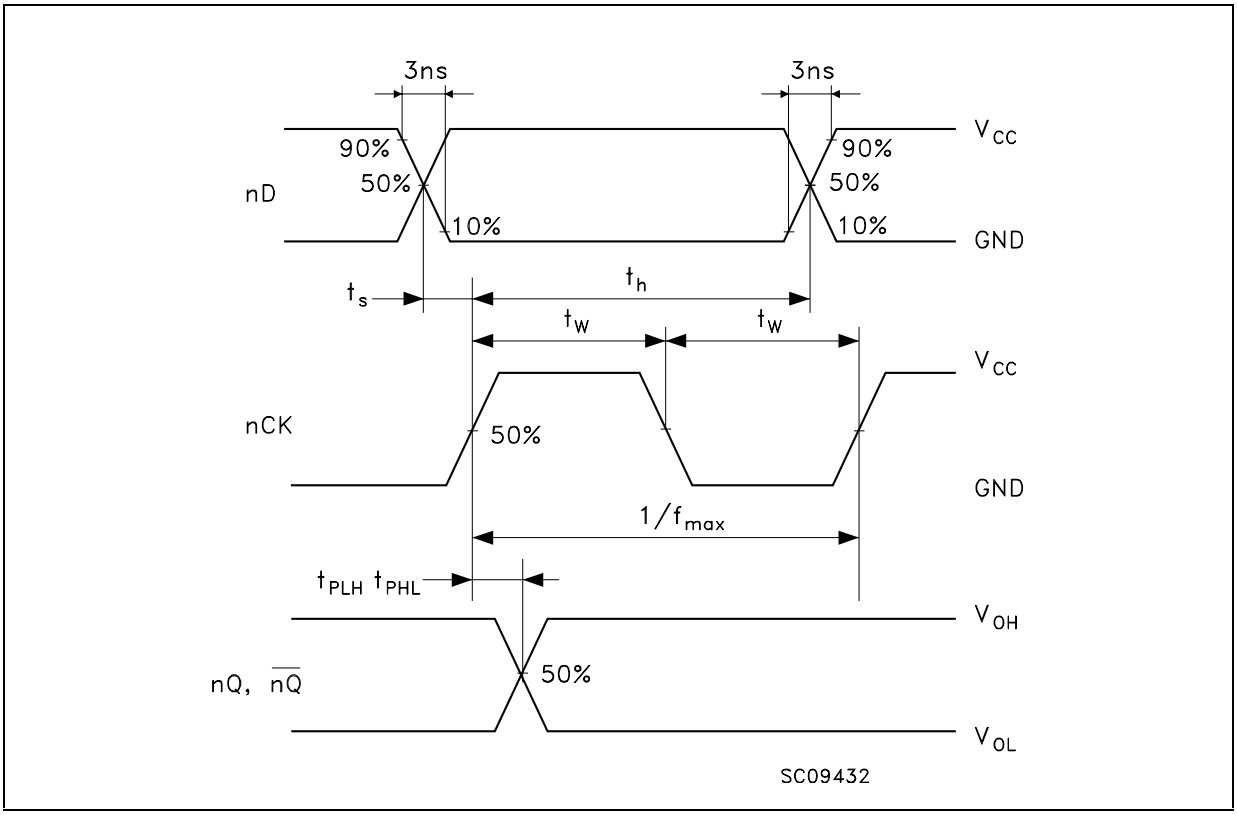
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

TEST CIRCUIT

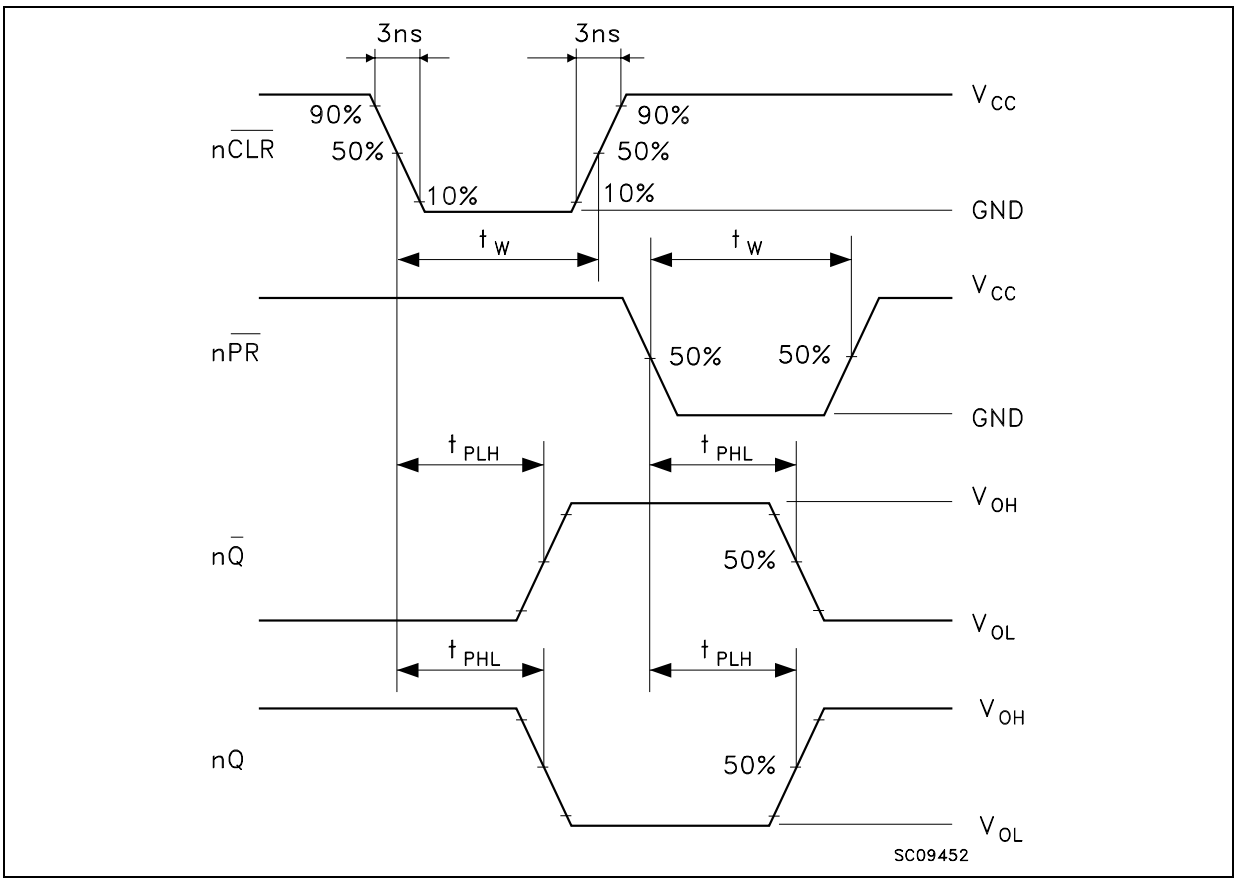


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

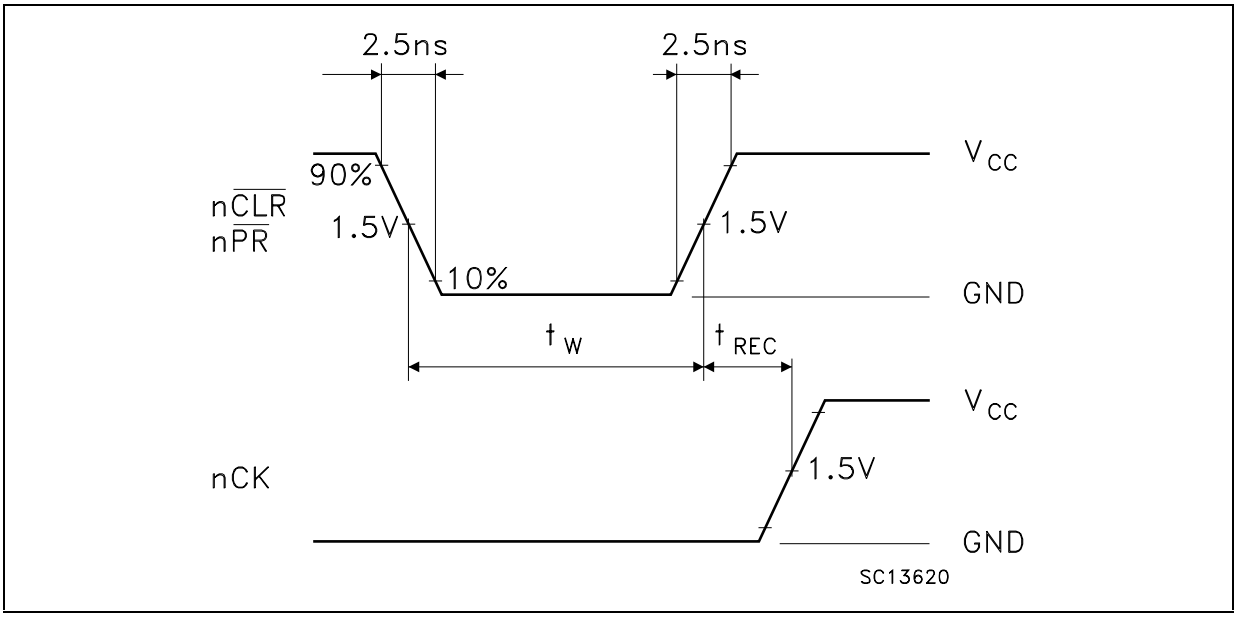
WAVEFORM1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz;50% dutycycle)



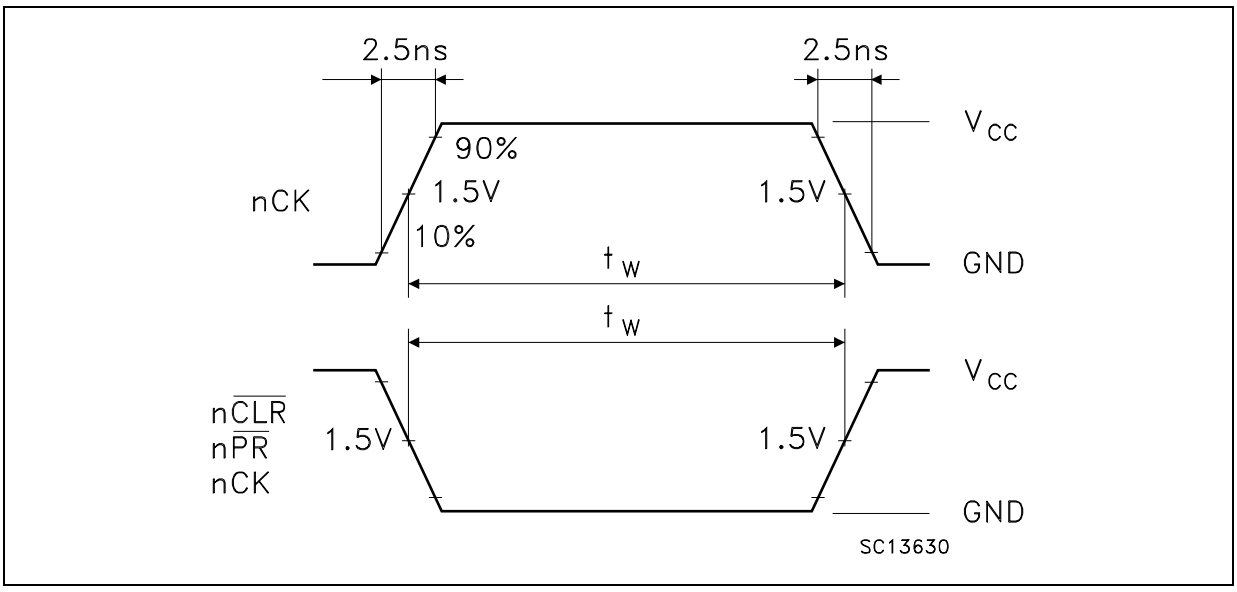
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: RECOVERY TIMES (f=1MHz; 50% duty cycle)

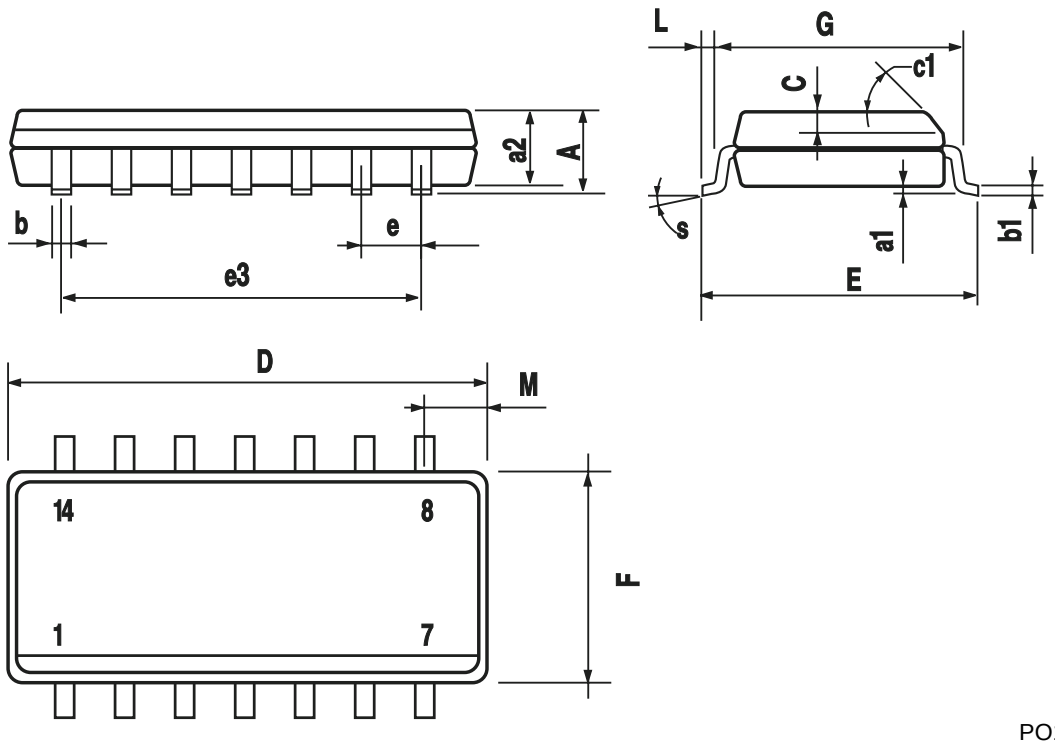


WAVEFORM 4: PULSE WIDTH



SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030