HB526A264DB Series

1,048,576-word × 64-bit × 2-bank Synchronous Dynamic RAM Module

HITACHI

ADE-203-607 (Z)
Preliminary
Rev. 0.1
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Description

The HB526A264DB is a 1M× 64 × 2 banks Synchronous Dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 8 pieces of 16-Mbit SDRAM (HM5216805TT/HM5216805LTT) sealed in TSOP package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). An outline of the HB526A264DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB526A264DB makes high density mounting possible without surface mount technology. The HB526A264DB provides common data inputs and outputs. Decoupling capacitors are mounted beside TSOP on the module board.

Features

- 144-pin Zig Zag Dual tabs socket type
  - Outline: 67.60 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - Lead pitch: 0.80 mm
- 3.3V power supply
- Clock frequency: 100 MHz / 83 MHz
- LVTTL interface
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length : 1/2/4/8/full page
- Programmable burst sequence
  - Sequential/interleave
- Full page burst length capability
  - Sequential burst
  - Burst stop capability
- Programmable $\overline{\text{CAS}}$ latency : 2/3
- Byte control by DQMB

Preliminary:The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

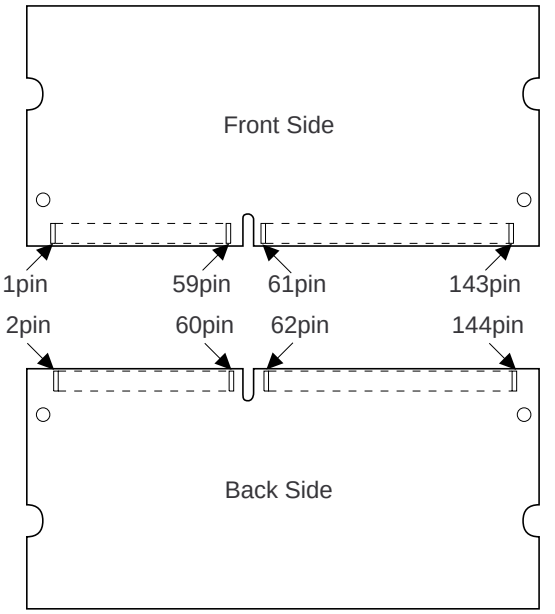
Hitachi semiconductor

- 4096 refresh cycles: 64 ms
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh
- Low self refresh current: HB526A264DB-10L (L-version)

Ordering Information

Type No.	Frequency	Package	Contact pad
HB526A264DB-10	100 MHz	Small outline DIMM (144-pin)	Gold
HB526A264DB-10L	100 MHz		
HB526A264DB-12	83 MHz		

Pin Arrangement



Pin Arrangement (cont.)

Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V_{SS}	73	NC	2	V_{SS}	74	CK1
3	DQ0	75	V_{SS}	4	DQ32	76	V_{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V_{DD}	10	DQ35	82	V_{DD}
11	V_{DD}	83	DQ16	12	V_{DD}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V_{SS}	20	DQ39	92	V_{SS}
21	V_{SS}	93	DQ20	22	V_{SS}	94	DQ52
23	DQMB0	95	DQ21	24	DQMB4	96	DQ53
25	DQMB1	97	DQ22	26	DQMB5	98	DQ54
27	V_{DD}	99	DQ23	28	V_{DD}	100	DQ55
29	A0	101	V_{DD}	30	A3	102	V_{DD}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11 (BS)
35	V_{SS}	107	V_{SS}	36	V_{SS}	108	V_{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10 (AP)	40	DQ41	112	NC
41	DQ10	113	V_{DD}	42	DQ42	114	V_{DD}
43	DQ11	115	DQMB2	44	DQ43	116	DQMB6
45	V_{DD}	117	DQMB3	46	V_{DD}	118	DQMB7
47	DQ12	119	V_{SS}	48	DQ44	120	V_{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V_{SS}	127	DQ27	56	V_{SS}	128	DQ59
57	NC	129	V_{DD}	58	NC	130	V_{DD}
59	NC	131	DQ28	60	NC	132	DQ60
61	CK0	133	DQ29	62	CKE0	134	DQ61
63	V_{DD}	135	DQ30	64	V_{DD}	136	DQ62
65	$\overline{RAS}$	137	DQ31	66	$\overline{CAS}$	138	DQ63

Front side				Back side			
Pin No.	**Signal name**	**Pin No.**	**Signal name**	**Pin No.**	**Signal name**	**Pin No.**	**Signal name**
67	$\overline{WE}$	139	V_{SS}	68	NC	140	V_{SS}
69	$\overline{S0}$	141	SDA	70	NC	142	SCL
71	NC	143	V_{DD}	72	NC	144	V_{DD}

Pin Description

Pin name	Function
A0 to A11	Address input — Row address A0 to A10 — Column address A0 to A8 — Bank select address A11
DQ0 to DQ63	Data-input/output
$\overline{S0}$	Chip select
$\overline{RAS}$	Row address asserted bank enable
$\overline{CAS}$	Column address asserted
$\overline{WE}$	Write enable
DQMB0 to DQMB7	Byte input/output mask
CK0/CK1	Clock input
CKE0	Clock enable
SDA	Data-input/output for serial PD
SCL	Clock input for serial PD
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	0	1	1	0B	11
4	Number of column addresses bits	0	0	0	0	1	0	0	1	09	9
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest $\overline{CAS}$ latency) 10 (10 ns)	1	0	1	0	0	0	0	0	A0	CL = 3
	12 (12 ns)	1	1	0	0	0	0	0	0	C0	
10	SDRAM access from Clock (highest $\overline{CAS}$ latency) -10 (7.5 ns)	0	1	1	1	0	1	0	1	75	
	-12 (9 ns)	1	0	0	1	0	0	0	0	90	
11	Module configuration type	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type	1	0	0	0	0	0	0	0	80	Normal (15.625 µs) Self refresh
13	SDRAM width	0	0	0	0	1	0	0	0	08	2M × 8
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00	—
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	8F	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	0	1	0	02	2
18	SDRAM device attributes: $\overline{CAS}$ latency	0	0	0	0	0	1	1	0	06	2, 3
19	SDRAM device attributes: $\overline{S0}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{WE}$ latency	0	0	0	0	0	0	0	1	01	0

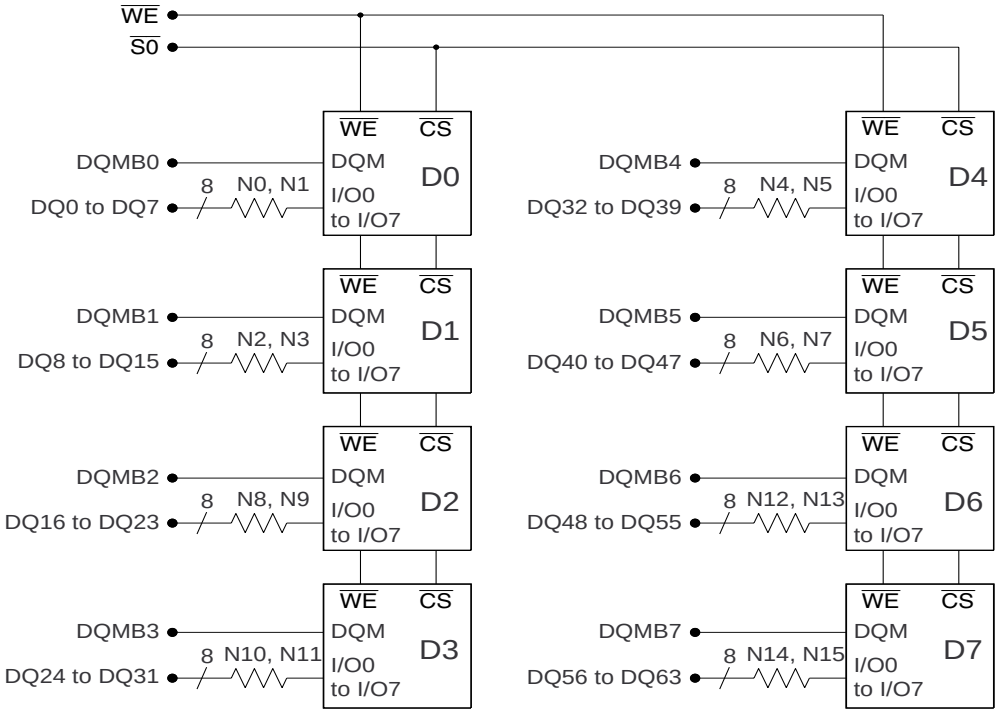
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00	Non buffer
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	$V_{CC} \pm 10\%$
23	SDRAM cycle time (2nd highest $\overline{CAS}$ latency) -10 (15 ns)	1	1	1	1	0	0	0	0	F0	CL = 2
	-12 (12 ns)	0	0	1	1	0	0	0	0	30	
24	SDRAM access from Clock (2nd highest $\overline{CAS}$ latency) -10 (9 ns)	1	0	0	1	0	0	0	0	90	
	-12 (12 ns)	1	1	0	0	0	0	0	0	C0	
25	SDRAM cycle time (3rd highest $\overline{CAS}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
26	SDRAM access from Clock (3rd highest $\overline{CAS}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time -10	0	0	0	1	1	1	1	0	1E	30 ns
	-12	0	0	1	0	0	1	0	0	24	36 ns
28	Row active to row active min -10	0	0	0	1	0	1	0	0	14	20 ns
	-12	0	0	0	1	1	0	0	0	18	24 ns
29	$\overline{RAS}$ to $\overline{CAS}$ delay min -10	0	0	0	1	1	1	1	0	1E	30 ns
	-12	0	0	0	1	1	1	1	0	1E	30 ns
30	Minimum $\overline{RAS}$ pulse width -10	0	0	1	1	1	1	0	0	3C	60 ns
	-12	0	1	0	0	1	0	0	0	48	72 ns
31	Density of each bank on module	0	0	0	0	0	1	0	0	04	16M byte
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	0	0	0	0	1	01	
63	Checksum for bytes 0 to 62 -10/10L	0	0	1	1	1	0	0	0	38	
	-12	1	1	1	1	1	0	0	1	F9	
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*[2] (ASCII-8bit code)

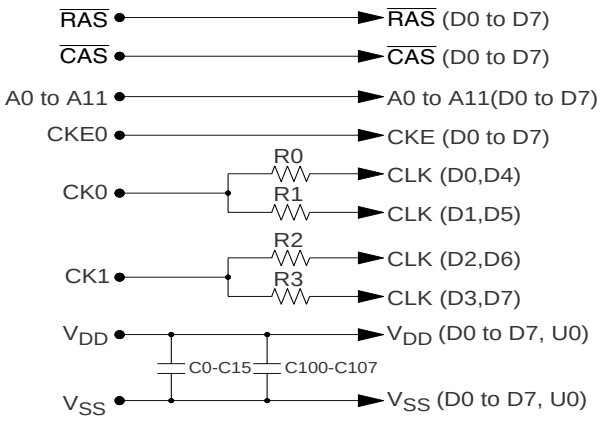
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
78	Manufacturer's part number	0	1	0	0	0	0	0	1	41	A
79	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
80	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number	0	0	1	1	0	1	0	0	34	4
82	Manufacturer's part number	0	1	0	0	0	1	0	0	44	D
83	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
84	Manufacturer's part number	0	1	0	1	1	1	1	1	5F	—
85	Manufacturer's part number	0	0	1	1	0	0	0	1	31	1
86	Manufacturer's part number	0	0	1	1	0	0	0	0	30	0
	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
87	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
	Manufacturer's part number (L-version)	0	1	0	0	1	1	0	0	4C	L
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (binary)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (binary)
95 to 98	Assembly serial number	*4									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*3
126	Intel specification frequency	0	1	1	0	0	1	1	0	66	66 MHz
127	Intel specification $\overline{\text{CAS}}$# latency support	0	0	0	0	0	1	1	0	06	CL = 2, 3

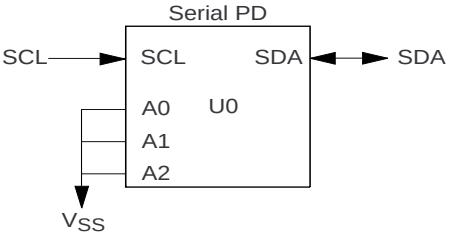
Notes: 1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High"

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows "J" on ASCII code.)
3. All bits of 99 through 125 are not defined ("1" or "0").
4. Bytes 95 through 98 are assembly serial number.

Block Diagram







Notes :
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D7 : HM5216805TT
U0 : 24C02
C0 to C17 : 0.33 μF
C100 to C107 : 0.1 μF
N0 to N15 : Network Resistors (10 Ω)
R0 to R3 : Chip Resistors

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{DD}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	8.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	3.0	3.3	3.6	V	1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	—	4.6	V	1, 2
Input low voltage	V_{IL}	–0.3	—	0.8	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns
3. V_{IL} (min) = –1.0 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526A264DB						
		-10/10L		-12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	800	—	680	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	—	24	—	24	mA	CKE0 = V_{IL}, t_{CK} = min	5
		—	16	—	16	mA	CKE0 = V_{IL} CK0/CK1 = V_{IL} or V_{IH} Fixed	6
		—	320	—	280	mA	CKE0 = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	56	—	56	mA	CKE0 = V_{IL}, t_{CK} = min, DQ = High-Z	1, 2
		—	360	—	320	mA	CKE0 = V_{IH}, NOP command t_{CK} = min, DQ = High-Z	1, 2, 3
Burst operating current ($\overline{CAS}$ Latency = 2)	I_{CC4}	—	800	—	680	mA	t_{CK} = min, BL = 4	1, 2, 4
($\overline{CAS}$ Latency = 3)	I_{CC4}	—	1200	—	1000	mA		
Refresh current	I_{CC5}	—	680	—	560	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	16	—	16	mA	$V_{IH} \geq V_{DD} - 0.2$ $V_{IL} \leq 0.2$ V	7
Self refresh current (L-version)	I_{CC6}	—	2	—	2	mA		
Input leakage current	I_{LI}	–10	10	–10	10	µA	$0 \leq Vin \leq V_{DD}$	
Output leakage current	I_{LO}	–10	10	–10	10	µA	$0 \leq Vout \leq V_{DD}$ DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CK0/CK1 cycles.
4. Input signal transition is once per one CK0/CK1 cycle.
5. After power down mode, CK0/CK1 operating current.
6. After power down mode, no CK0/CK1 operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address)	C_{IN}	60	pF	1, 3
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CK0/CK1, CKE0)	C_{IN}	60	pF	1, 3
Input capacitance ($\overline{S0}$)	C_{IN}	60	pF	1, 3
Input capacitance (DQMB0 to DQMB7)	C_{IN}	25	pF	1, 2, 3
Input/Output capacitance (DQ0 to DQ63)	$C_{I/O}$	20	pF	1, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526A264DB					
		-10/10L		-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
System clock cycle time ($\overline{CAS}$ Latency = 2)	t_{CK}	15	—	18	—	ns	1
($\overline{CAS}$ Latency = 3)	t_{CK}	10	—	12	—		
CK0/CK1 high pulse width	t_{CKH}	3	—	4	—	ns	1
CK0/CK1 low pulse width	t_{CKL}	3	—	4	—	ns	1
Access time from CK0/CK1 ($\overline{CAS}$ Latency = 2)	t_{AC}	—	9	—	12	ns	1, 2
($\overline{CAS}$ Latency = 3)	t_{AC}	—	7.5	—	9		
Data-out hold time	t_{OH}	3	—	3	—	ns	1, 2
CK0/CK1 to Data-out low impedance	t_{LZ}	0	—	0	—	ns	1, 2, 3
CK0/CK1 to Data-out high impedance	t_{HZ}	—	7	—	9	ns	1, 4
Data-in setup time	t_{DS}	2	—	3	—	ns	1
Data in hold time	t_{DH}	1	—	1	—	ns	1
Address setup time	t_{AS}	2	—	3	—	ns	1
Address hold time	t_{AH}	1	—	1	—	ns	1
CKE0 setup time	t_{CES}	2	—	3	—	ns	1, 5
CKE0 setup time for power down exit	t_{CESP}	2	—	3	—	ns	1
CKE0 hold time	t_{CEH}	1	—	1	—	ns	1

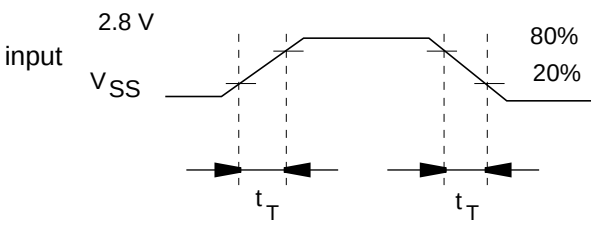
AC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

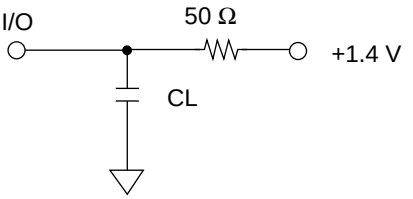
		HB526A264DB					
		-10/10L		-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Command ($\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQMB) setup time	t_{CS}	2	—	3	—	ns	1
Command ($\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQMB) hold time	t_{CH}	1	—	1	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	—	108	—	ns	1
Active to precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to precharge on full page mode	t_{RASC}	—	120000	—	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	36	—	ns	1
Precharge to active command period	t_{RP}	30	—	36	—	ns	1
Write recovery or data in to precharge lead time	t_{DPL}	15	—	18	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	—	24	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is C_L = 50 pF with current source.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE0 setup time to CKE0 rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures





Relationship Between Frequency and Minimum Latency

Parameter		HB526A264DB						
		-10/10L			-12			
Frequency (MHz)		100	66	33	83	55	28	
t_{CK} (ns)	Symbol	10	15	30	12	18	36	Notes
Active command to column command (same bank)	t_{RCD}	3	2	1	3	2	1	1
Active command to active command (same bank)	t_{RC}	9	6	3	9	6	3	= [t_{RAS} + t_{RP}] 1
Active command to precharge command (same bank)	t_{RAS}	6	4	2	6	4	2	1
Precharge command to active command (same bank)	t_{RP}	3	2	1	3	2	1	1
Write recovery or data input to precharge command (same bank)	t_{DPL}	2	1	1	2	1	1	1
Active command to active command (different bank)	t_{RRD}	2	2	1	2	2	1	1
Self refresh exit time	I_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	I_{APW}	5	3	2	5	3	2	= [t_{DPL} + t_{RP}]
Self refresh exit to command input	I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance ($\overline{CAS}$ latency = 3)	I_{HZP}	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	I_{HZP}	—	2	2	—	2	2	
Last data out to active command (auto precharge) (same bank)	I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge) ($\overline{CAS}$ latency = 3)	I_{EP}	–2	–2	–2	–2	–2	–2	
($\overline{CAS}$ latency = 2)	I_{EP}	—	–1	–1	—	–1	–1	
Column command to column command	I_{CCD}	1	1	1	1	1	1	
Write command to data in latency	I_{WCD}	0	0	0	0	0	0	
DQMB to data in	I_{DID}	0	0	0	0	0	0	
DQMB to data out	I_{DOD}	2	2	2	2	2	2	
CKE0 to CK0/CK1 disable	I_{CLE}	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency (cont)

Parameter		HB526A264DB						
		-10/10L			-12			
Frequency (MHz)		**100**	**66**	**33**	**83**	**55**	**28**	
t_{CK} (ns)	**Symbol**	**10**	**15**	**30**	**12**	**18**	**36**	**Notes**
Register set to active command	t_{RSA}	1	1	1	1	1	1	
$\overline{S0}$ to command disable	I_{CDD}	0	0	0	0	0	0	
Power down exit to command input	I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold ($\overline{CAS}$ latency = 3)	I_{BSR}	2	2	2	2	2	2	
($\overline{CAS}$ latency = 2)	I_{BSR}	—	1	1	—	1	1	
Burst stop to output high impedance ($\overline{CAS}$ latency = 3)	I_{BSH}	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	I_{BSH}	—	2	2	—	2	2	
Burst stop to write data ignore	I_{BSW}	0	0	0	0	0	0	

Notes: 1. t_{RCD} to t_{RRD} are recommended value.

2. When self refresh exit is executed, CKE0 should be kept “H” longer than I_{SREX} from exit cycle.

Pin Functions

CK0/CK1 (input pin): CK0/CK1 is the master clock input to this pin. The other input signals are referred at CK0/CK1 rising edge.

$\overline{S0}$ (input pin): When $\overline{S0}$ is Low, the command input cycle becomes valid. When $\overline{S0}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): Although these pin names are the same as those of conventional DRAM modules, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A10 (input pins): Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK0/CK1 rising edge. Column address (AY0 to AY8) is determined by A0 to A8 level at the read or write command cycle CK0/CK1 rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.

A11 (input pin): A11 is a bank select signal (BS). The memory array of the HB526A264DB is divided into bank 0 and bank 1, both which contain 2048 row × 512 column × 8 bits. If A11 is Low, bank 0 is selected, and if A11 is High, bank 1 is selected.

CKE0 (input pin): This pin determines whether or not the next CK0/CK1 is valid. If CKE0 is High, the next CK0/CK1 rising edge is valid. If CKE0 is Low, the next CK0/CK1 rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63 (DQ pins): Data is input to and output from these pins. These pins are the same as those of a conventional DRAM module.

V_{DD} (power supply pins): 3.3 V is applied.

V_{SS} (power supply pins): Ground is connected.

Command Operation

Command Truth Table

The synchronous DRAM module recognizes the following commands specified by the $\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE0 n - 1	CKE0 n	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0 to A9
Ignore command	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop in full page	BST	H	×	L	H	H	L	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	×	L	H	L	H	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	×	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	H	×
Refresh	REF/SELF	H	V	L	L	L	H	×	×	×
Mode register set	MRS	H	×	L	L	L	L	V	V	V

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}. V: Valid address input

Ignore command [DESL]: When this command is set ($\overline{S0}$ is High), the synchronous DRAM module ignore command input at the clock. However, the internal status is held.

No operation [NOP]: This command is not an execution command. However, the internal operations continue.

Burst stop in full-page [BST]: This command stops a full-page burst operation (burst length = full-page (512)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for a full-page of data (512), it automatically returns to the start address, and input/output is performed repeatedly.

Column address strobe and read command [READ]: This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY8) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READ A]: This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4, or 8. When the burst length is full-page (512), this command is illegal.

Column address strobe and write command [WRIT]: This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY8) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY8) and the bank select address (A11).

Write with auto-precharge [WRIT A]: This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation. When the burst length is full-page (512), this command is illegal.

Row address strobe and bank activate [ACTV]: This command activates the bank that is selected by A11 (BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated.

Precharge selected bank [PRE]: This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

Refresh [REF/SELF]: This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE0 truth table section.

Mode register set [MRS]: Synchronous DRAM module has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQMB Truth Table

Function	Symbol	CKE0 n - 1	n	DQMB
Write enable/output enable	ENB	H	×	L
Write inhibit/output disable	MASK	H	×	H

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
I_{DOD} is needed.

The HB526A264DB series can mask input/output data by means of DQMB During reading, the output buffer is set to Low-Z by setting DQMB to Low, enabling data output. On the other hand, when DQMB is set to High, the output buffer becomes High-Z, disabling data output. During writing, data is written by setting DQMB to Low. When DQMB is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMB. For details, refer to the DQMB control section of the HB526A264DB operating instructions.

CKE0 Truth Table

Current state	Function	CKE0 n-1	CKE0 n	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	×	×	×	×
Any	Clock suspend	L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit	L	H	×	×	×	×	×
Idle	Auto refresh command REF	H	H	L	L	L	H	×
Idle	Self refresh entry SELF	H	L	L	L	L	H	×
Idle	Power down entry	H	L	L	H	H	H	×
		H	L	H	×	×	×	×
Self-refresh	Self refresh exit SELFX	L	H	L	H	H	H	×
		L	H	H	×	×	×	×
Power down	Power down exit	L	H	L	H	H	H	×
		L	H	H	×	×	×	×

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

Clock suspend mode entry: The synchronous DRAM module enters clock suspend mode from active mode by setting CKE0 to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ A suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT A suspend: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend: During clock suspend mode, keep the CKE0 to Low.

Clock suspend mode exit: The synchronous DRAM module exits from clock suspend mode by setting CKE0 to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and completed precharge operation.

Auto refresh command [REF]: When this command is input from the IDLE state, the synchronous DRAM module starts auto refresh operation. (The auto refresh is the same as the CBR refresh of conventional DRAM module.) During the auto refresh operation, refresh address and bank select address are generated inside the synchronous DRAM module. For every auto refresh cycle, the internal address counter is updated. Accordingly, 4096 times are required to refresh the entire memory. Before executing the auto refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto refresh, no precharge command is required after auto refresh.

Self refresh entry [SELF]: When this command is input during the IDLE state, the synchronous DRAM module starts self refresh operation. After the execution of this command, self refresh continues while CKE0 is Low. Since self refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the synchronous DRAM module enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

Self refresh exit: When this command is executed during self refresh mode, the synchronous DRAM module can exit from self refresh mode. After exiting from self refresh mode, the synchronous DRAM module enters the IDLE state.

Power down exit: When this command is executed at the power down mode, the synchronous DRAM module can exit from power down mode. After exiting from power down mode, the synchronous DRAM module enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM module.

Current state	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	×	×	×	×	DESL	Enter IDLE after t_{RP}
	L	H	H	H	×	NOP	Enter IDLE after t_{RP}
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set

Current state	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Row active	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and new read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Current state	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and new read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and new write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*[2]
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto refresh)	H	×	×	×	×	DESL	Enter IDLE after t_{RC}
	L	H	H	H	×	NOP	Enter IDLE after t_{RC}
	L	H	H	L	×	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{DPL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOR] or [BST]: When these commands are executed, the synchronous DRAM module enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM module enters refresh mode (auto refresh or self refresh).

To [MRS]: The synchronous DRAM module enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM module to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM module enters precharge mode.

From [READ with AUTO PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM module then enters precharge mode.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM module then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

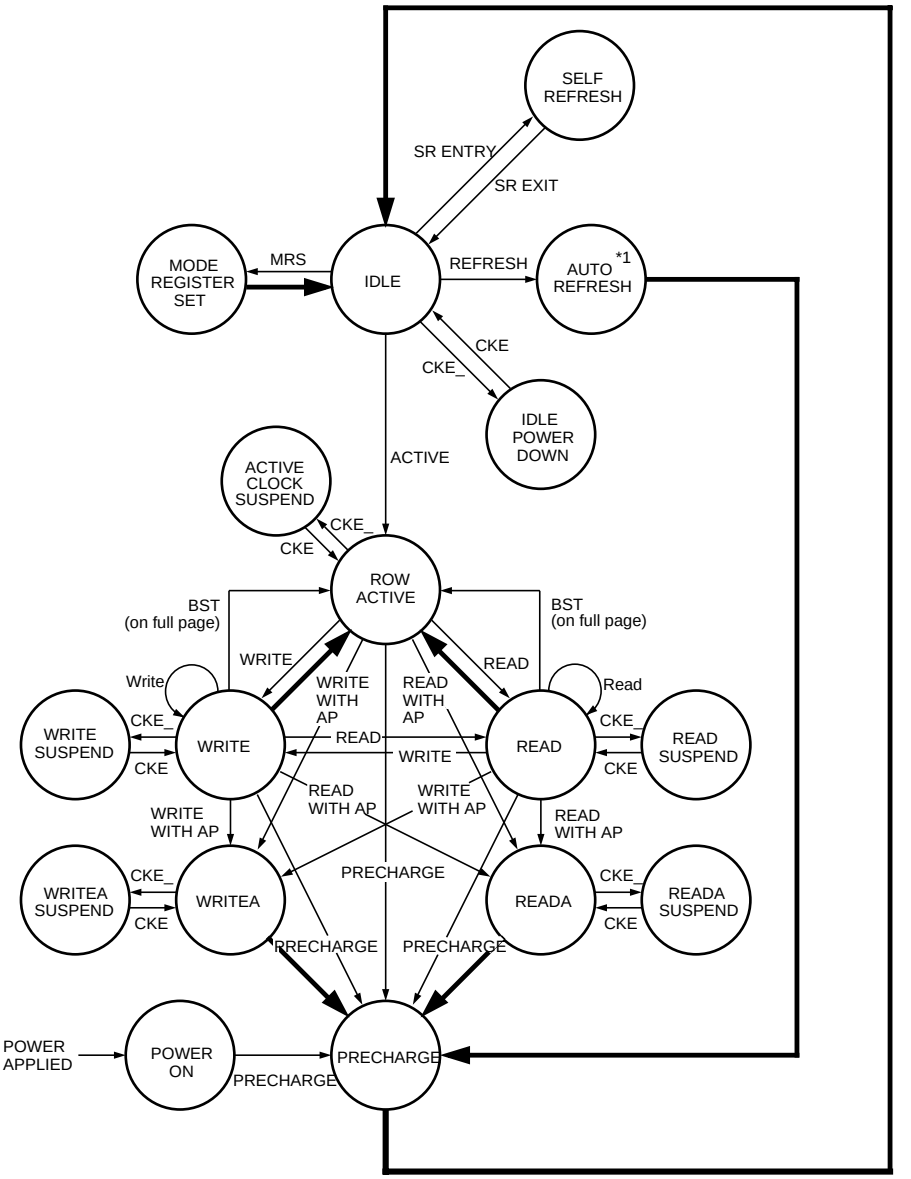
To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the synchronous DRAM module enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM module automatically enters the IDLE state.

Simplified State Diagram



Automatic transition after completion of command.

Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A11, A10, A9, A8: (OPCODE): The synchronous DRAM module has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and BURST WRITE: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

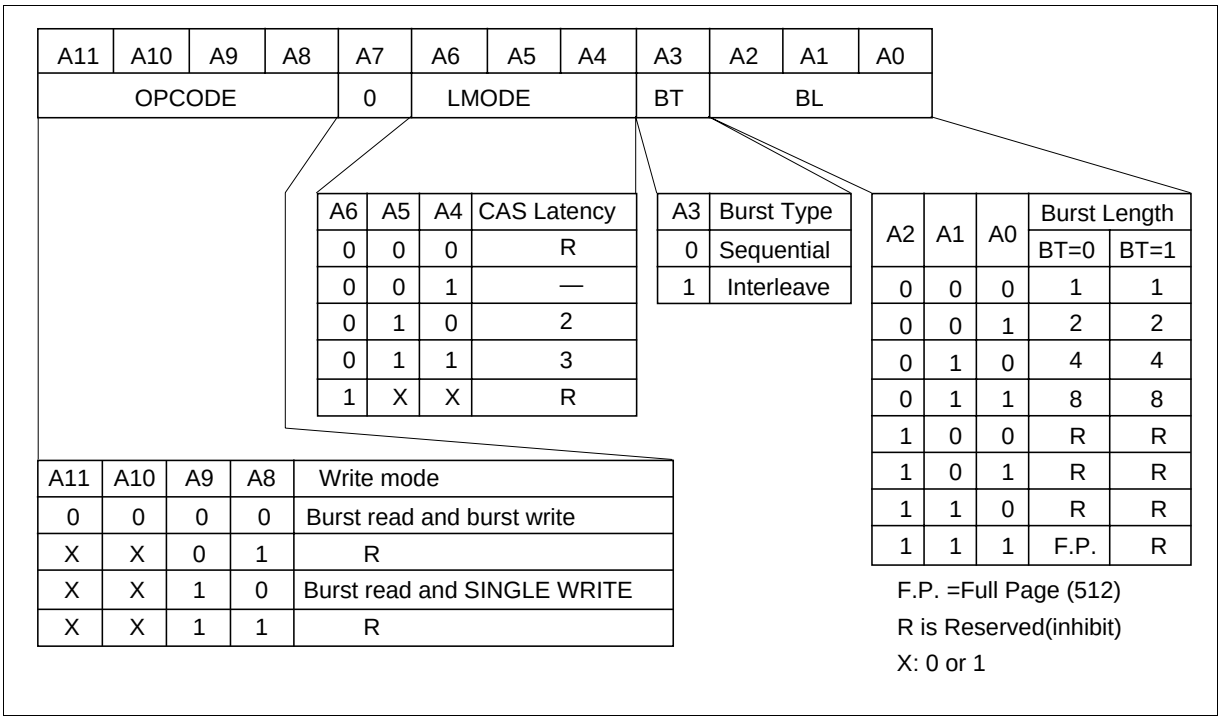
Burst read and SINGLE WRITE: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle.

A6, A5, A4: (LMODE): These pins specify the $\overline{\text{CAS}}$ latency.

A3: (BT): A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

A2, A1, A0: (BL): These pins specify the burst length.



A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE				0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	—
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A11	A10	A9	A8	Write mode
0	0	0	0	Burst read and burst write
X	X	0	1	R
X	X	1	0	Burst read and SINGLE WRITE
X	X	1	1	R

F.P. =Full Page (512)
R is Reserved(inhibit)
X: 0 or 1

Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

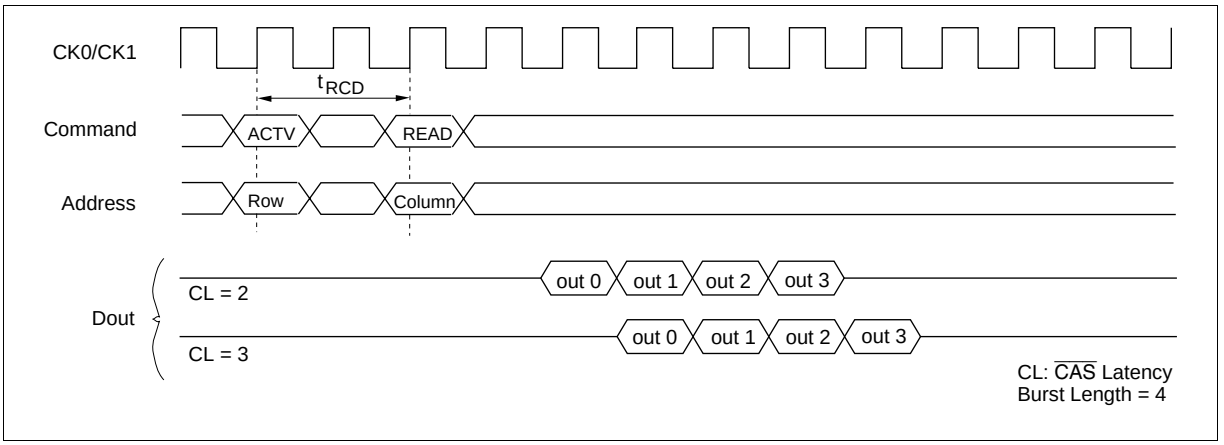
Operation of HB526A264DB Series

Read/Write Operations

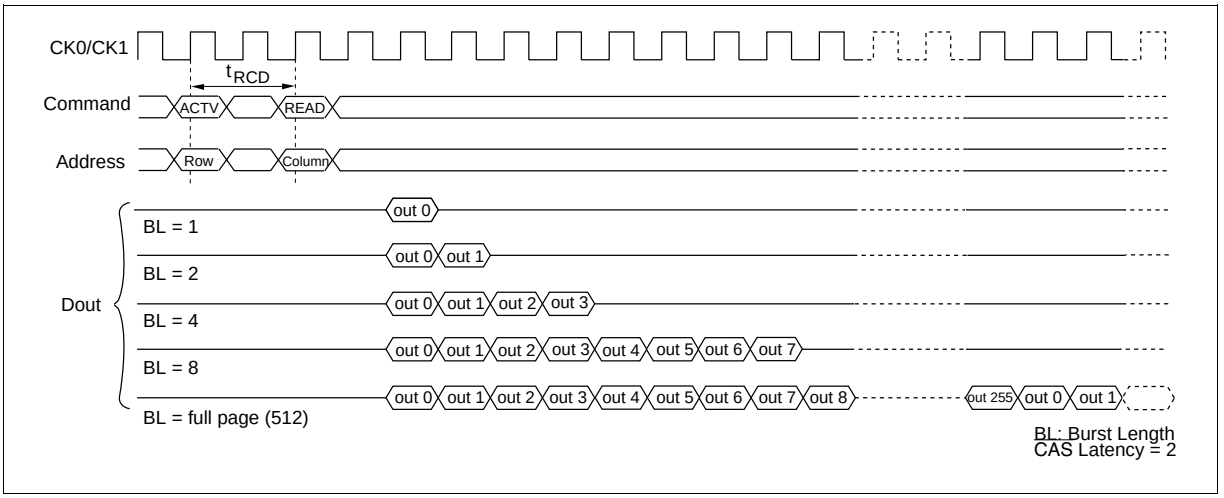
Bank active: Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A11 pin, and the row address (AX0 to AX10) is activated by the A0 to A10 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

Read operation: A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency-1) cycle after read command set. HB526A264DB series can perform a burst read operation. The burst length can be set to 1, 2, 4, 8 or full-page (512). The start address for a burst read is specified by the column address (AY0 to AY8) and the bank select address (A11) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 2 or 3. When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output. When the burst length is full-page (512), data is repeatedly output until the burst stop command is input. The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency



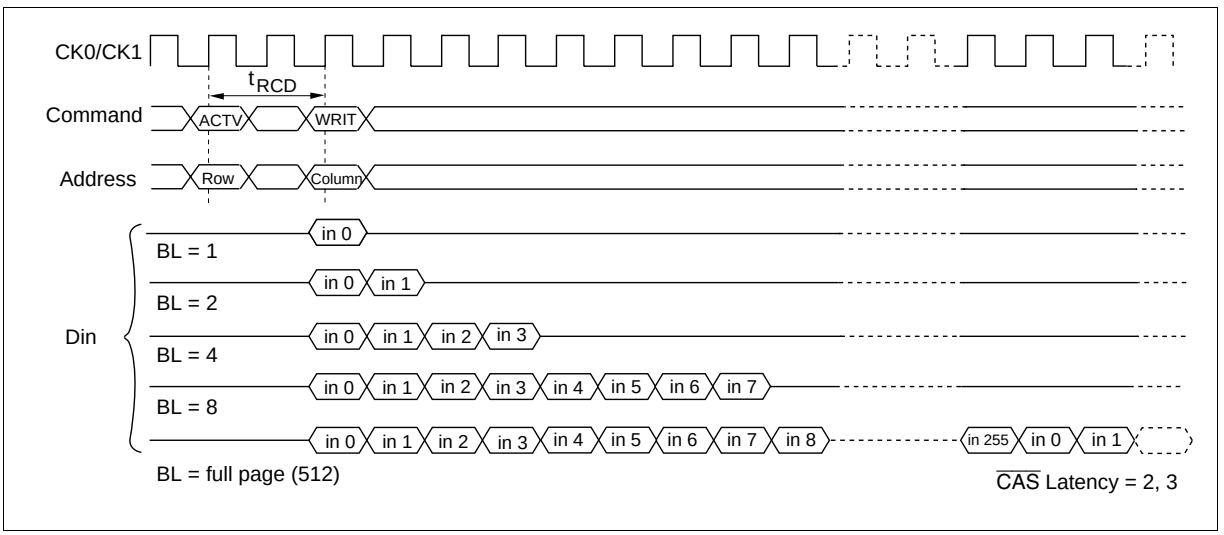
Burst Length



Write operation: Burst write or single write mode is selected by the OPCODE (A11, A10, A9, A8) of the mode register.

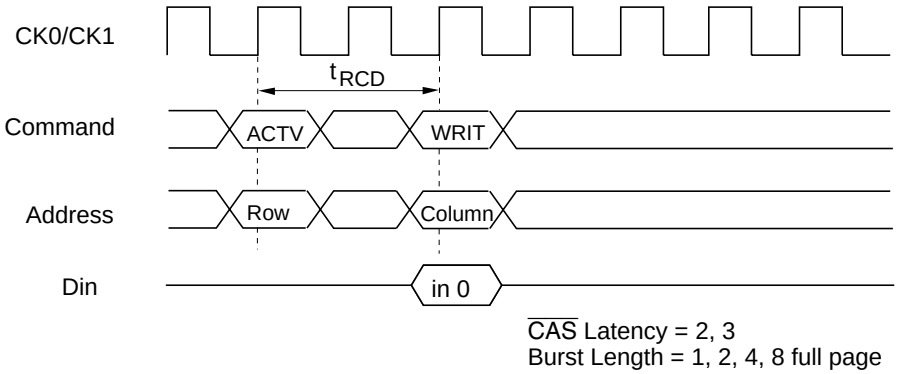
Burst write

A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address (AY0 to AY8) and the bank select address (A11) at the write command set cycle.



Single write

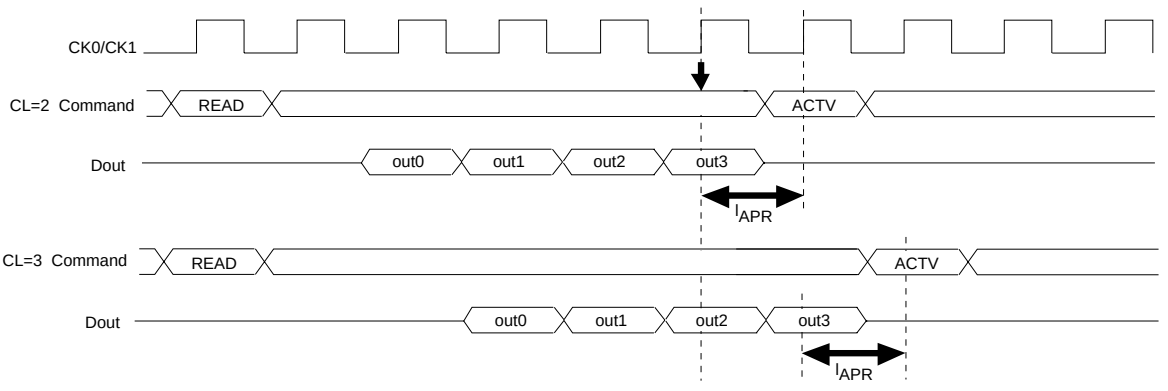
A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY8) and the bank select address (A11) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).



Auto Precharge

Read with auto precharge: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by I_{APR} is required before execution of the next command.

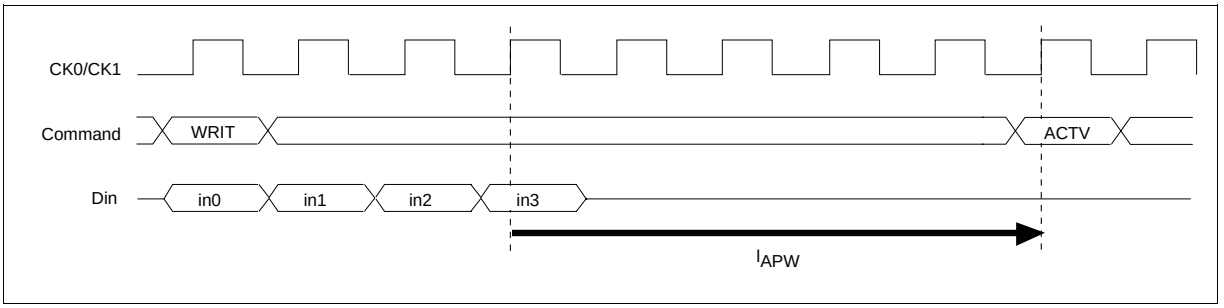
$\overline{\text{CAS}}$ latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output



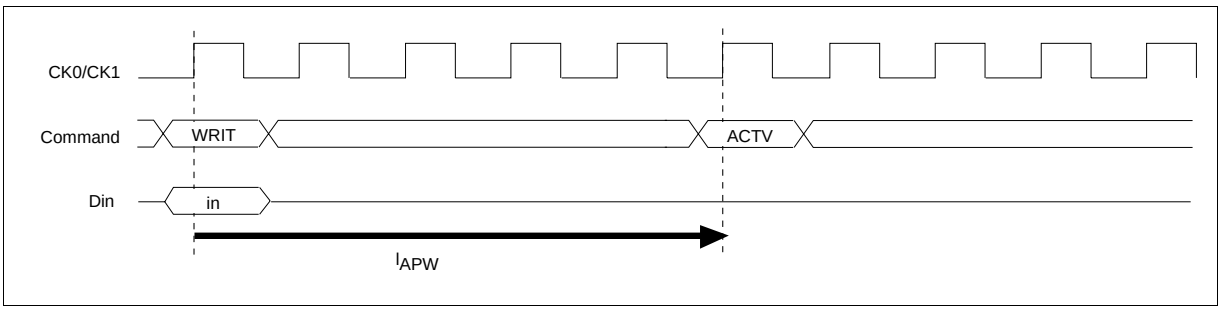
Note: Internal auto-precharge starts at the timing indicated by "↓".
At CLK = 50 MHz (I_{APR} changes depending on the operating frequency.)

Write with auto precharge: In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of I_{APW} is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write

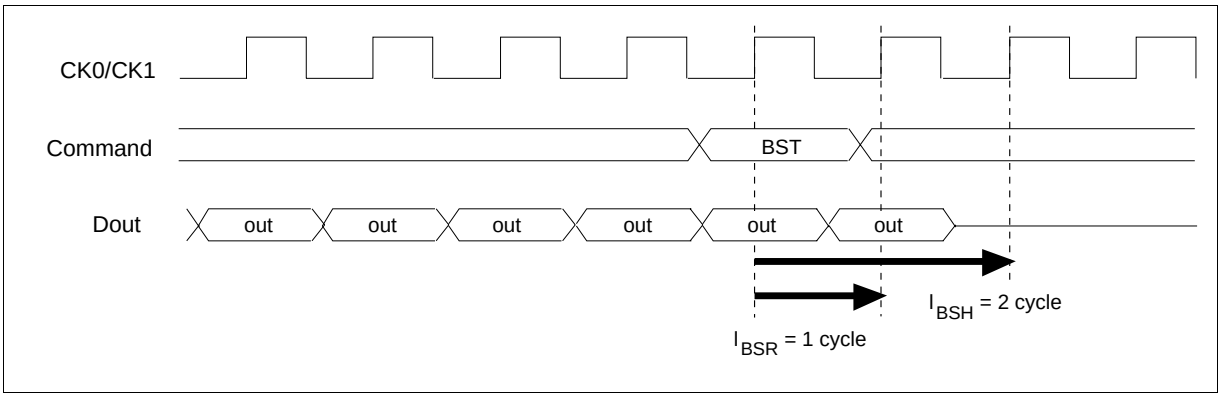


Full-page Burst Stop

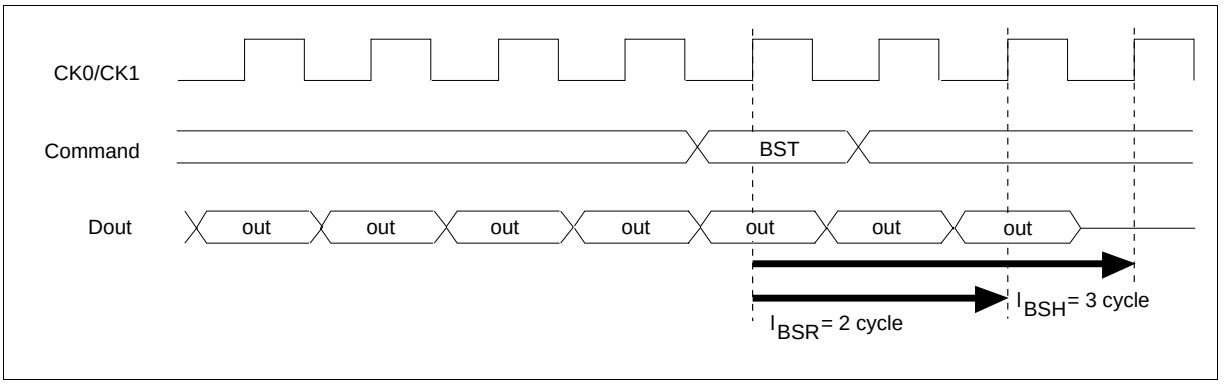
Burst stop command during burst read: The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read. The timing from command input to the last data changes depending on the $\overline{\text{CAS}}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths 1, 2, 4 and 8.

$\overline{\text{CAS}}$ latency	BST to valid data	BST to high impedance
2	1	2
3	2	3

$\overline{\text{CAS}}$ Latency = 2, Burst Length = full page

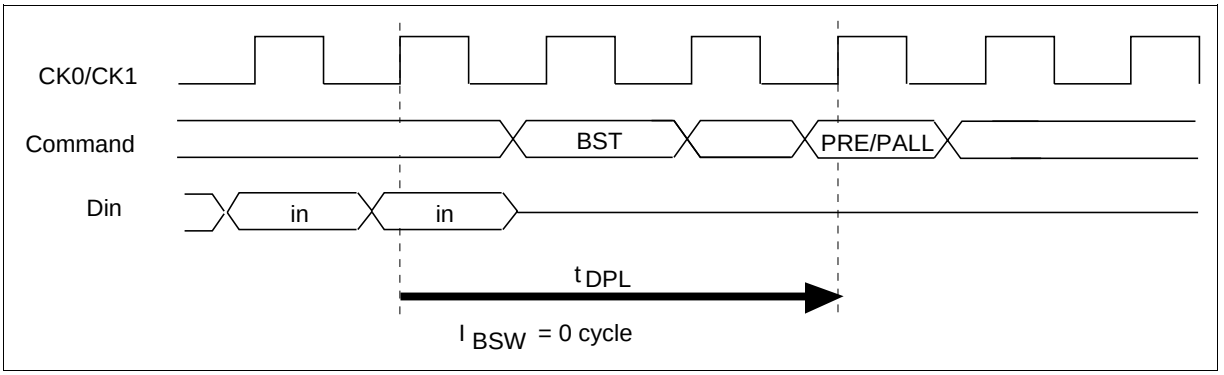


$\overline{\text{CAS}}$ Latency = 3, Burst Length = full page



Burst stop command at burst write: The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command and in subsequent cycles. In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4 and 8. And an interval of t_{DPL} is required between the BST command and the next precharge command.

Burst Length = full page

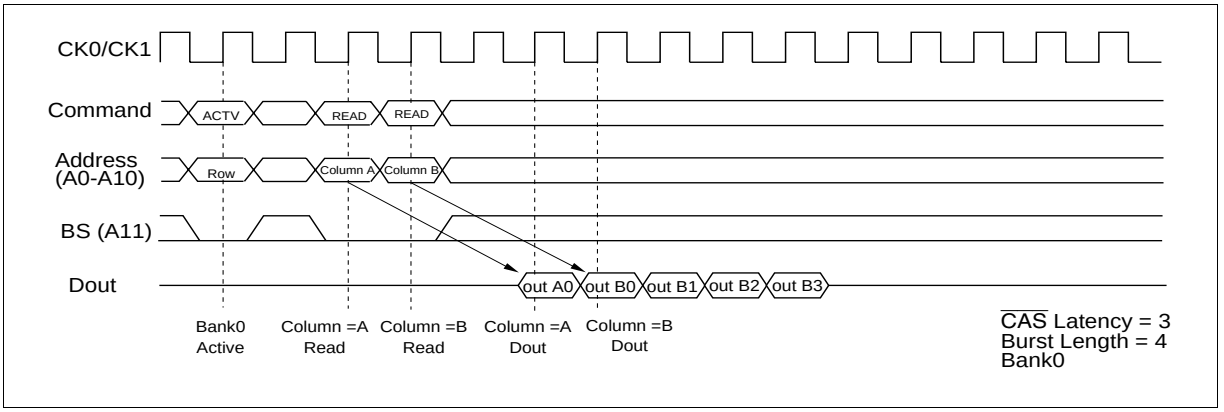


Command Intervals

Read command to Read command interval:

Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

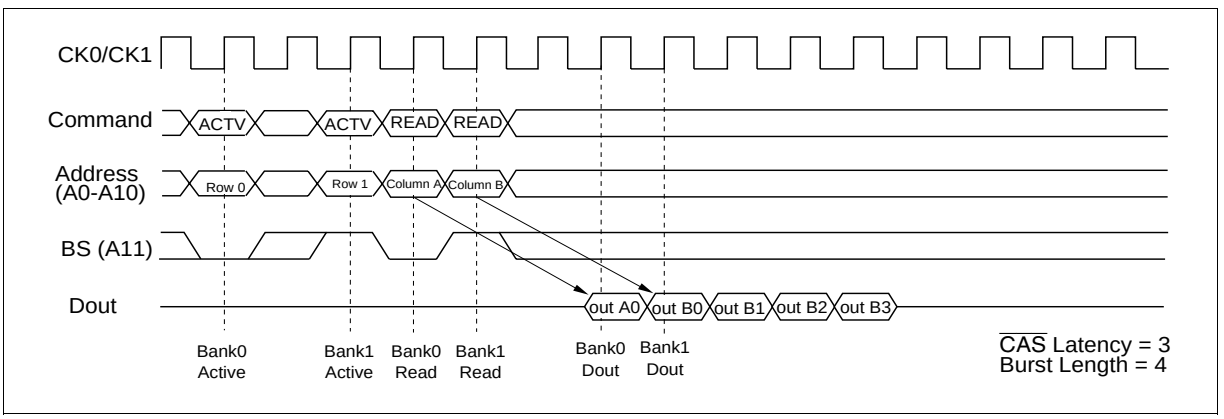
READ to READ Command Interval (same ROW address in same bank)



Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

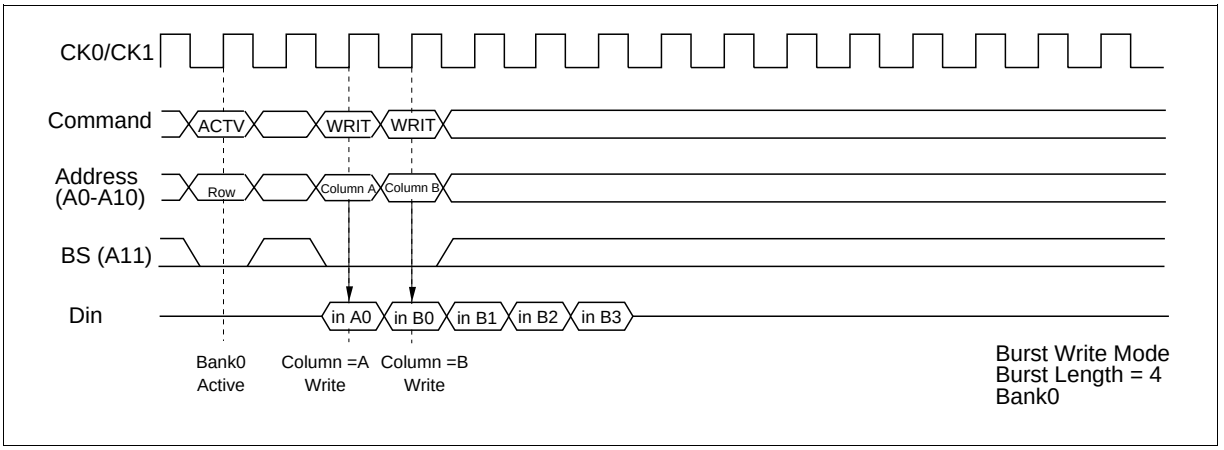
READ to READ Command Interval (different bank)



Write command to Write command interval:

Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle. In the case of burst writes, the second write command has priority.

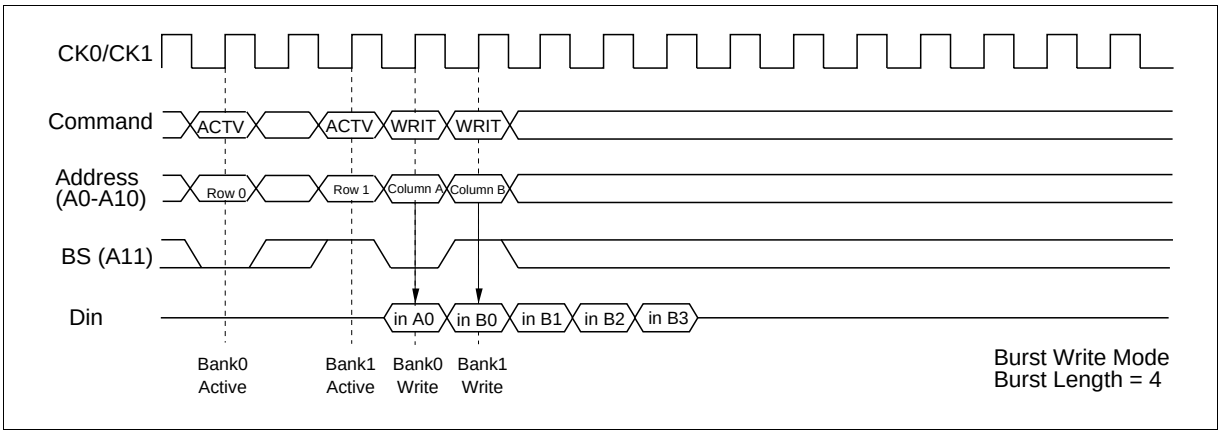
WRITE to WRITE Command Interval (same ROW address in same bank)



Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

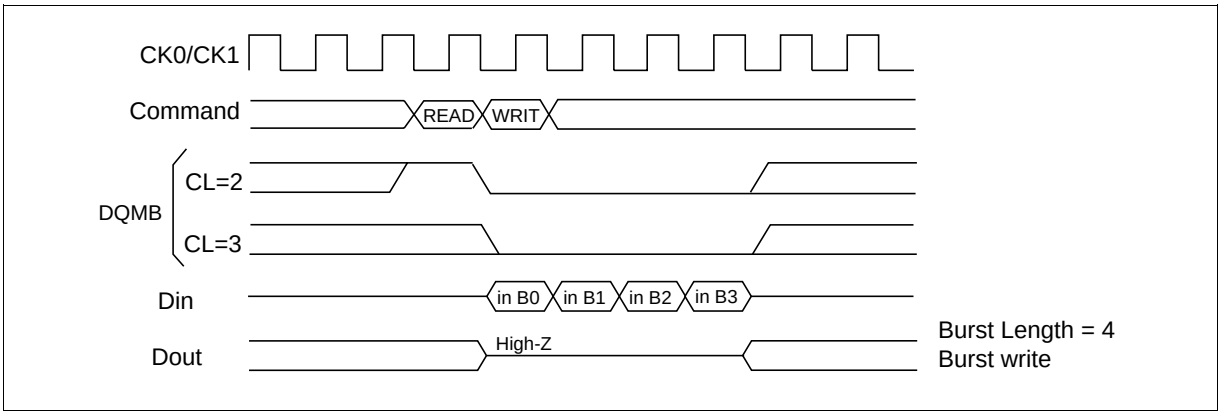
WRITE to WRITE Command Interval (different bank)



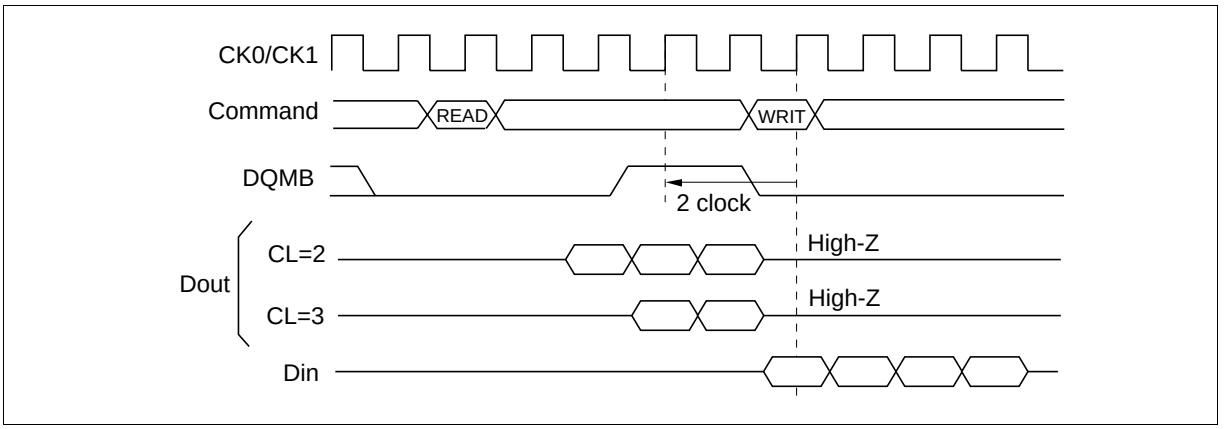
Read command to Write command interval:

Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQMB must be set High so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)



READ to WRITE Command Interval (2)



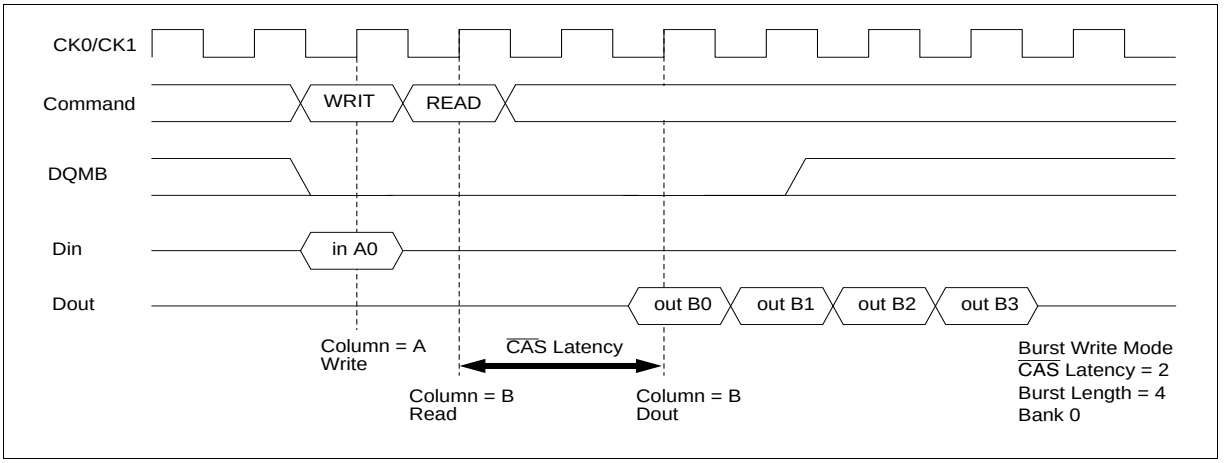
Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQMB must be set High so that the output buffer becomes High-Z before data input.

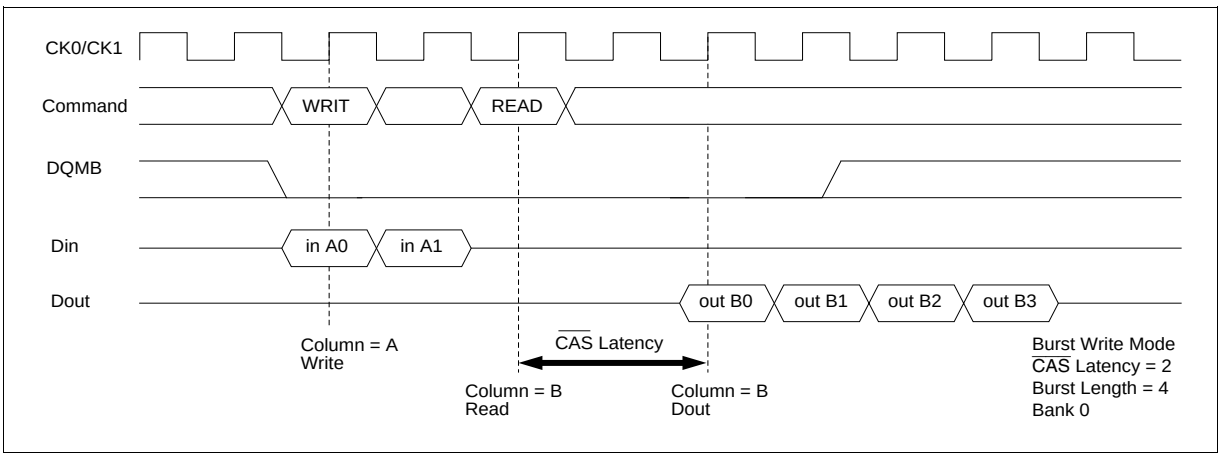
Write command to Read command interval:

Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



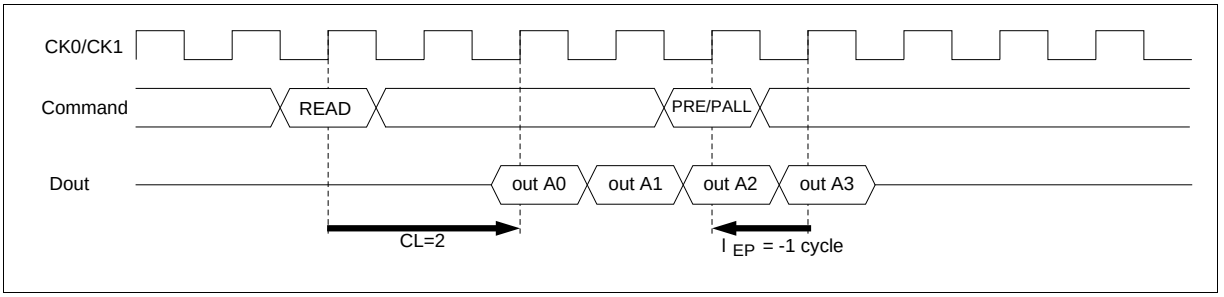
Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address).

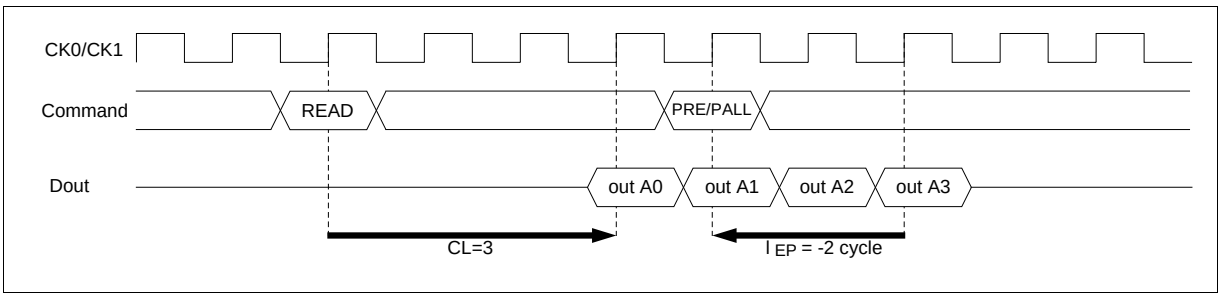
Read command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by I_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by I_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

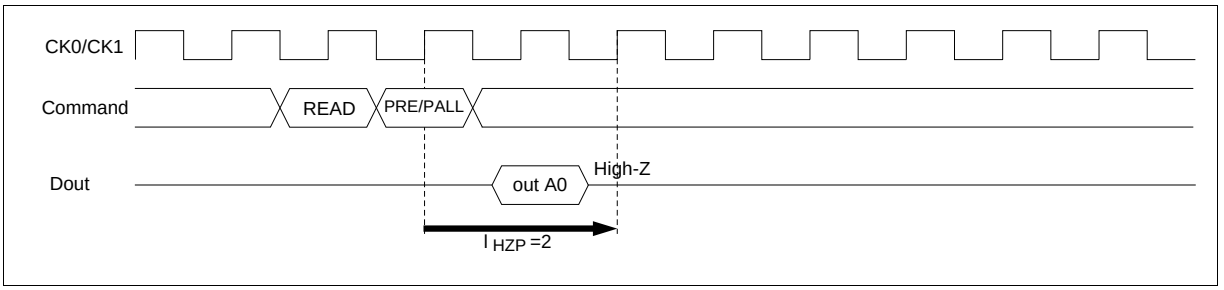


$\overline{\text{CAS}}$ Latency = 3, Burst Length = 4

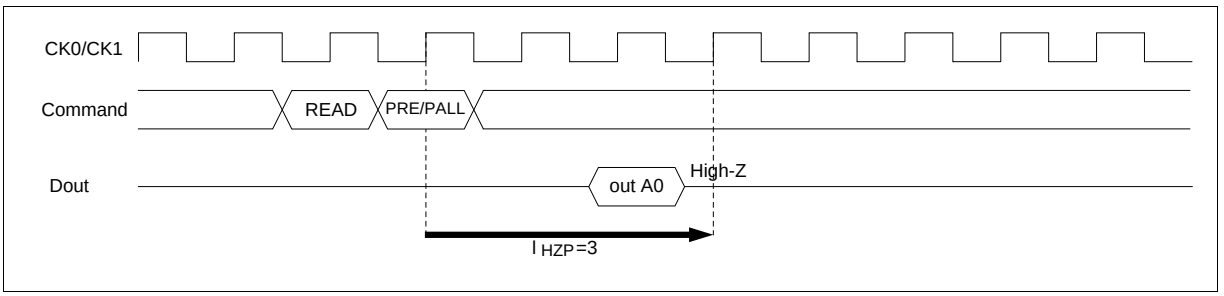


READ to PRECHARGE Command Interval (same bank): To stop output data

$\overline{\text{CAS}}$ Latency = 2, Burst Length = 1, 2, 4, 8



$\overline{\text{CAS}}$ Latency = 3, Burst Length = 1, 2, 4, 8

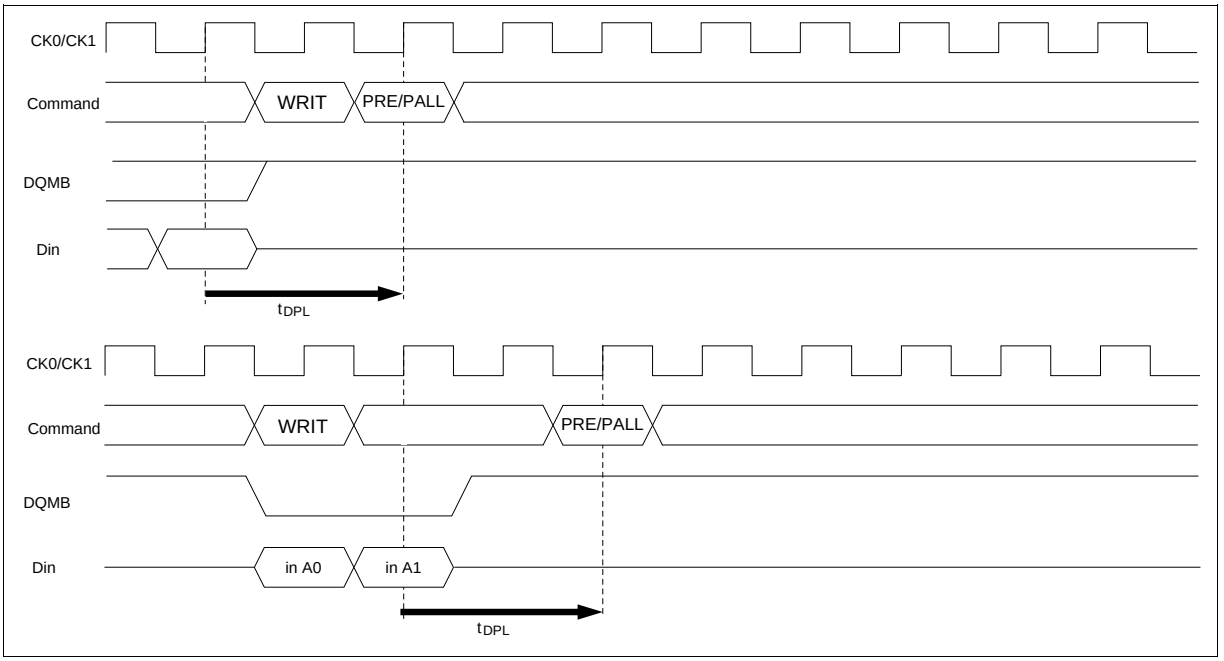


Write command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle.

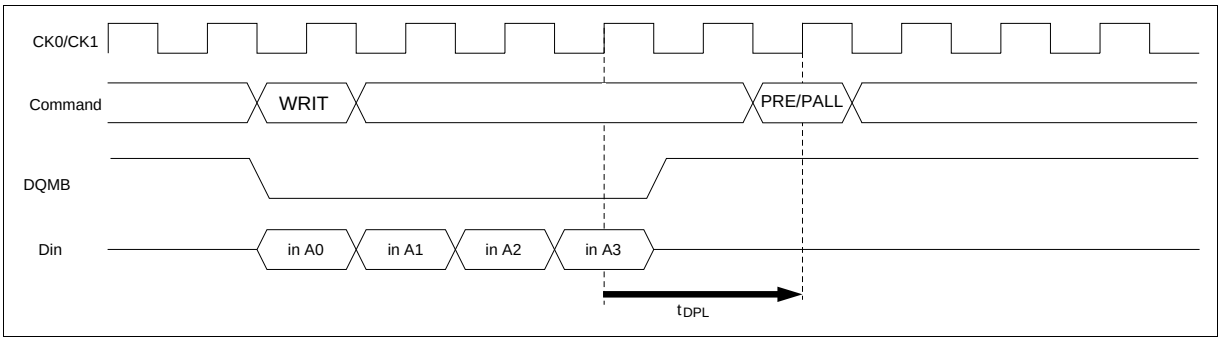
WRITE to PRECHARGE Command Interval (same bank): However, if the burst write operation is unfinished, the input data must be masked by means of DQMB for assurance of the cycle defined by t_{DPL}.

WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)



Burst Length = 4 (To write all data)

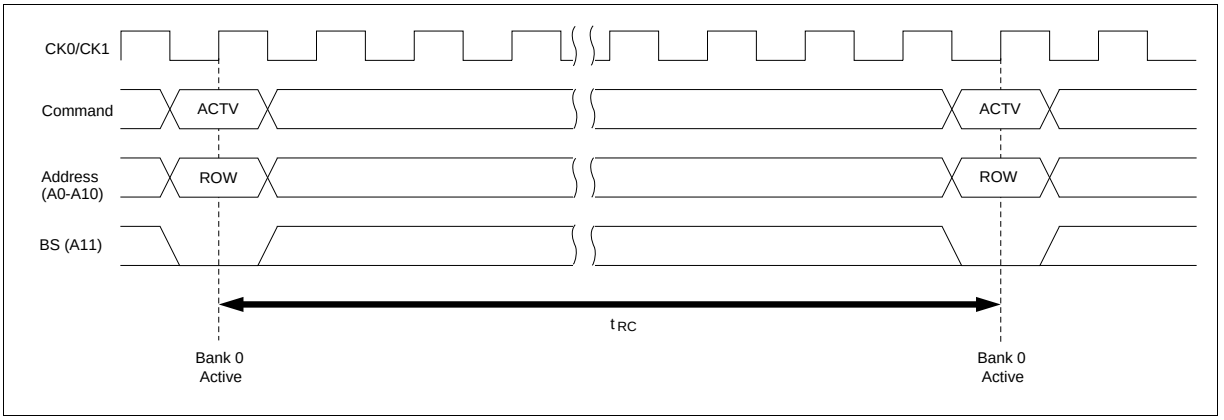


Bank active command interval:

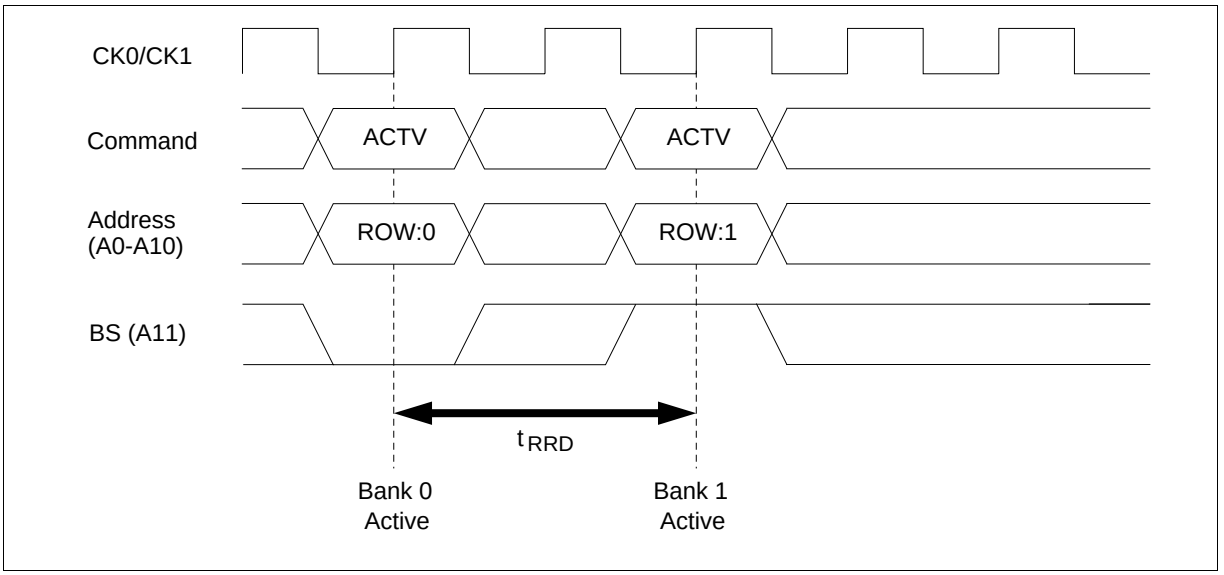
Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

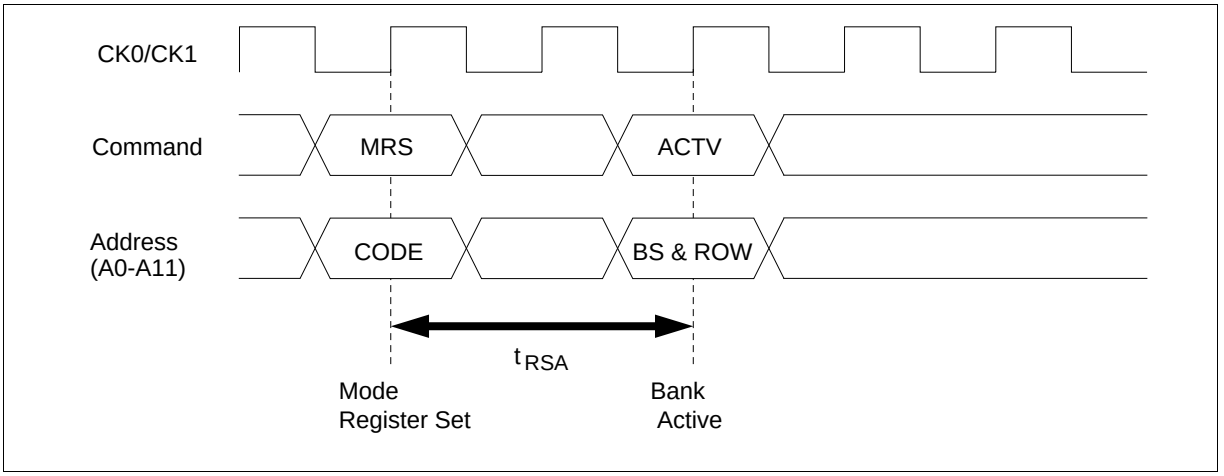
Bank active to bank active for same bank



Bank active to bank active for different bank



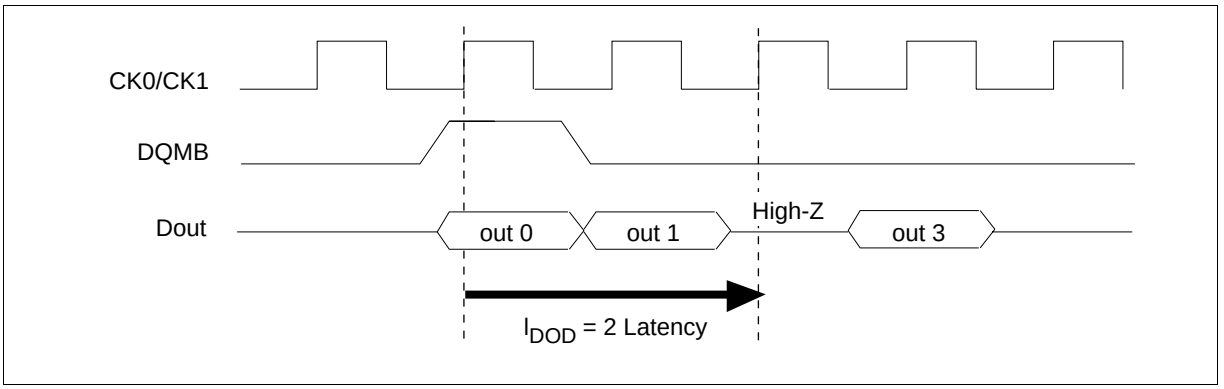
Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



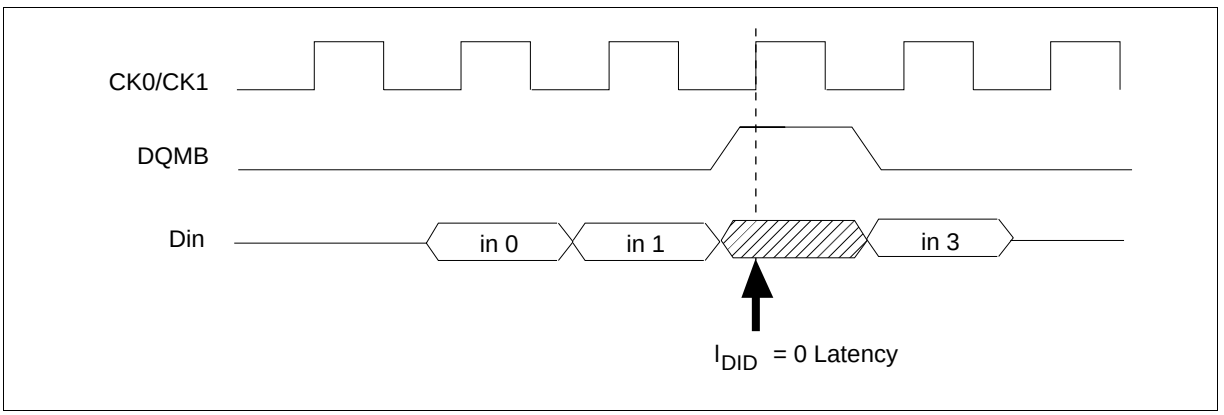
DQMB Control

The DQMB mask the lower and upper bytes of the DQ data, respectively. The timing of DQMB is different during reading and writing.

Reading: When data is read, the output buffer can be controlled by DQMB. By setting DQMB to Low, the output buffer becomes Low-Z, enabling data output. By setting DQMB to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQMB during reading is 2.



Writing: Input data can be masked by DQMB. By setting DQMB to Low, data can be written. In addition, when DQMB is set to High, the corresponding data is not written, and the previous data is held. The latency of DQMB during writing is 0.



Refresh

Auto-refresh: All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the interval counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4096 cycles/64 ms. (4096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh: After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. If you use distributed auto-refresh mode with 15.6 µs interval in normal read/write cycle, auto-refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode. If you use address refresh or burst auto-refresh mode in normal read/write cycle, 4096 cycles of distributed auto-refresh with 15.6 µs interval should be executed within 64 ms immediately after exiting from and before entering into self refresh mode.

Others

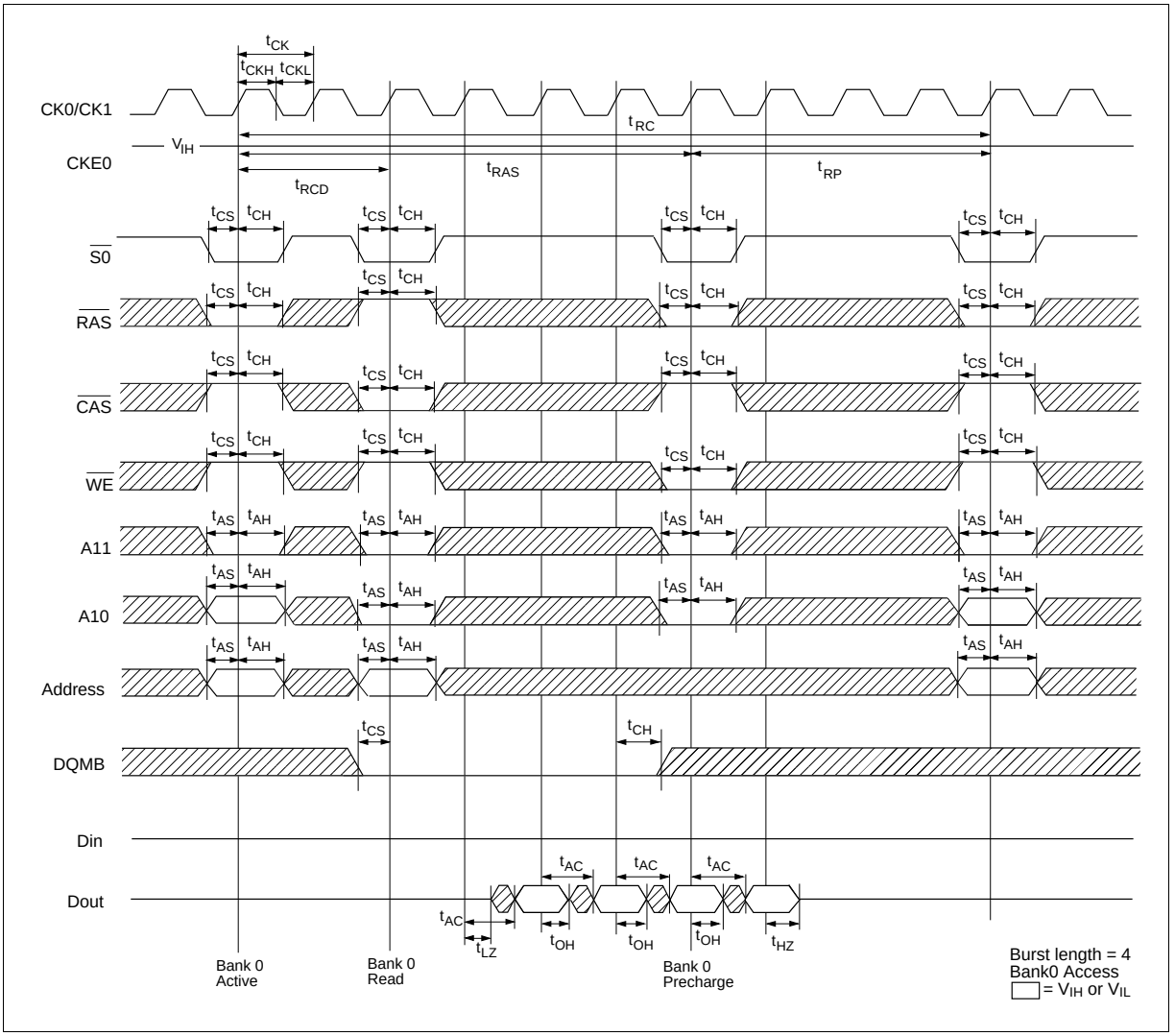
Power-down mode: The synchronous DRAM module enters power-down mode when CKE0 goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE0 is held Low. In addition, by setting CKE0 to High, the synchronous DRAM module exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

Clock suspend mode: By driving CKE0 to Low during a bank-active or read/write operation, the synchronous DRAM module enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE0 is driven High, the synchronous DRAM module terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE0 Truth Table".

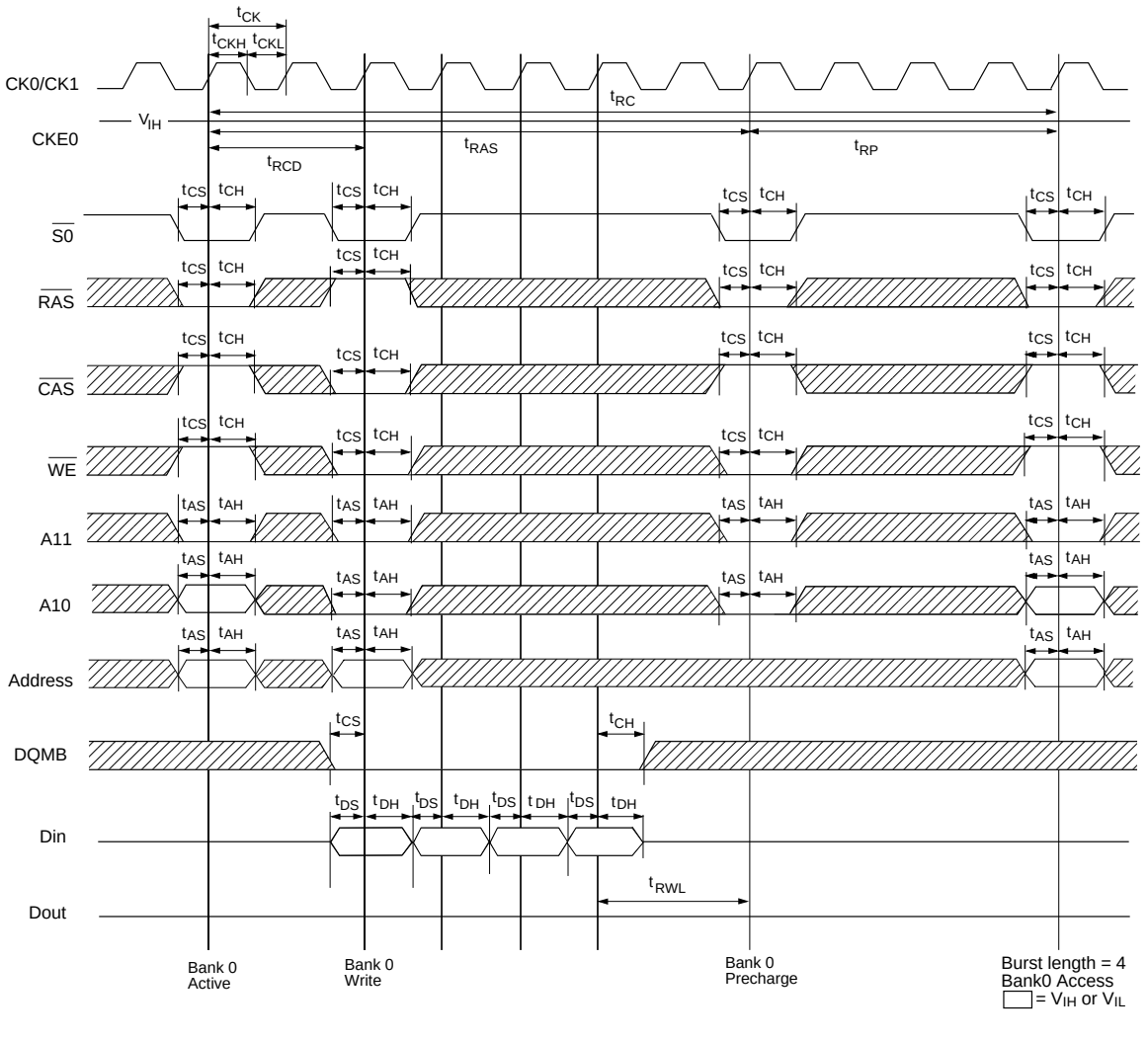
Power-up sequence: During power-up sequence, the DQMB and the CKE0 must be set to High. When 200 µs has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

Timing Waveforms

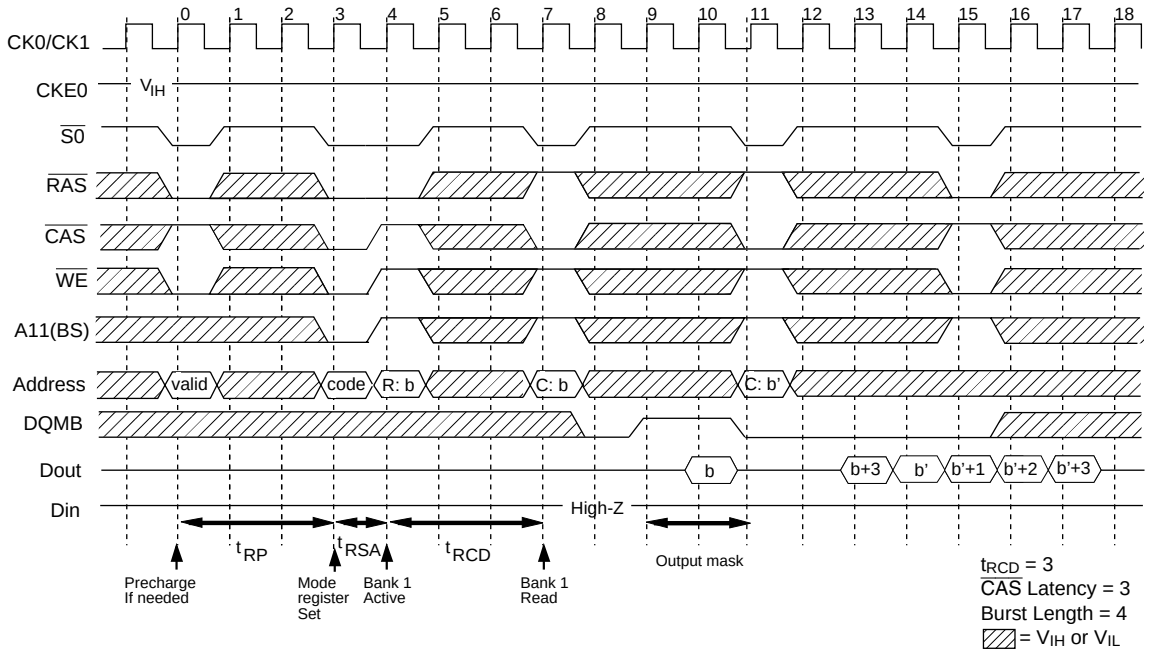
Read Cycle



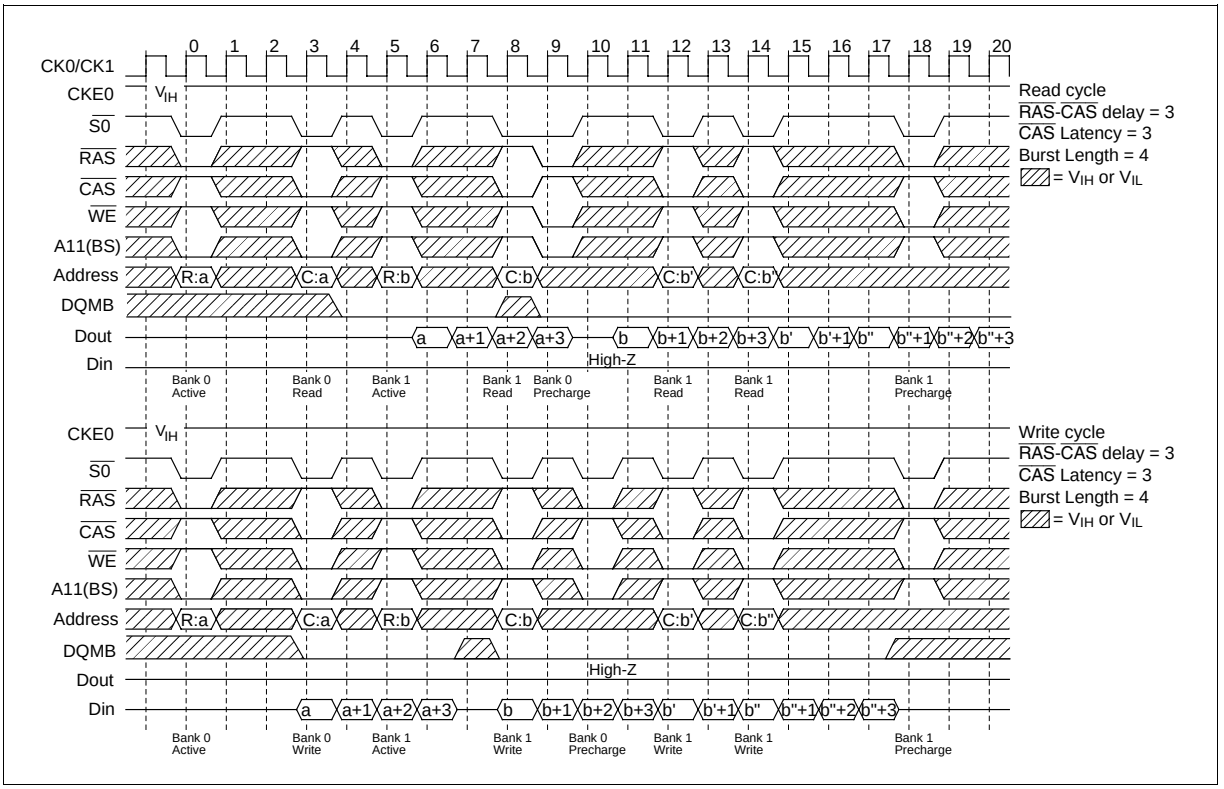
Write Cycle


tCK
tCKH tCKL
CK0/CK1
tRC
VIH
CKE0
tRAS
tRP
tRCD
tCS tCH
S0
RAS
CAS
WE
tAS tAH
A11
A10
Address
DQMB
tDS tDH
Din
Dout
tRWL
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
Burst length = 4
Bank0 Access
= VIH or VIL

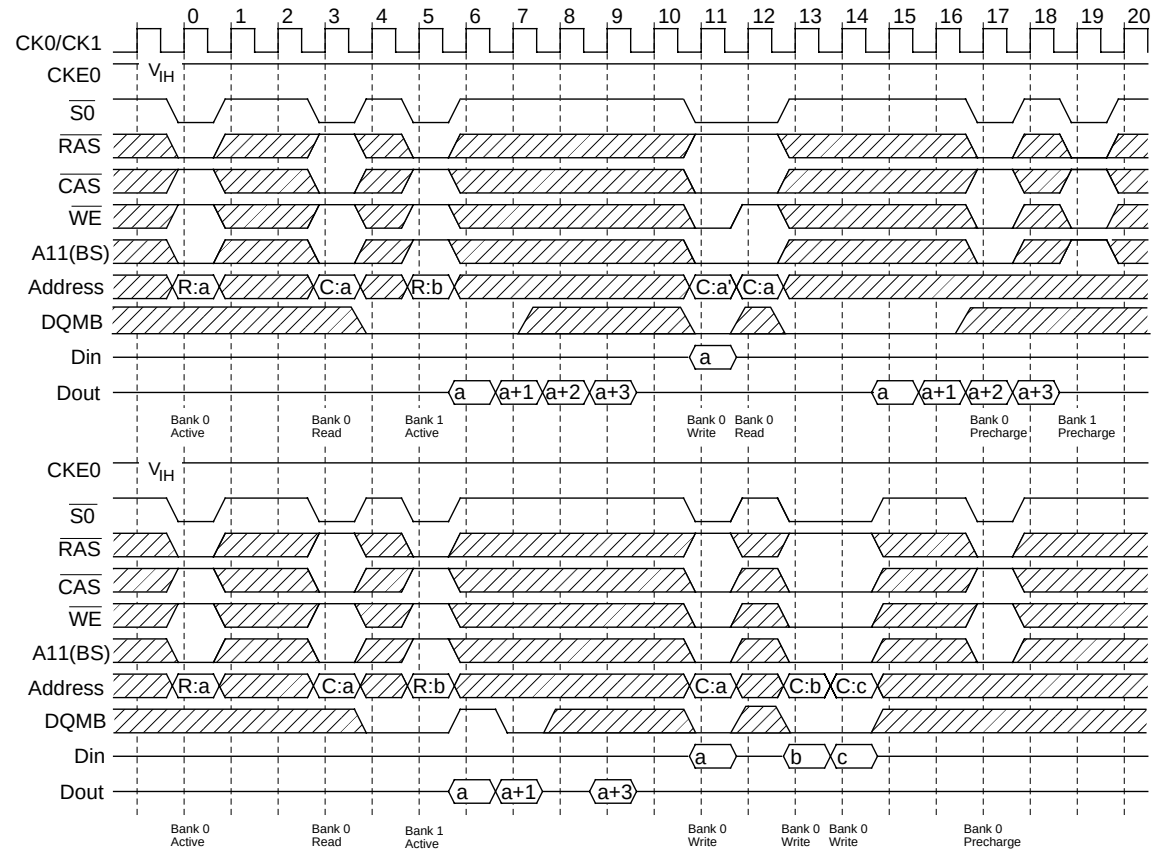
Mode Register Set Cycle



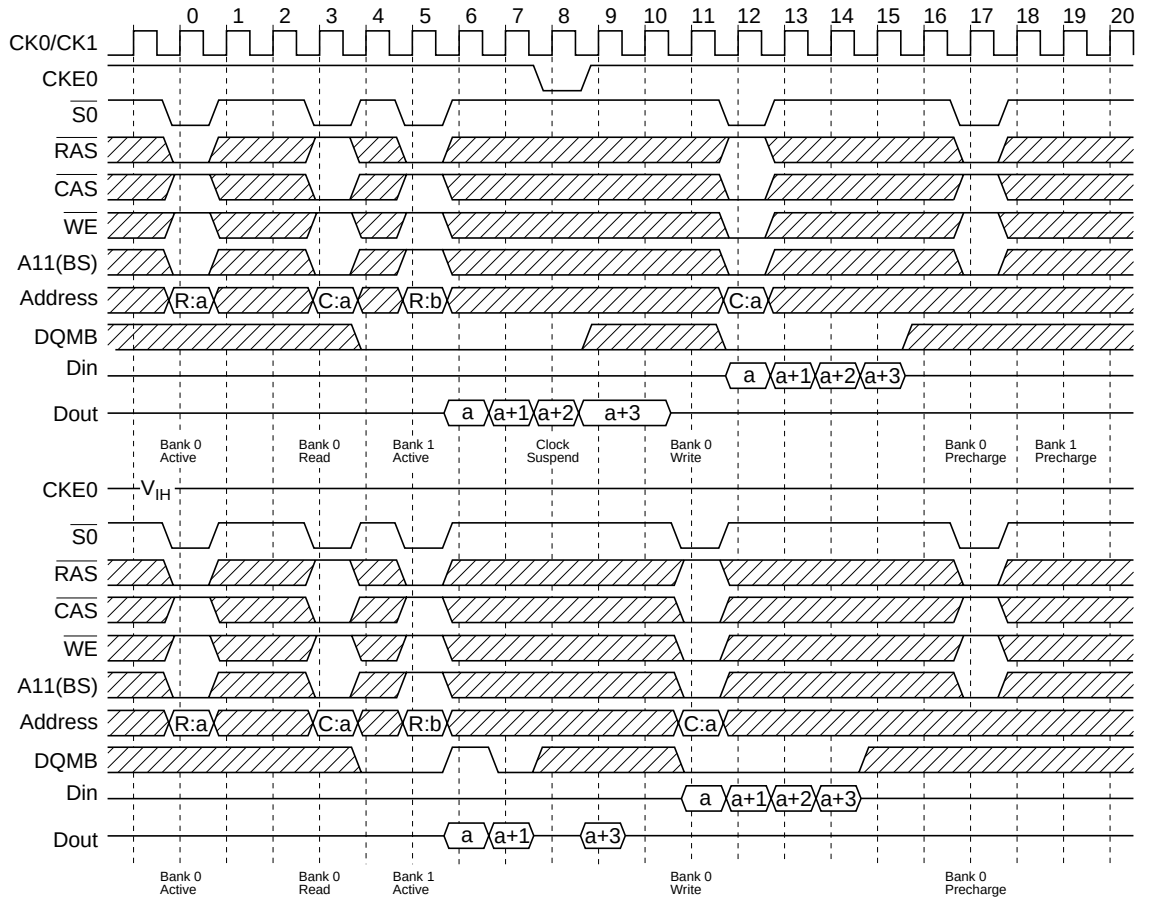
Read Cycle/Write Cycle



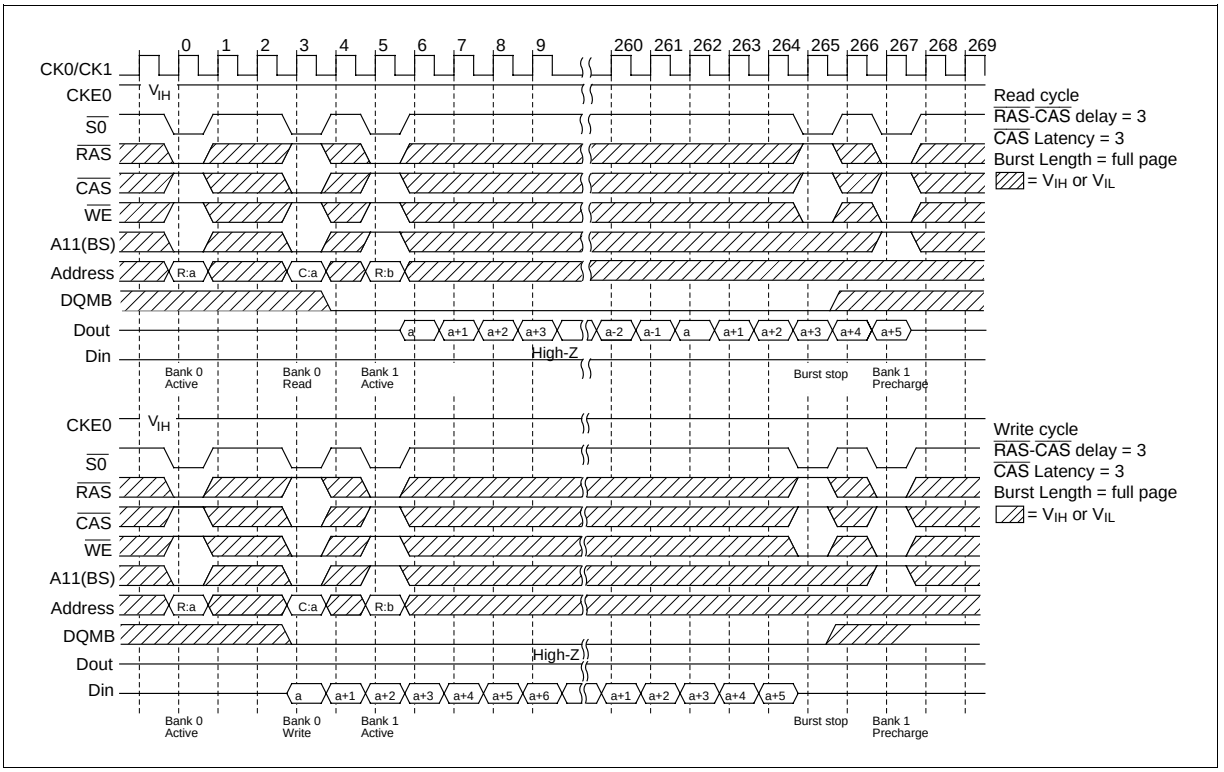
Read/Single Write Cycle



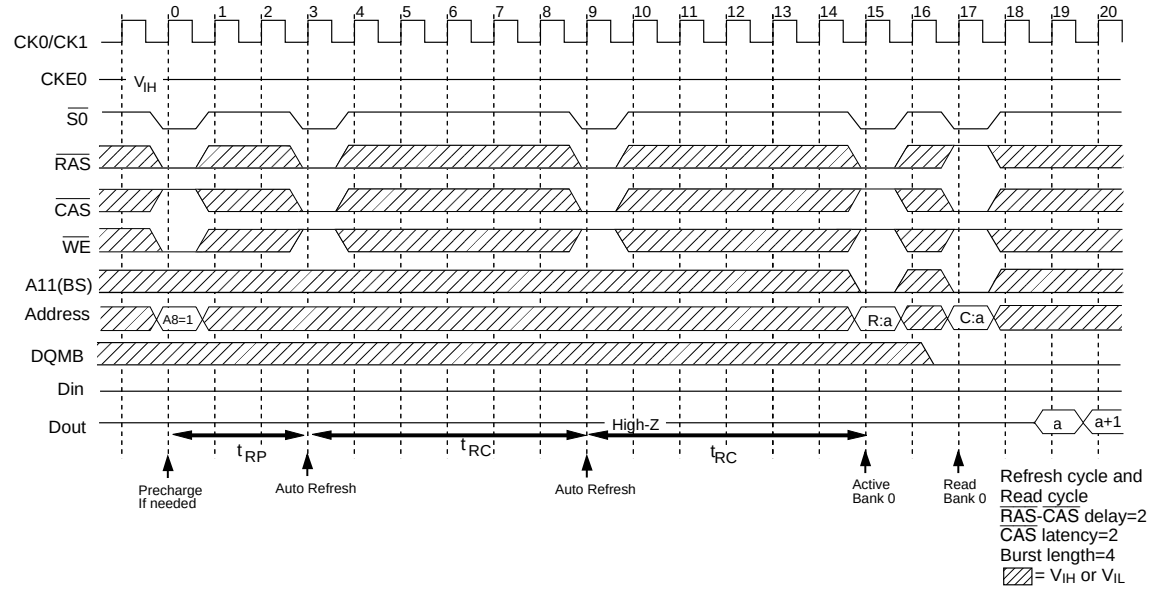
Read/Burst Write Cycle



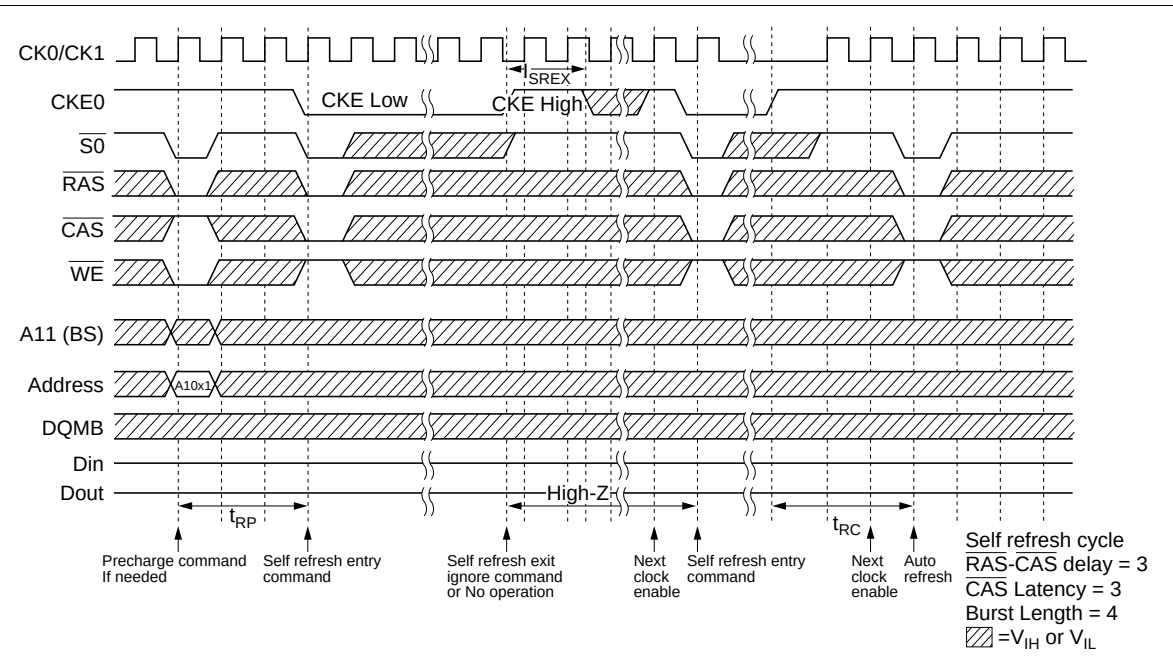
Full Page Read/Write Cycle



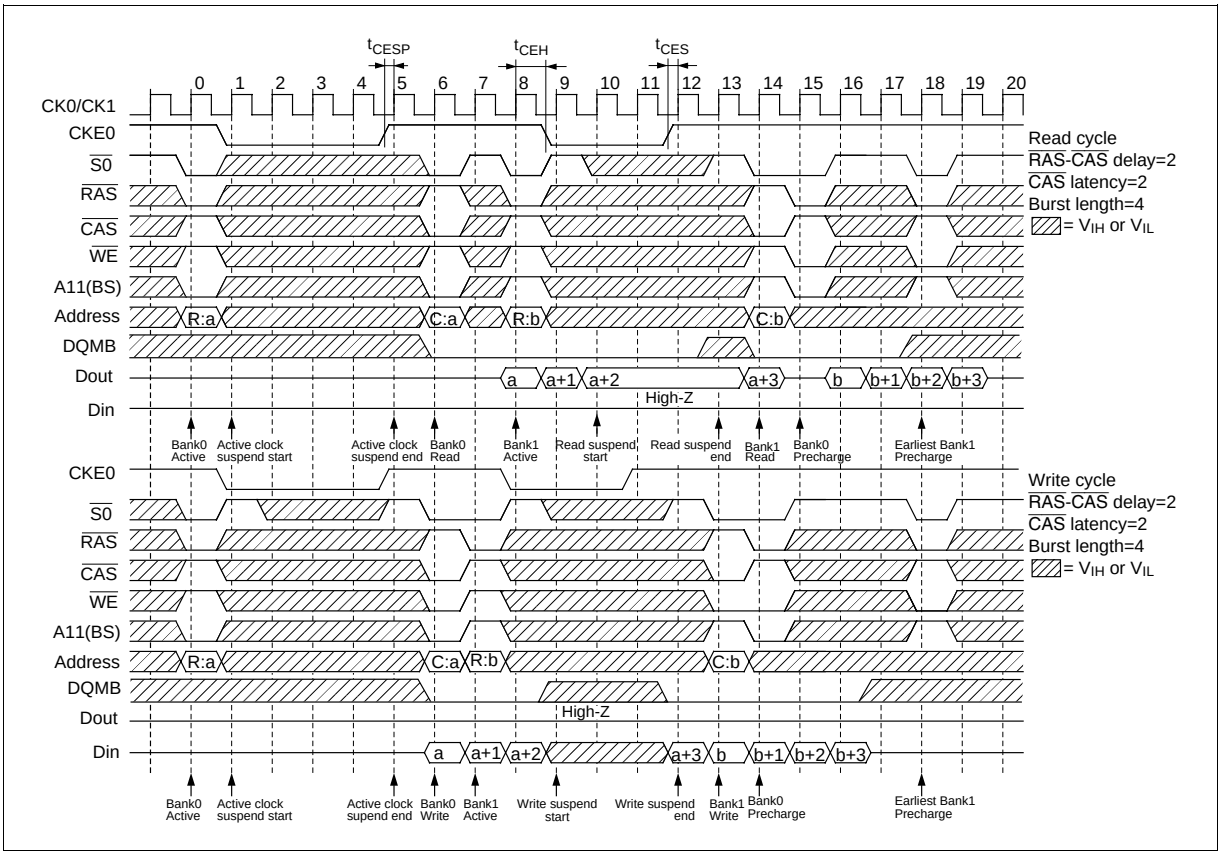
Auto Refresh Cycle



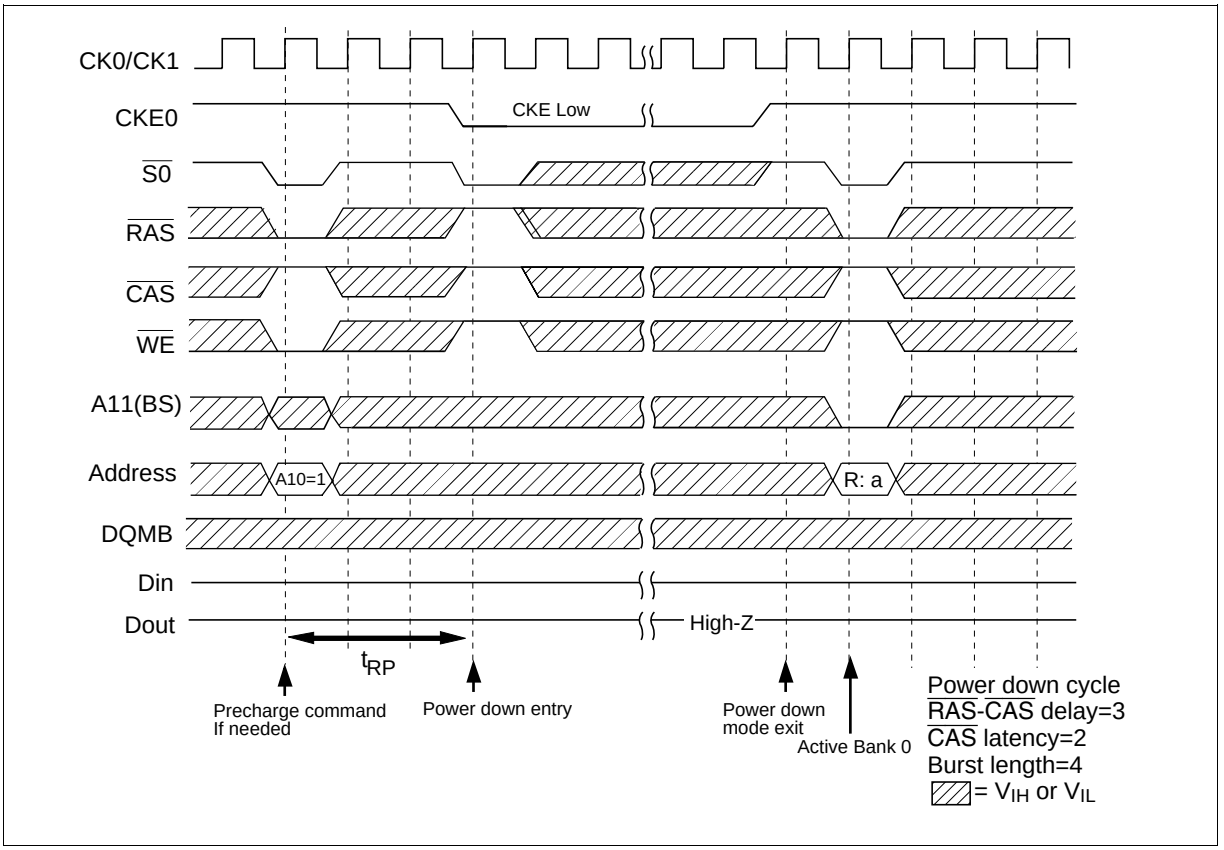
Self Refresh Cycle



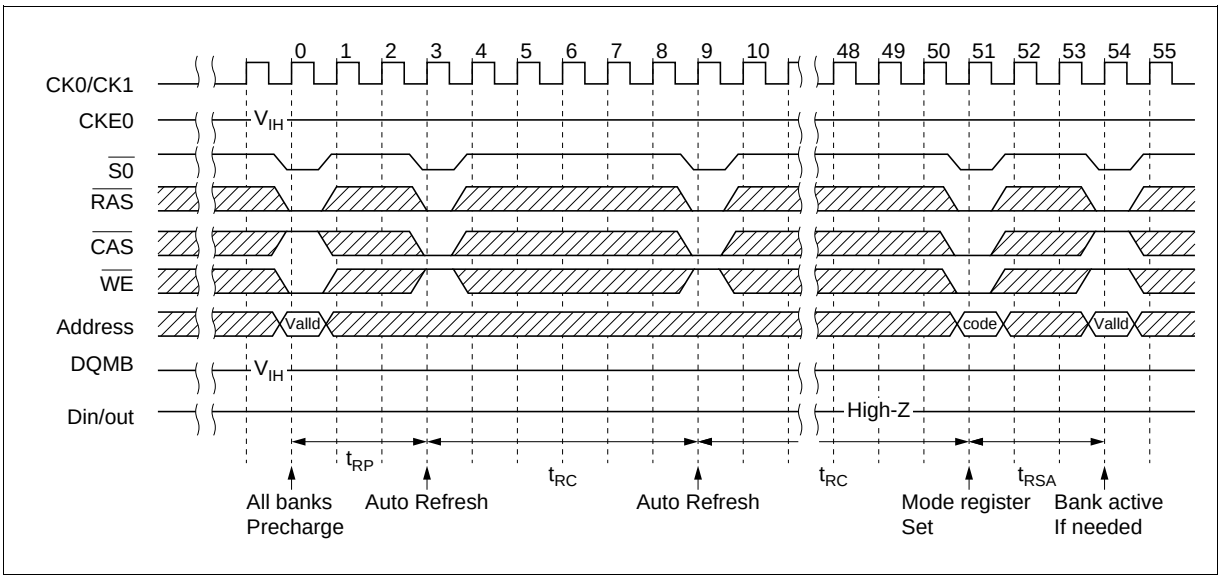
Clock Suspend Mode



Power Down Mode

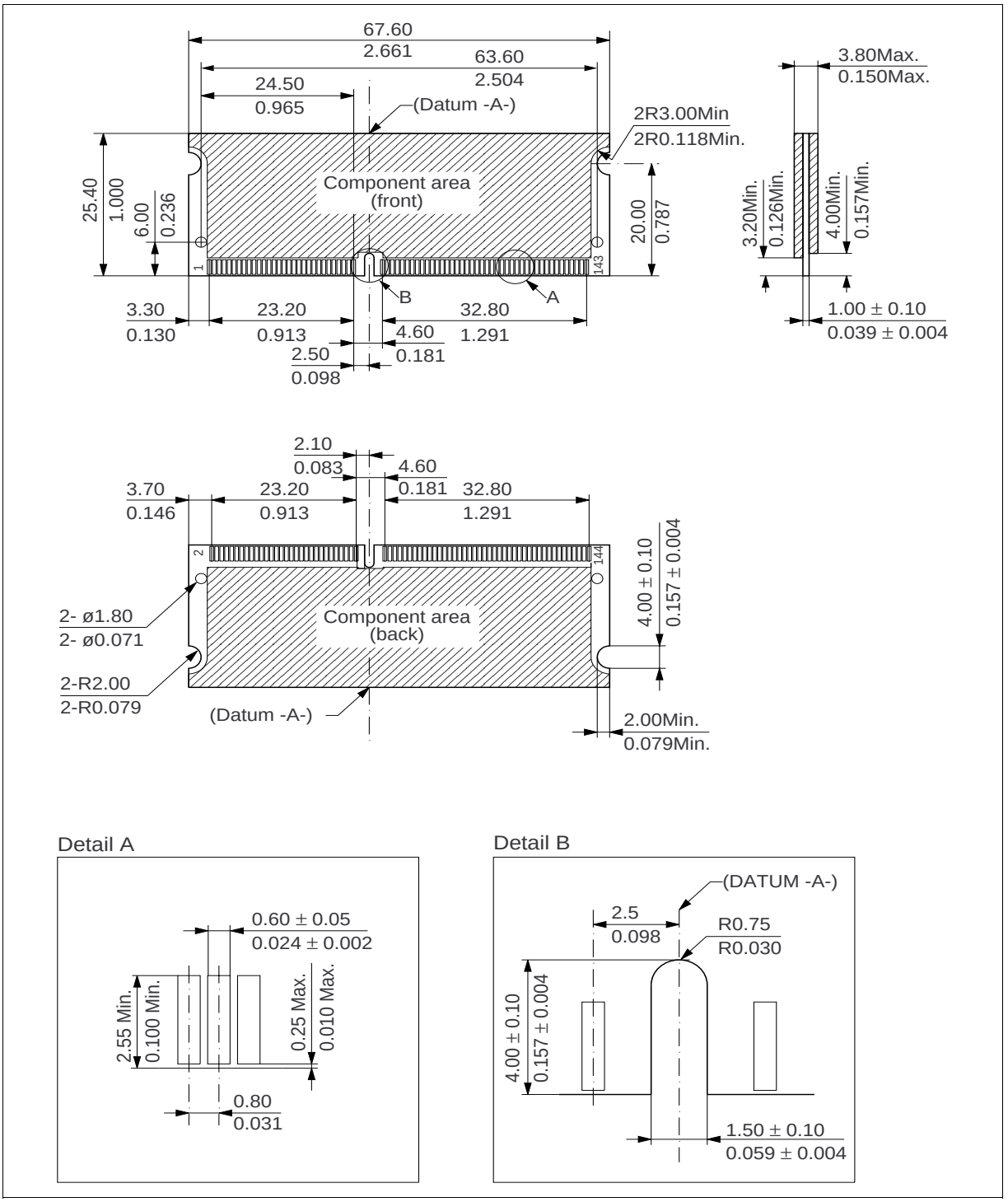


Power Up Sequence



Physical Outline

Unit: mm / inch



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 18, 1996	Initial issue	T. Sugano	K. Tsuneda
0.1	May. 20, 1997	(referred to HM5216805/HM5216405 rev.3.0) Correct errors Addition of HB526A264DB-10L Deletion of HB526A264DB-15 Change of Serial PD Matrix Absolute Maximum Ratings Topr: 0 to 65 ˚C to 0 to 70˚C Change of note1 DC Characteristics Addition of I_{CC6} (L-version) max: 2/2 mA AC Characteristics t_{AC} (CL = 2) max: 9.5/12 ns to 9/12 ns t_{AC} (CL = 3) max: 8/9.5 ns to 7.5/9 ns t_{HZ} min: 2/2 ns to —/— ns Change of symbol: t_{RWL} to t_{DPL} Change of description for Self-refresh		