HB56A841BR Series, HB56A441BR Series

8,388,608-word × 40-bit High Density Dynamic RAM Module
4,194,304-word × 40-bit High Density Dynamic RAM Module

HITACHI

ADE-203-731A (Z)
Rev.1.0
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Description

The HB56A841BR is a 8M × 40 dynamic RAM module, mounted 20 pieces of 16-Mbit DRAM (HM5117400) sealed in SOJ package. The HB56A441BR is a 4M × 40 dynamic RAM module, mounted 10 pieces of 16-Mbit DRAM (HM5117400) sealed in SOJ package. An outline of the HB56A841BR, HB56A441BR is 72-pin single in-line package. Therefore, the HB56A841BR, HB56A441BR make high density mounting possible without surface mount technology. The HB56A841BR, HB56A441BR provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 72-pin single in-line package
  - — Outline: 107.95 mm (Length) × 25.40 mm (Height) × 9.14/5.28 mm (Thickness)
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 50/60/70ns (max)
- Low power dissipation
  - — Active mode: 5.52/4.99/4.46 W (max) (HB56A841BR Series)
    5.25/4.73/4.20 W (max) (HB56A441BR Series)
  - — Standby mode (TTL): 210 mW (max) (HB56A841BR Series)
    (TTL): 105 mW (max) (HB56A441BR Series)
    (CMOS): 105 mW (max) (HB56A841BR Series)
    (CMOS): 52.5 mW (max) (HB56A441BR Series)
- Fast page mode capability
- Refresh period
  - — 2048 refresh cycles: 32 ms

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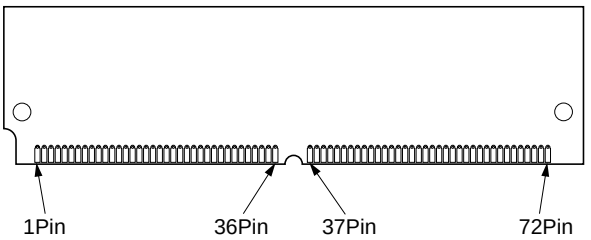
- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56A841BR-5	50 ns	72-pin SIP socket type	Gold
HB56A841BR-6	60 ns		
HB56A841BR-7	70 ns		
HB56A441BR-5	50 ns		
HB56A441BR-6	60 ns		
HB56A441BR-7	70 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	$\overline{OE}$	37	DQ19	55	DQ28
2	DQ0	20	DQ8	38	DQ20	56	DQ29
3	DQ1	21	DQ9	39	V_{SS}	57	DQ30
4	DQ2	22	DQ10	40	$\overline{CAS0}$	58	DQ31
5	DQ3	23	DQ11	41	A10	59	V_{CC}
6	DQ4	24	DQ12	42	NC	60	DQ32
7	DQ5	25	DQ13	43	$\overline{CAS1}$ (NC)*[1]	61	DQ33
8	DQ6	26	DQ14	44	$\overline{RAS0}$	62	DQ34
9	DQ7	27	DQ15	45	$\overline{RAS1}$ (NC)*[2]	63	DQ35
10	V_{CC}	28	A7	46	DQ21	64	DQ36
11	PD4	29	DQ16	47	$\overline{WE}$	65	DQ37
12	A0	30	V_{CC}	48	$\times 40$ (V_{SS})	66	DQ38
13	A1	31	A8	49	DQ22	67	PD0
14	A2	32	A9	50	DQ23	68	PD1
15	A3	33	NC	51	DQ24	69	PD2
16	A4	34	NC	52	DQ25	70	PD3
17	A5	35	DQ17	53	DQ26	71	DQ39
18	A6	36	DQ18	54	DQ27	72	V_{SS}

Notes: 1. $\overline{CAS1}$: HB56A841BR, NC: HB56A441BR
2. $\overline{RAS1}$: HB56A841BR, NC: HB56A441BR

Pin Description

Pin name	Function
A0 to A10	Address inputs: — Row address: A0 to A10 — Column address: A0 to A10 — Refresh address: A0 to A10
DQ0 to DQ39	Data-in/Data-out
$\overline{CAS0}$, $\overline{CAS1}$	Column address strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD0 to PD4	Presence detect pin
NC	No connection

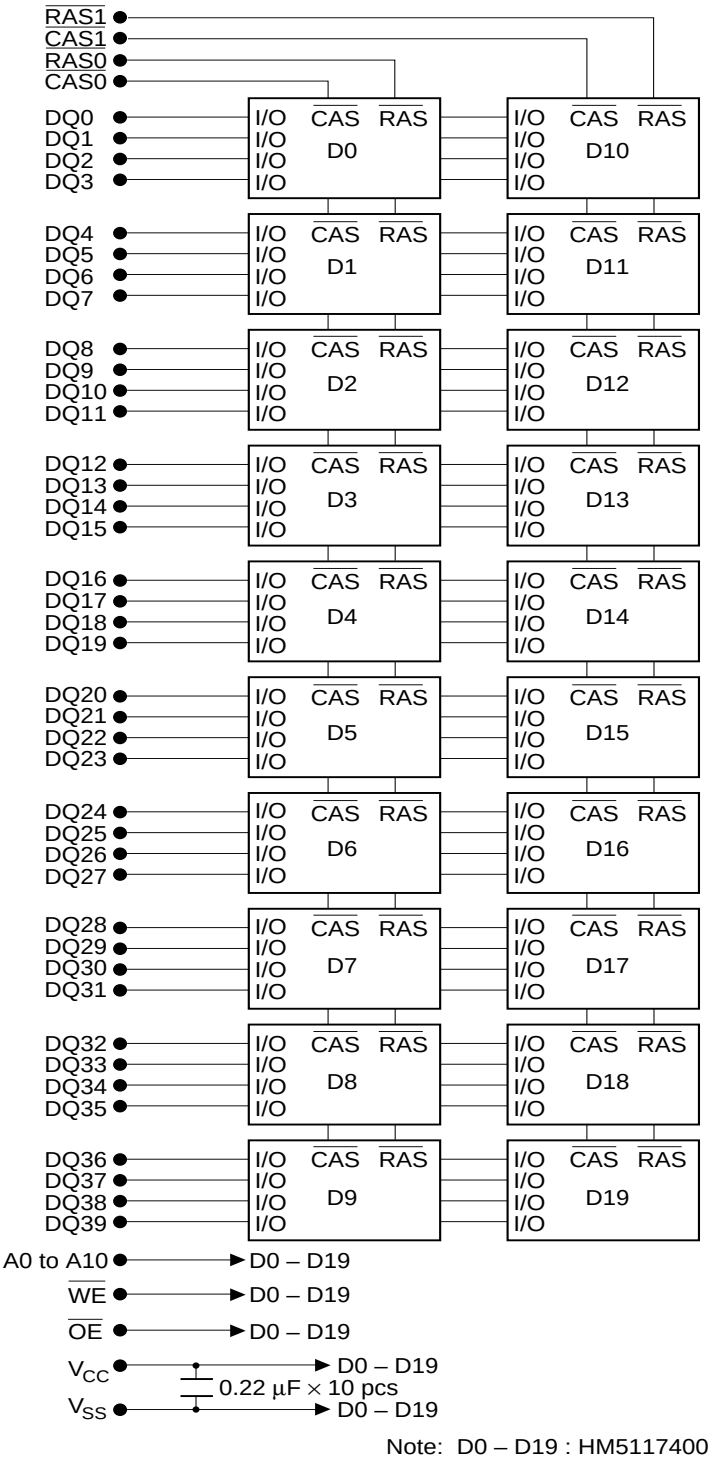
Presence Detect Pin Arrangement (HB56A841BR)

		Function		
Pin No.	Pin name	50 ns	60 ns	70 ns
67	PD0	NC	NC	NC
68	PD1	V_{SS}	V_{SS}	V_{SS}
69	PD2	V_{SS}	NC	V_{SS}
70	PD3	V_{SS}	NC	NC
11	PD4	V_{SS}	V_{SS}	V_{SS}

Presence Detect Pin Arrangement (HB56A441BR)

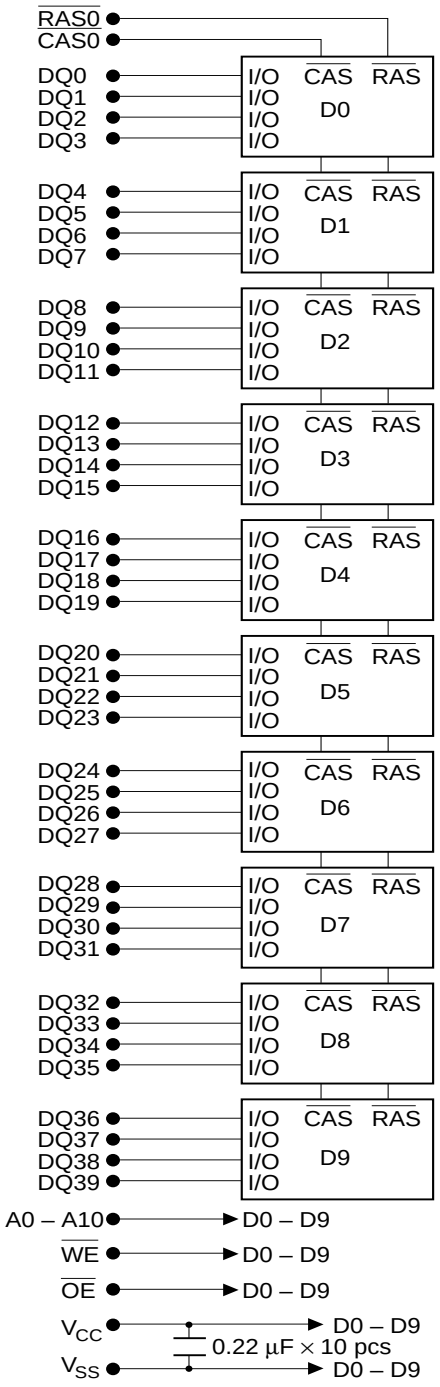
		Function		
Pin No.	Pin name	50 ns	60 ns	70 ns
67	PD0	V_{SS}	V_{SS}	V_{SS}
68	PD1	NC	NC	NC
69	PD2	V_{SS}	NC	V_{SS}
70	PD3	V_{SS}	NC	NC
11	PD4	V_{SS}	V_{SS}	V_{SS}

Block Diagram (HB56A841BR)



Note: D0 – D19 : HM5117400

Block Diagram (HB56A441BR)



Note: D0 – D9 : HM5117400

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	10	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56A841BR)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	1050	—	950	—	850	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	40	—	40	—	40	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Dout = High-Z	
		—	20	—	20	—	20	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1050	—	950	—	850	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	100	—	100	—	100	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1050	—	950	—	850	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	950	—	850	—	750	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56A441BR)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	1000	—	900	—	800	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	20	—	20	—	20	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Dout = High-Z	
		—	10	—	10	—	10	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1000	—	900	—	800	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	50	—	50	—	50	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1000	—	900	—	800	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	900	—	800	—	700	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56A841BR)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	140	pF	1
Input capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	160	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	90	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	25	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56A441BR)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	90	pF	1
Input capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	90	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	90	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70˚C, V_{CC} = 5 V ±5%, V_{SS} = 0 V) *[1], *[2], *[18], *[19]

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	90	—	110	—	130	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10000	15	10000	18	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	

Read Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	9, 20
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5

Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	7	—	10	—	15	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	15	—	18	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	—	15	—	18	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	7	—	10	—	15	—	ns	15

Read-Modify-Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	131	—	155	—	181	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	73	—	85	—	98	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	36	—	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	48	—	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	7	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	7	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

Fast Page Mode Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	35	—	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	30	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	—	35	—	40	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode read-modify-write cycle time	t_{PRWC}	76	—	85	—	96	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	53	—	60	—	68	—	ns	14

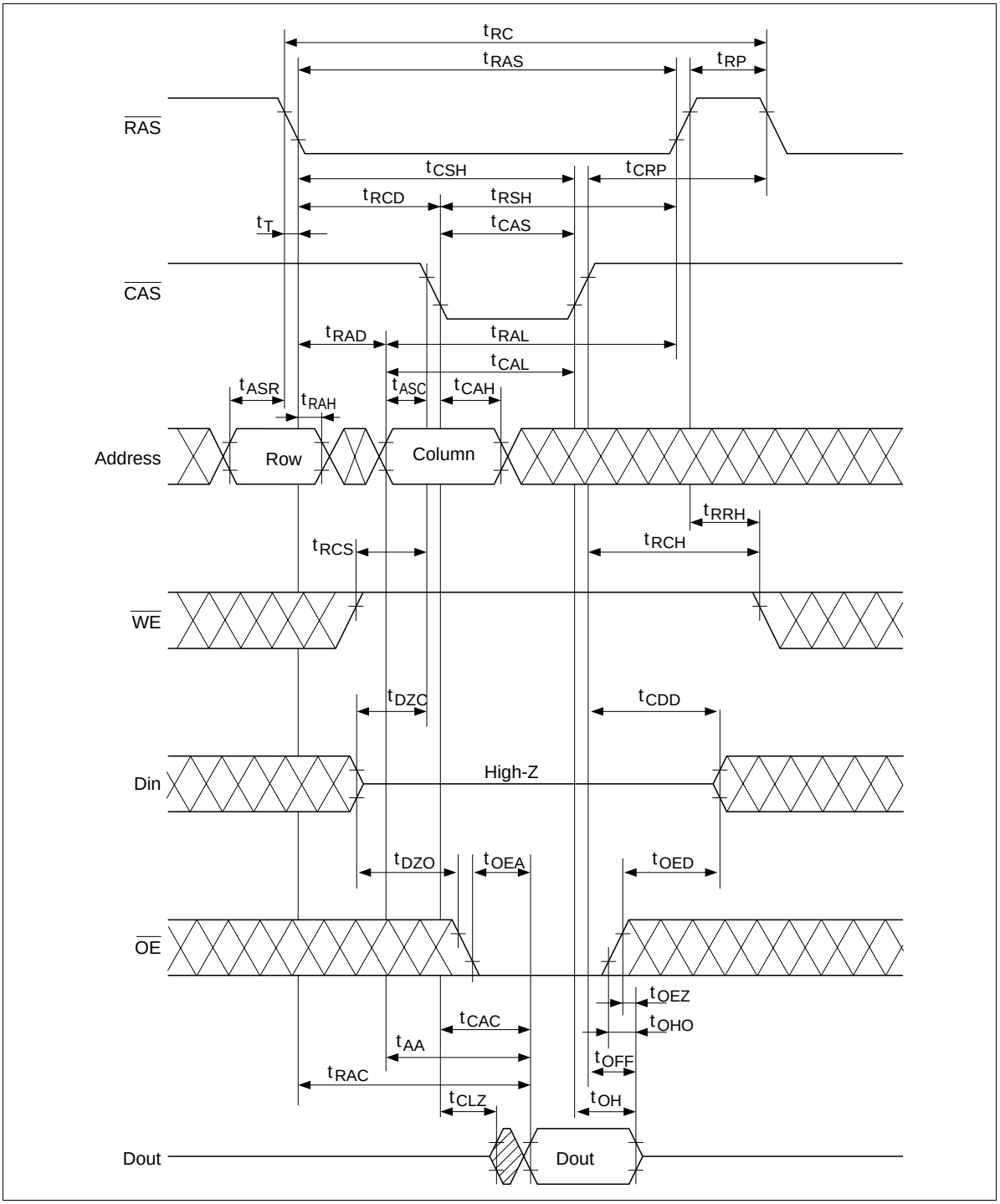
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) is define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} or t_{CPA}.
18. In delayed write or read-modify-write cycle, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min / V_{IL} max level.
21. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

    ///////: Invalid Dout

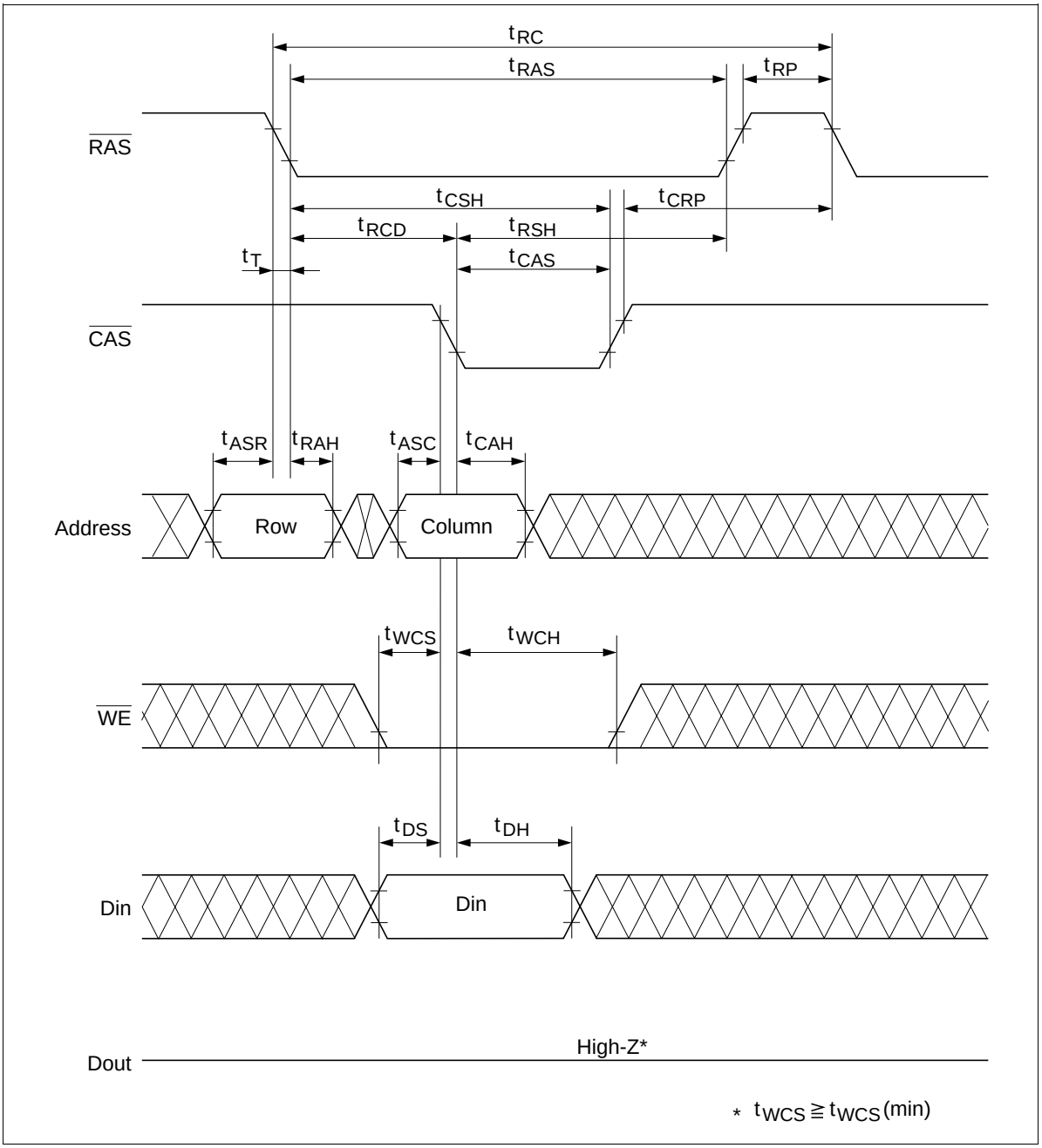
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[21]

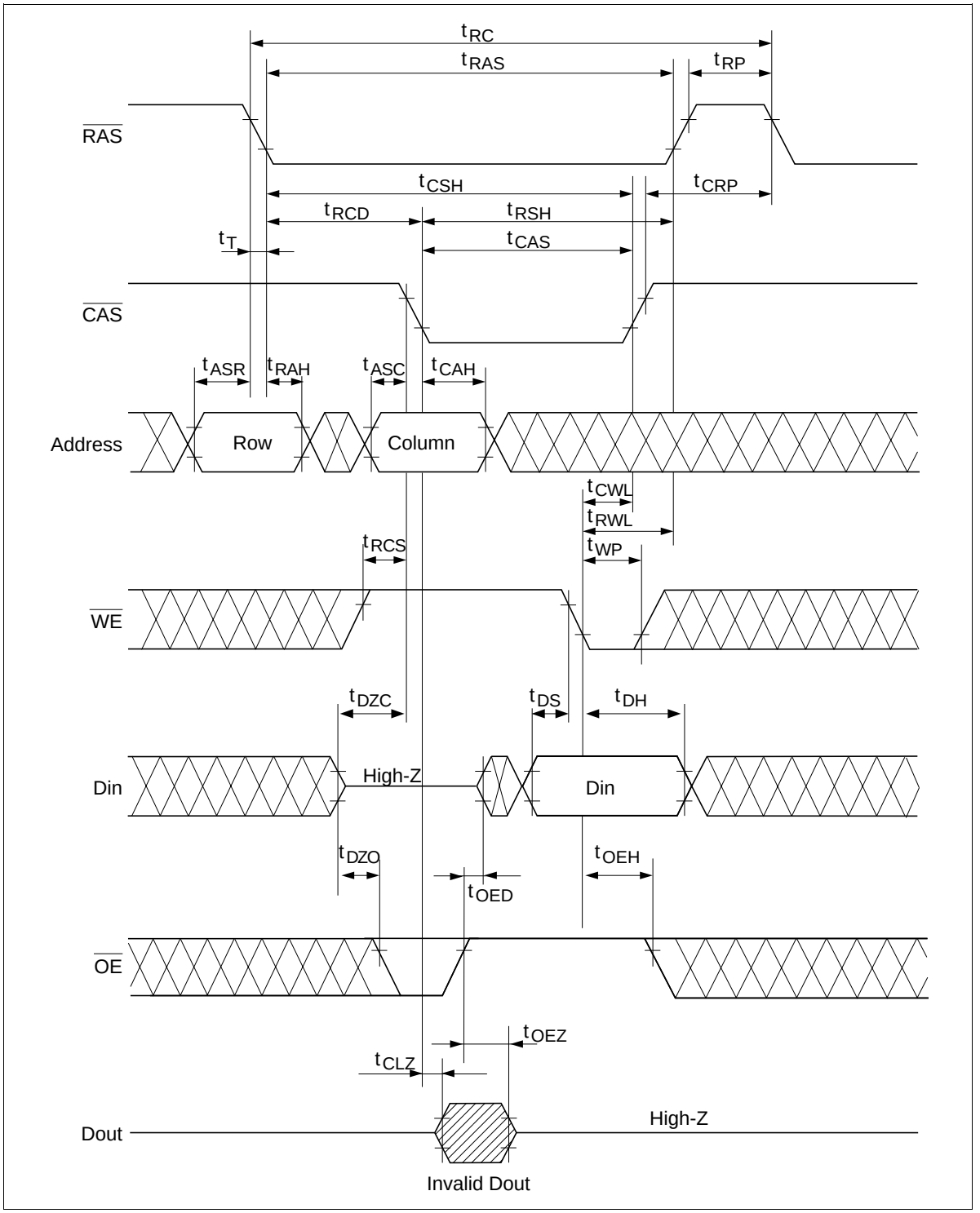
Read Cycle



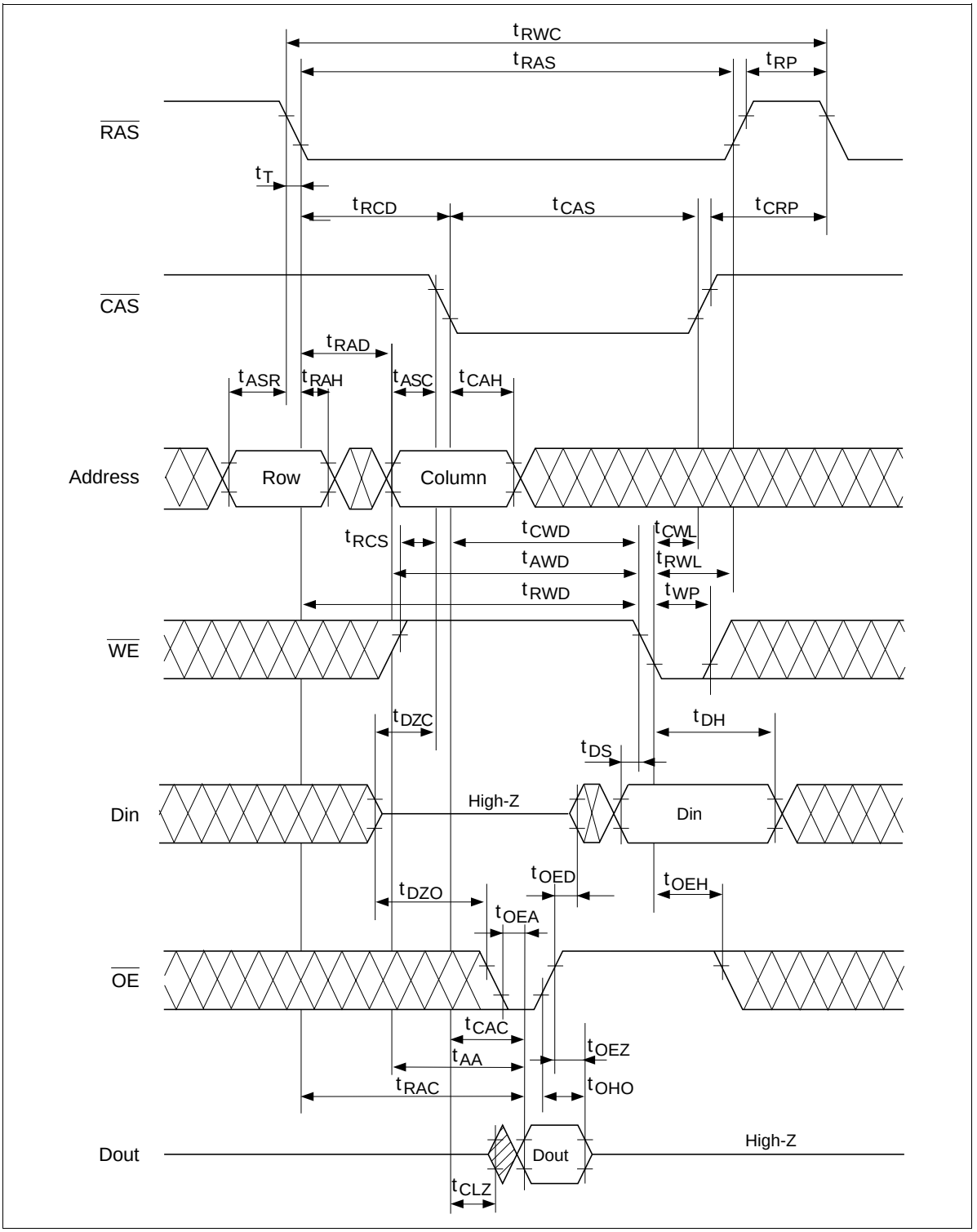
Early Write Cycle



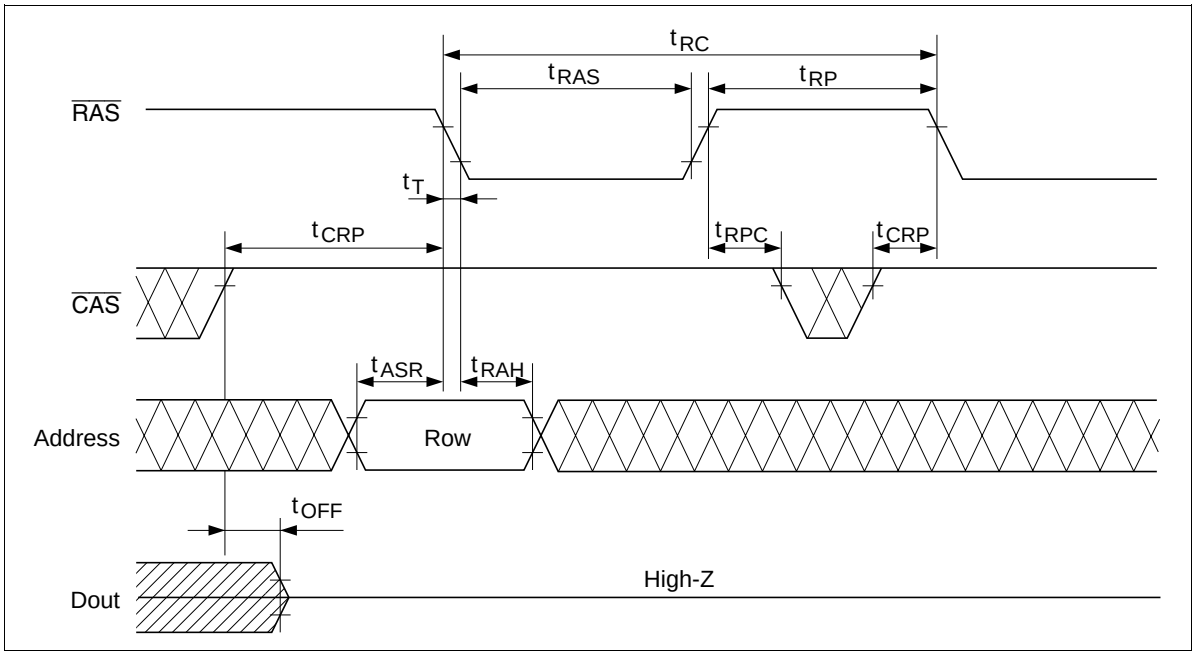
Delayed Write Cycle*[18]



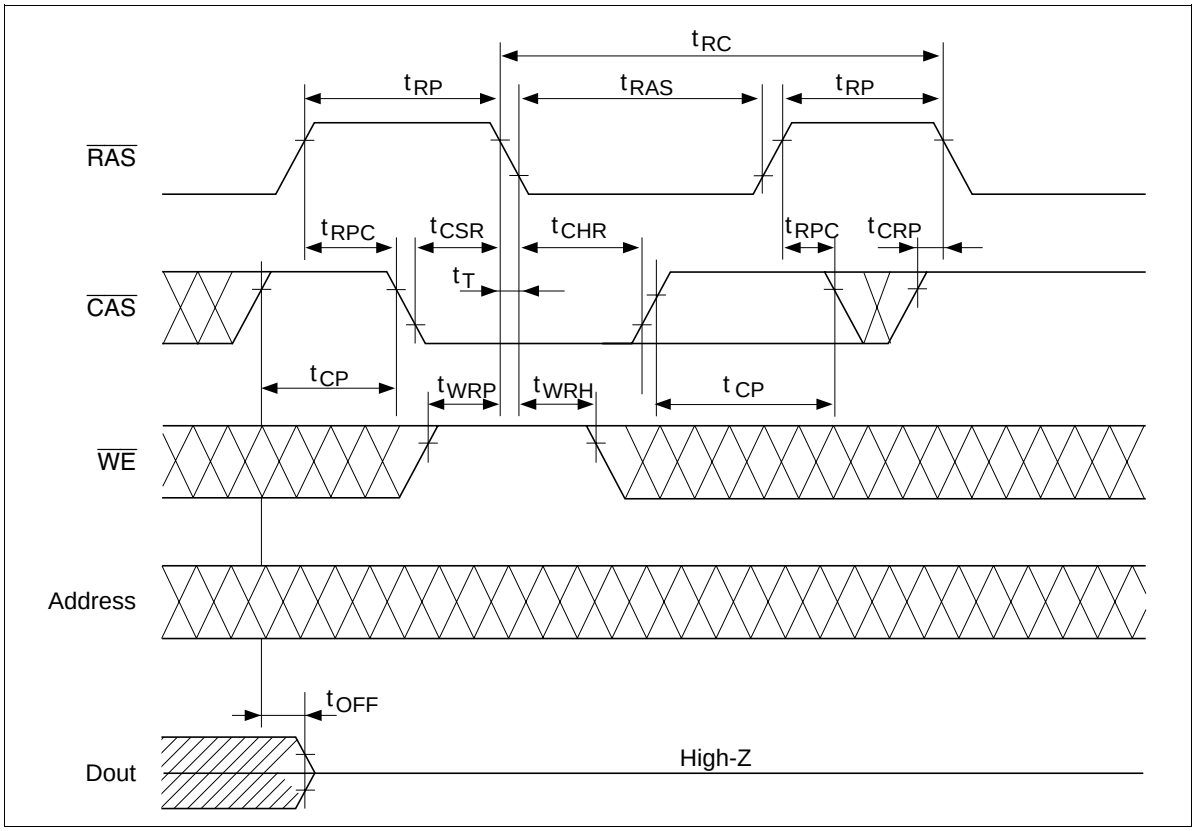
Read-Modify-Write Cycle*[18]



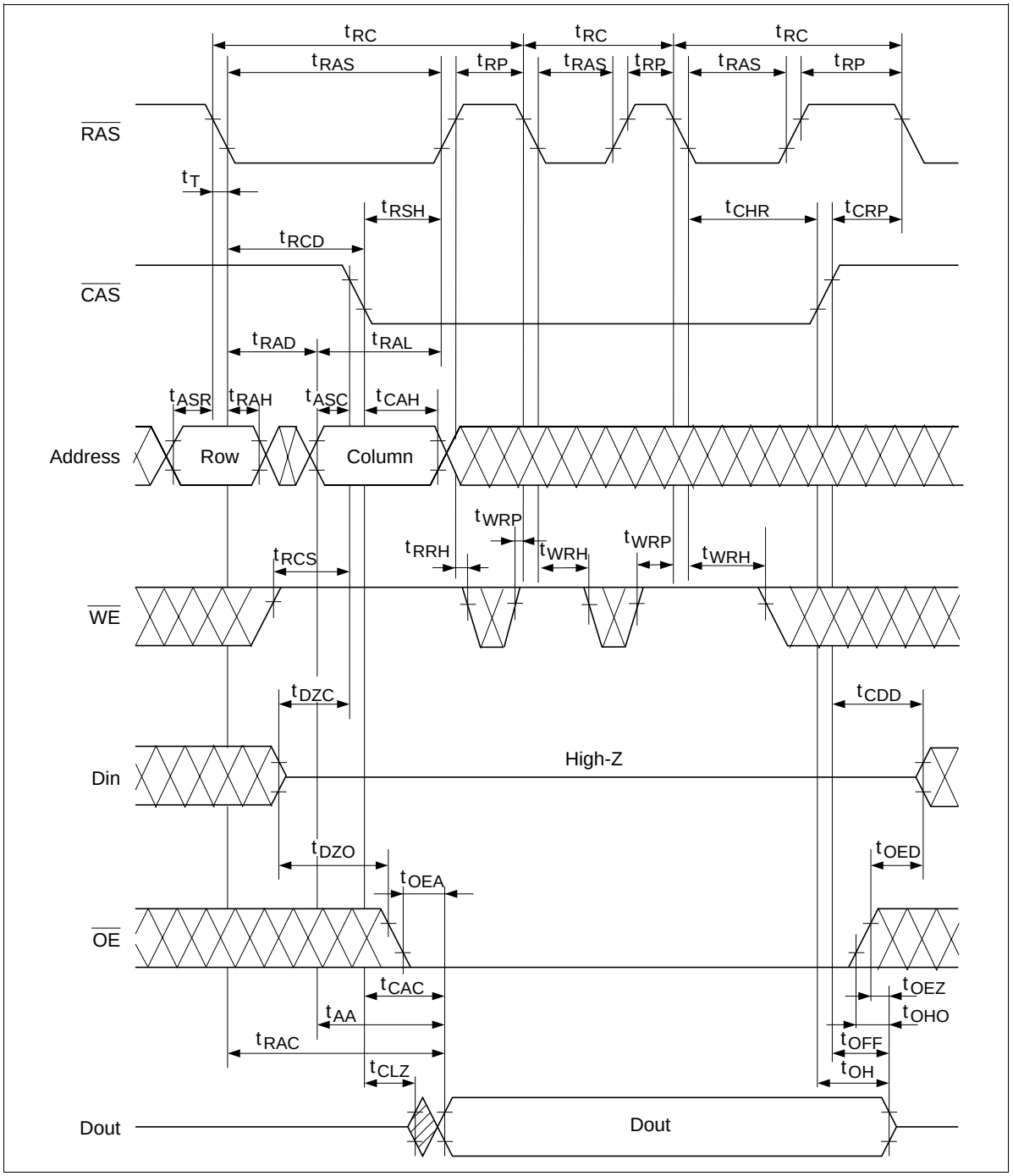
$\overline{\text{RAS}}$-Only Refresh Cycle



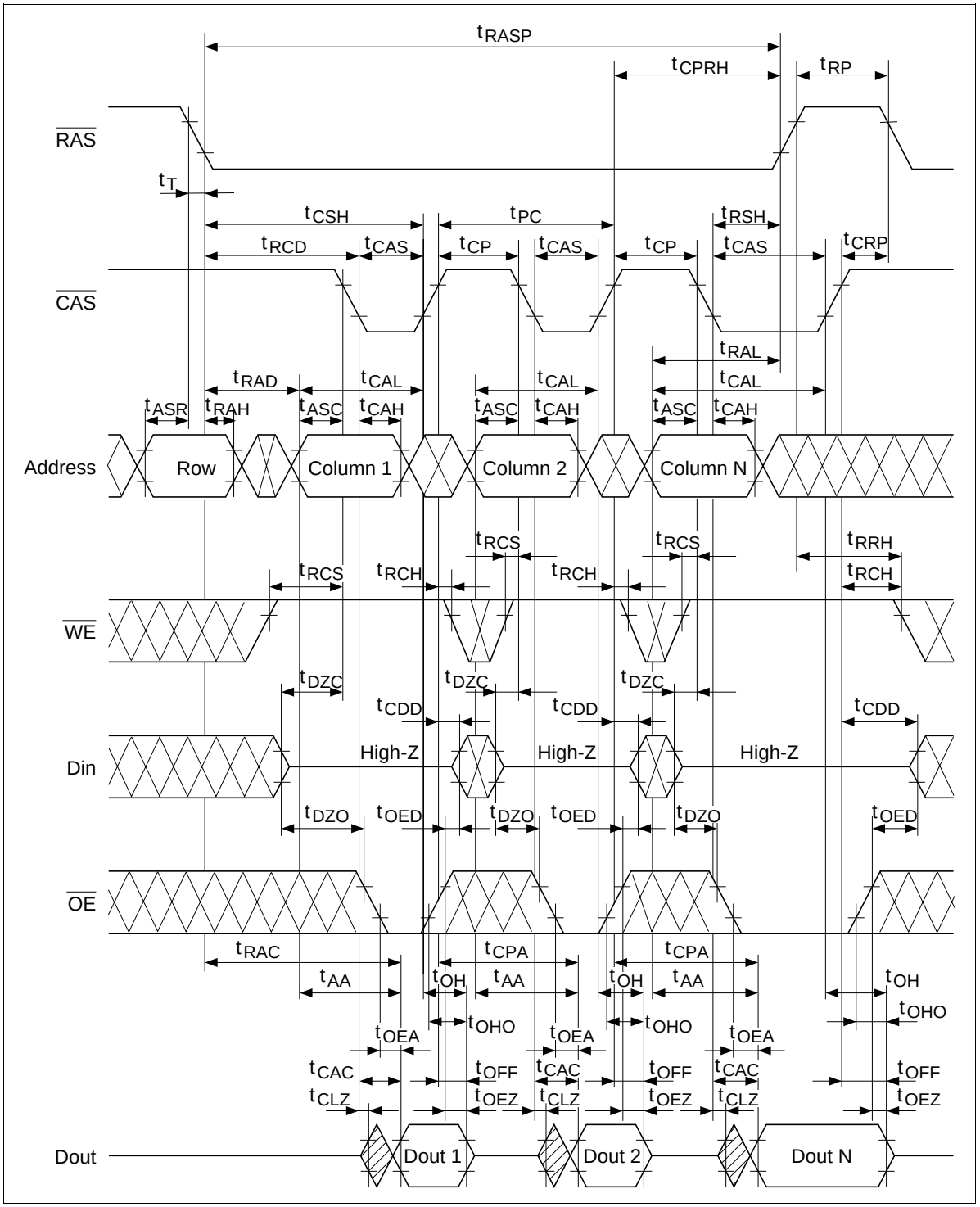
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



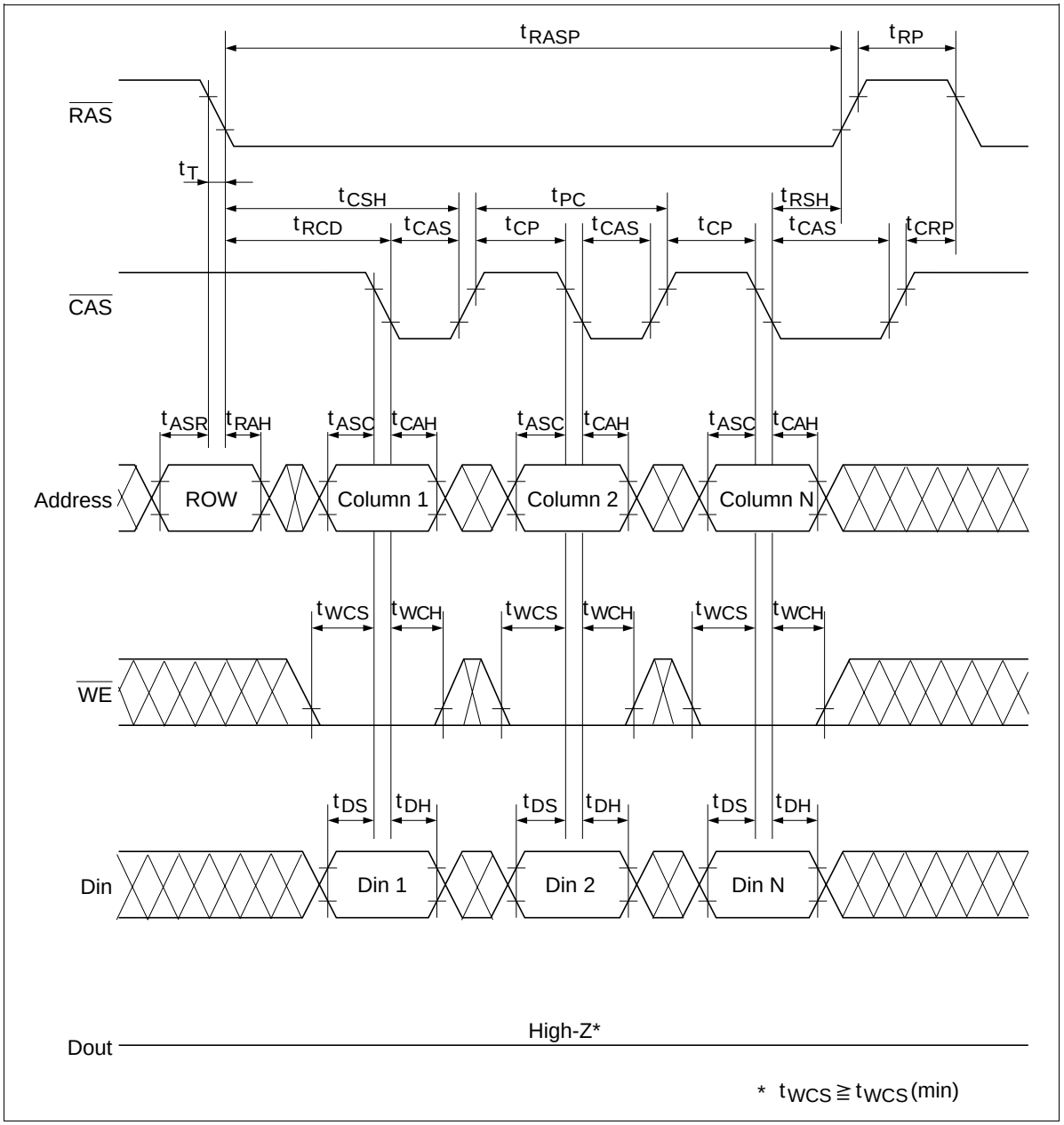
Hidden Refresh Cycle



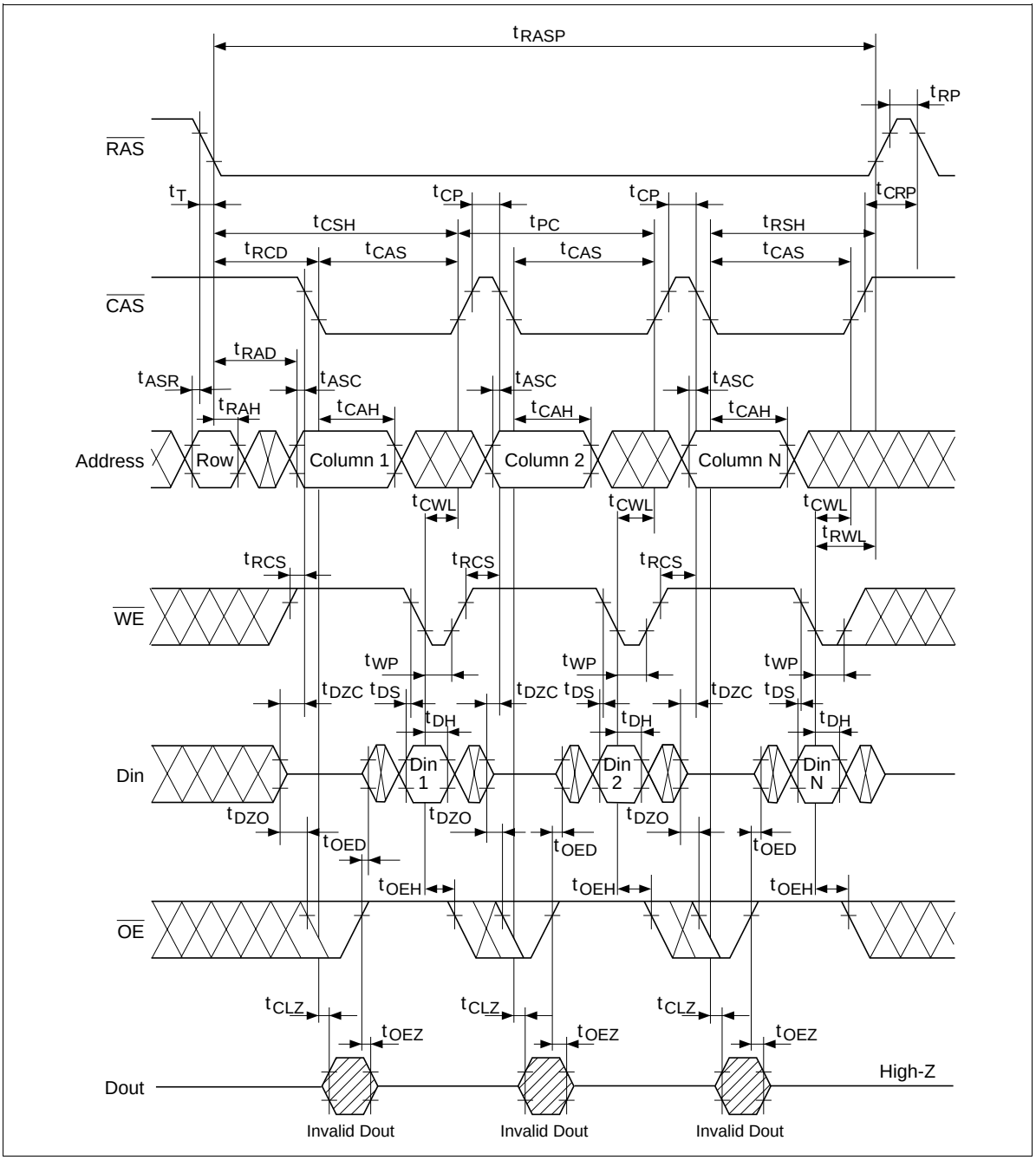
Fast Page Mode Read Cycle



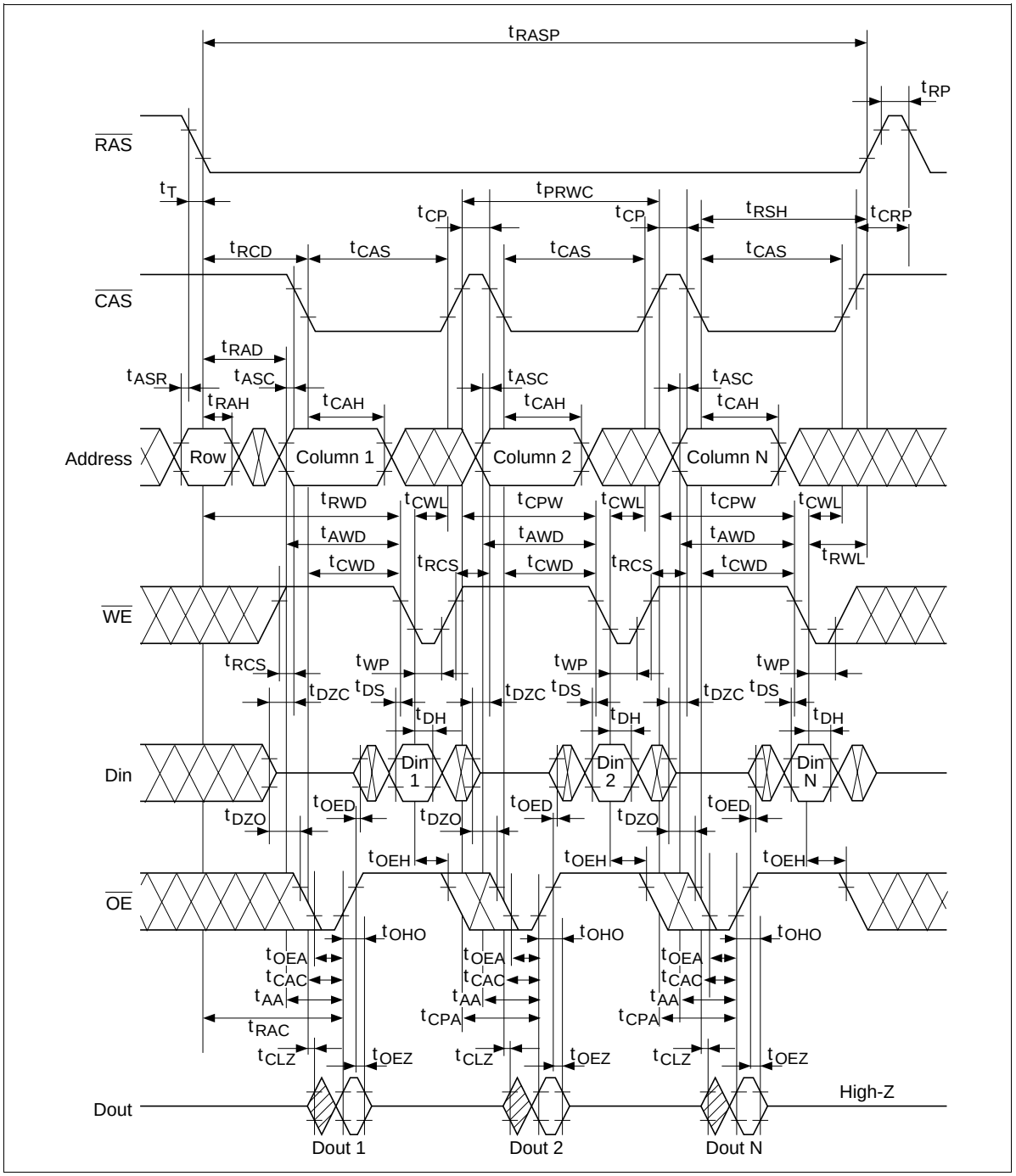
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle*[18]

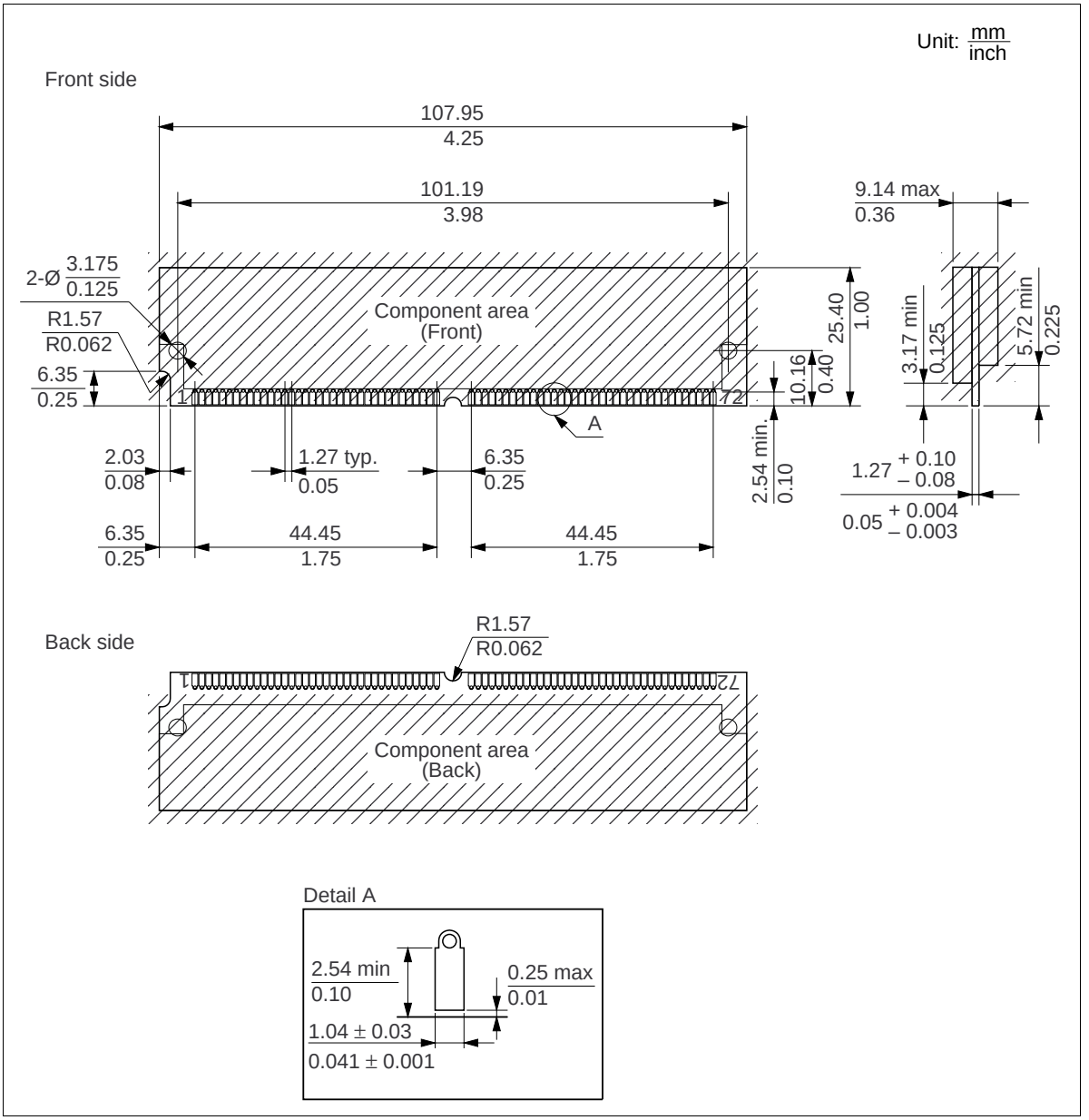


Fast Page Mode Read-Modify-Write Cycle*[18]

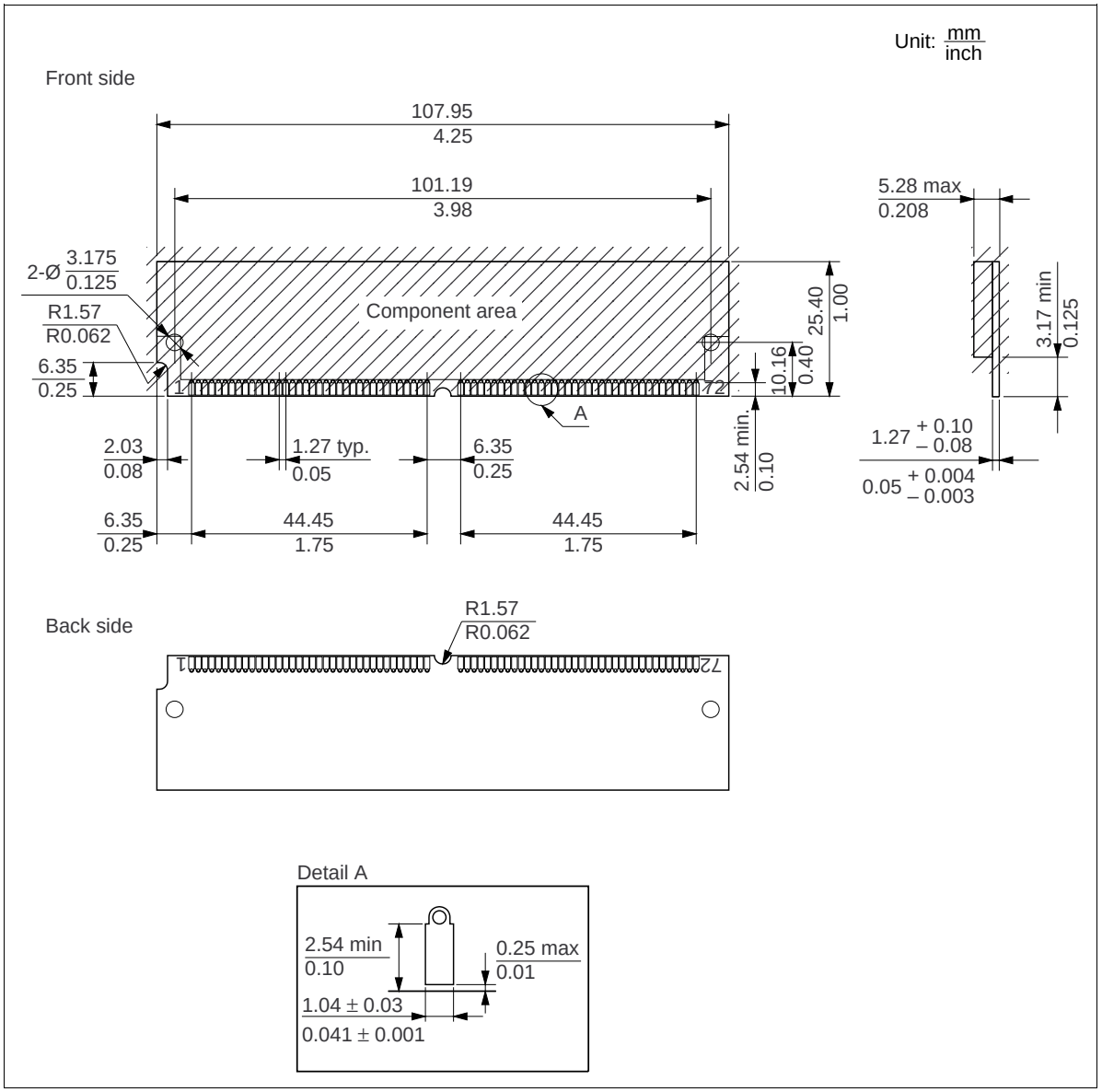


Physical Outline

HB56A841BR Series



HB56A441BR Series



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Feb. 20, 1997	Initial issue		