
HB56S872ESN Series, HB56S864ESN Series

8,388,608-word $\times$ 72-bit High Density Dynamic RAM Module
8,388,608-word $\times$ 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-778A (Z)

Rev. 1.0

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Description

The HB56S872ESN, HB56S864ESN belong to 8 Byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56S872ESN is a $8\text{M} \times 72$ dynamic RAM module, mounted 36 pieces of 16-Mbit DRAM (HM5116405) sealed in TCP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56S864ESN is a $8\text{M} \times 64$ dynamic RAM module, mounted 32 pieces of 16-Mbit DRAM (HM5116405) sealed in TCP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56S872ESN, HB56S864ESN offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56S872ESN, HB56S864ESN is 168-pin socket type package (dual lead out). Therefore, the HB56S872ESN, HB56S864ESN make high density mounting possible without surface mount technology. The HB56S872ESN, HB56S864ESN provide common data inputs and outputs. Decoupling capacitors are mounted beneath each TCP on the module board.

Features

- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 5.0 V ($\pm 5\%$) supply
- JEDEC standard outline unbuffered 8 byte DIMM
- High speed
 - Access time: $t_{\text{RAC}} = 60/70 \text{ ns (max)}$
 $t_{\text{CAC}} = 15/18 \text{ ns (max)}$
- Low power dissipation
 - Active mode: 8.03/7.09 W (max) (HB56S872ESN)
7.14/6.30 W (max) (HB56S864ESN)
 - Standby mode (TTL): 378 mW (max) (HB56S872ESN)
(TTL): 336 mW (max) (HB56S864ESN)
(CMOS): 189 mW (max) (HB56S872ESN)
(CMOS): 168 mW (max) (HB56S864ESN)

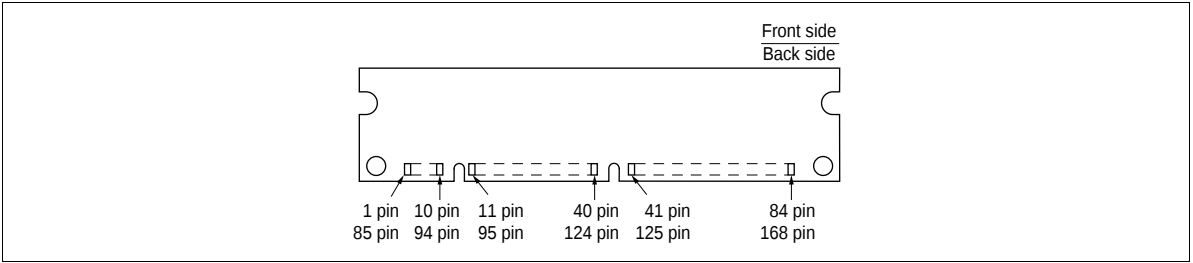
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- EDO page mode capability
- 4,096 refresh cycle: 64 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh

Ordering Information

Type No.	Access time	Package	Contact pad
HB56S872ESN-6	60 ns	168-pin dual lead out socket type	Gold
HB56S872ESN-7	70 ns		
HB56S864ESN-6	60 ns		
HB56S864ESN-7	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	36	A6	71	DQ26	106	CB5 (NC)* ⁶
2	DQ0	37	A8	72	DQ27	107	V _{SS}
3	DQ1	38	A10	73	V _{CC}	108	NC
4	DQ2	39	NC	74	DQ28	109	NC
5	DQ3	40	V _{CC}	75	DQ29	110	V _{CC}
6	V _{CC}	41	V _{CC}	76	DQ30	111	NC
7	DQ4	42	NC	77	DQ31	112	$\overline{\text{CAS4}}$
8	DQ5	43	V _{SS}	78	V _{SS}	113	$\overline{\text{CAS5}}$
9	DQ6	44	$\overline{\text{OE2}}$	79	NC	114	$\overline{\text{RAS1}}$
10	DQ7	45	$\overline{\text{RAS2}}$	80	NC	115	NC
11	DQ8	46	$\overline{\text{CAS2}}$	81	NC	116	V _{SS}
12	V _{SS}	47	$\overline{\text{CAS3}}$	82	SDA	117	A1
13	DQ9	48	$\overline{\text{WE2}}$	83	SCL	118	A3
14	DQ10	49	V _{CC}	84	V _{CC}	119	A5
15	DQ11	50	NC	85	V _{SS}	120	A7
16	DQ12	51	NC	86	DQ32	121	A9
17	DQ13	52	CB2 (NC)* ³	87	DQ33	122	A11
18	V _{CC}	53	CB3 (NC)* ⁴	88	DQ34	123	NC
19	DQ14	54	V _{SS}	89	DQ35	124	V _{CC}
20	DQ15	55	DQ16	90	V _{CC}	125	NC
21	CB0 (NC)* ¹	56	DQ17	91	DQ36	126	NC
22	CB1 (NC)* ²	57	DQ18	92	DQ37	127	V _{SS}
23	V _{SS}	58	DQ19	93	DQ38	128	NC
24	NC	59	V _{CC}	94	DQ39	129	$\overline{\text{RAS3}}$
25	NC	60	DQ20	95	DQ40	130	$\overline{\text{CAS6}}$
26	V _{CC}	61	NC	96	V _{SS}	131	$\overline{\text{CAS7}}$
27	$\overline{\text{WE0}}$	62	NC	97	DQ41	132	NC
28	$\overline{\text{CAS0}}$	63	NC	98	DQ42	133	V _{CC}
29	$\overline{\text{CAS1}}$	64	V _{SS}	99	DQ43	134	NC
30	$\overline{\text{RAS0}}$	65	DQ21	100	DQ44	135	NC
31	$\overline{\text{OE0}}$	66	DQ22	101	DQ45	136	CB6 (NC)* ⁷
32	V _{SS}	67	DQ23	102	V _{CC}	137	CB7 (NC)* ⁸
33	A0	68	V _{SS}	103	DQ46	138	V _{SS}
34	A2	69	DQ24	104	DQ47	139	DQ48
35	A4	70	DQ25	105 (NC)* ⁵	CB4	140	DQ49

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Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
141	DQ50	148	V _{SS}	155	DQ58	162	V _{SS}
142	DQ51	149	DQ53	156	DQ59	163	NC
143	V _{CC}	150	DQ54	157	V _{CC}	164	NC
144	DQ52	151	DQ55	158	DQ60	165	SA0
145	NC	152	V _{SS}	159	DQ61	166	SA1
146	NC	153	DQ56	160	DQ62	167	SA2
147	NC	154	DQ57	161	DQ63	168	V _{CC}

- Notes:
- 1. CB0: HB56S872ESN, NC: HB56S864ESN
 - 2. CB1: HB56S872ESN, NC: HB56S864ESN
 - 3. CB2: HB56S872ESN, NC: HB56S864ESN
 - 4. CB3: HB56S872ESN, NC: HB56S864ESN
 - 5. CB4: HB56S872ESN, NC: HB56S864ESN
 - 6. CB5: HB56S872ESN, NC: HB56S864ESN
 - 7. CB6: HB56S872ESN, NC: HB56S864ESN
 - 8. CB7: HB56S872ESN, NC: HB56S864ESN

Pin Description

Pin name	Function
A0 to A11	Address input — Row address: A0 to A11 — Column address: A0 to A9 — Refresh address: A0 to A11
DQ0 to DQ63	Data-in/data-out
$\overline{\text{RAS0}}$ to $\overline{\text{RAS3}}$	Row address strobe
$\overline{\text{CAS0}}$ to $\overline{\text{CAS7}}$	Column address strobe
$\overline{\text{WE0}}$, $\overline{\text{WE2}}$	Read/Write enable
$\overline{\text{OE0}}$, $\overline{\text{OE2}}$	Output enable
SDA	Serial data out (Bit0 to 7)
SCL	Clock for presence detect
SA0 to SA2	Serial address input
CB0 to CB7*1	Check bit
V _{cc}	Power supply
V _{ss}	Ground
NC	No connection

Note: 1. This function is supported only HB56S872ESN.

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Serial PD Matrix*¹

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	0	1	0	02	EDO
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	1	0	02	2
6	Module data width (HB56S872ESN)	0	1	0	0	1	0	0	0	48	72
	(HB56S864ESN)	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	0	00	TTL
9	$\overline{\text{RAS}}$ access time -6	0	0	1	1	1	1	0	0	3C	$t_{\text{RAC}} = 60 \text{ ns}$
	-7	0	1	0	0	0	1	1	0	46	$t_{\text{RAC}} = 70 \text{ ns}$
10	$\overline{\text{CAS}}$ access time -6	0	0	0	0	1	1	1	1	0F	$t_{\text{CAC}} = 15 \text{ ns}$
	-7	0	0	0	1	0	0	1	0	12	$t_{\text{CAC}} = 18 \text{ ns}$
11	Module configuration type (HB56S872ESN)	0	0	0	0	0	0	1	0	02	ECC
	(HB56S864ESN)	0	0	0	0	0	0	0	0	00	Non-parity
12	Refresh rate/type	0	0	0	0	0	0	0	0	00	Normal (15.625 μs)
13	DRAM width	0	0	0	0	0	1	0	0	04	$\times 4$
14	Error checking DRAM width (HB56S872ESN)	0	0	0	0	0	1	0	0	04	$\times 4$
	(HB56S864ESN)	0	0	0	0	0	0	0	0	00	
15 to 31	Reserved for future offerings	0	0	0	0	0	0	0	0	00	
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future offerings
62	SPD data revision code	0	0	0	0	0	0	0	1	01	Rev. 1

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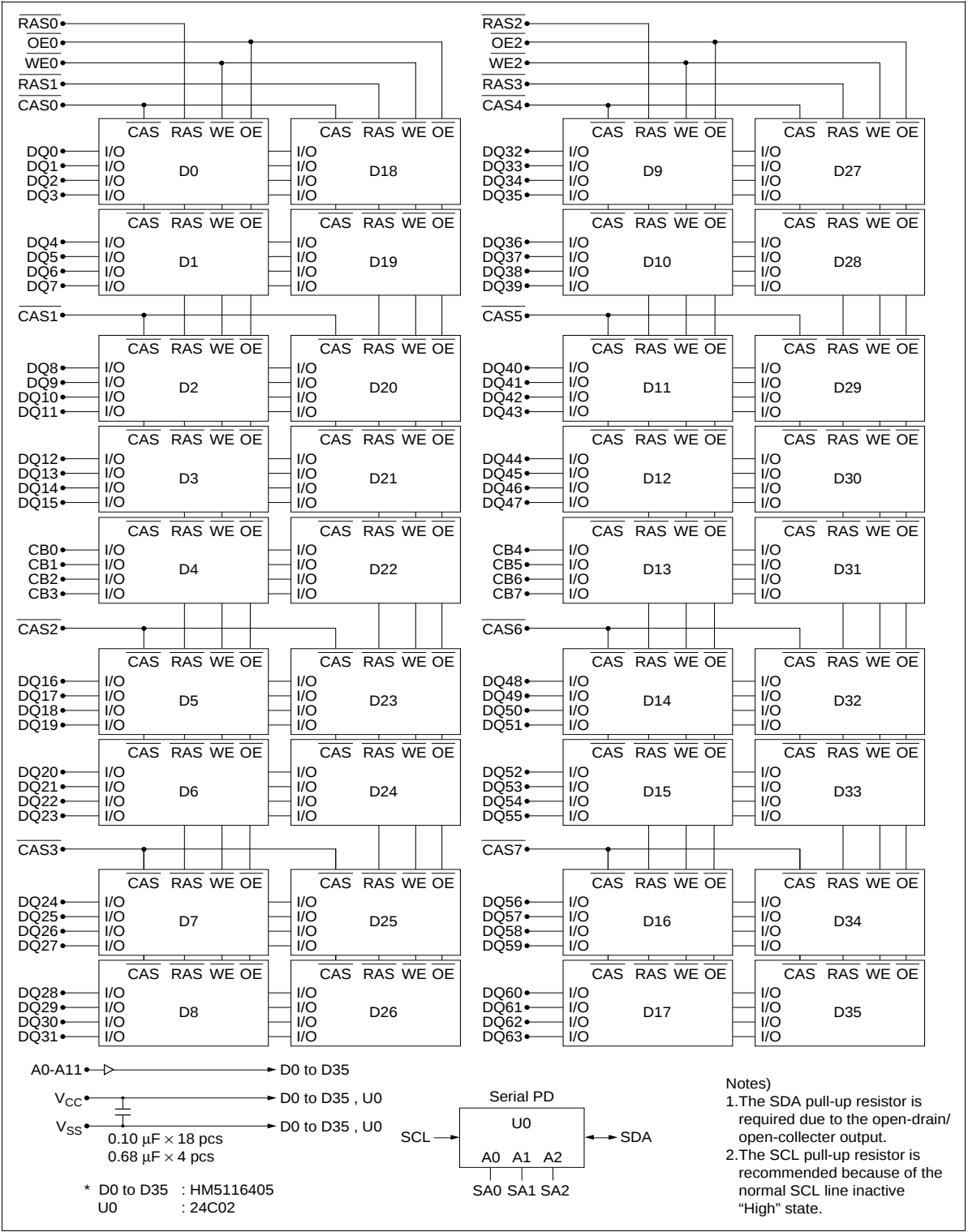
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
63	Checksum for bytes 0 to 62 (HB56S872ESN-6)	0	1	0	0	0	0	0	0	40	
	(HB56S864ESN-6)	0	0	1	1	0	0	1	0	32	
	(HB56S872ESN-7)	0	1	0	0	1	1	0	1	4D	
	(HB56S864ESN-7)	0	0	1	1	1	1	1	1	3F	
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	Hitachi
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	×	ASCII-8bit code*2
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
77	Manufacturer's part number	0	1	0	1	0	0	1	1	53	S
78	Manufacturer's part number	0	0	1	1	1	0	0	0	38	8
79	Manufacturer's part number (HB56S872ESN)	0	0	1	1	0	1	1	1	37	7
	(HB56S864ESN)	0	0	1	1	0	1	1	0	36	6
80	Manufacturer's part number (HB56S872ESN)	0	0	1	1	0	0	1	0	32	2
	(HB56S864ESN)	0	0	1	1	0	1	0	0	34	4
81	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
82	Manufacturer's part number	0	1	0	1	0	0	1	1	53	S
83	Manufacturer's part number	0	1	0	0	1	1	1	0	4E	N
84	Manufacturer's part number	0	1	0	1	1	1	1	1	5F	—
85	Manufacturer's part number -6	0	0	1	1	0	1	1	0	36	6
	-7	0	0	1	1	0	1	1	1	37	7
86	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
87	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)

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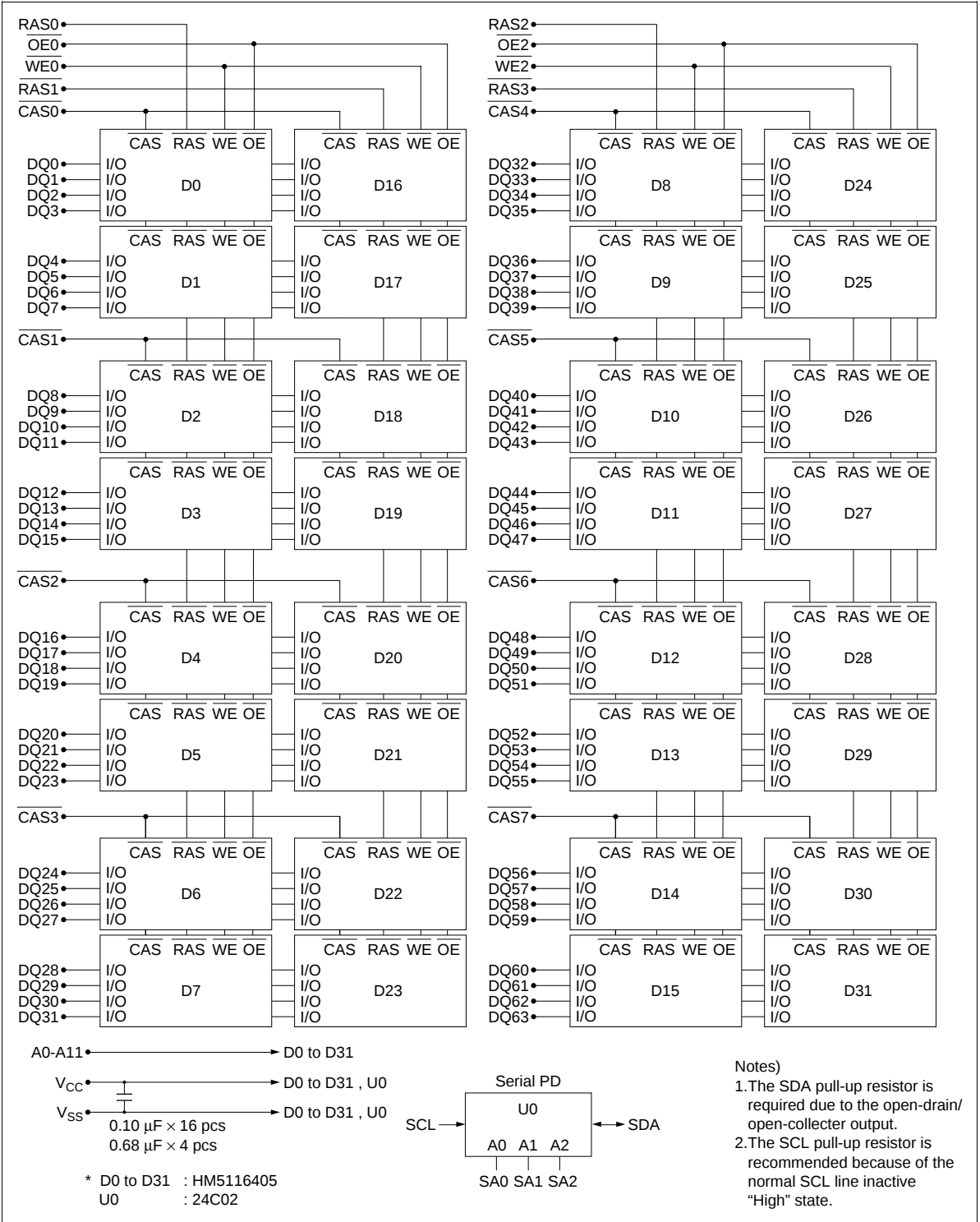
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	xx	Year-code (binary) ^{*3}
94	Manufacturing date	×	×	×	×	×	×	×	×	xx	Week-code (binary) ^{*4}
95 to 98	Assembly serial number	^{*5}									
99 to 125	Manufacturer specific data	^{*6}									
126	Reserved	0	0	0	0	0	0	0	0	00	Not use
127	Reserved	0	0	0	0	0	0	0	0	00	Not use

- Notes:
1. All serial PD data are not protected. 0: Serial data, “Low level”, 1: Serial data, “High level”
 2. Byte72 is manufacturing location code. (ex: in case of Japan, byte72 is 4Ah. 4Ah shows “J” on ASCII code.)
 3. Byte 93 (Manufacturing date-year code) ex: 61h shows year 97, 62h shows year 98.
 4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11, 24h shows week 36.
 5. Bytes 95 through 98 are assembly serial number.
 6. All bits of 99 through 125 are not defined (“1” or “0”).

Block Diagram (HB56S872ESN)



Block Diagram (HB56S864ESN)



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS} .	V_T	−0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation (HB56S872ESN)	Pt	36	W
Power dissipation (HB56S864ESN)	Pt	32	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5.0 V ±5%, V_{SS} = 0 V) (HB56S872ESN)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I _{CC1}	—	1530	—	1350	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	72	—	72	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	36	—	36	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	1530	—	1350	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	180	—	180	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	1530	—	1350	mA	t _{RC} = min	
EDO page mode current	I _{CC7}	—	1350	—	1260	mA	t _{HPC} = min	1, 3
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5.0\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) (HB56S864ESN)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I_{CC1}	—	1360	—	1200	mA	$t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	64	—	64	mA	TTL interface RAS, CAS = V_{IH} Dout = High-Z	
		—	32	—	32	mA	CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
RAS-only refresh current	I_{CC3}	—	1360	—	1200	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	160	—	160	mA	RAS = V_{IH} , CAS = V_{IL} Dout = enable	1
CAS-before-RAS refresh current	I_{CC6}	—	1360	—	1200	mA	$t_{RC} = \text{min}$	
EDO page mode current	I_{CC7}	—	1200	—	1120	mA	$t_{HPC} = \text{min}$	1, 3
Input leakage current	I_{LI}	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 5.5\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 5.5\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL} .

3. Address can be changed once or less while CAS = V_{IH} .

Capacitance (Ta = 25°C, V_{CC} = 5.0 V ±5%) (HB56S872ESN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	200	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I2}	—	62	pF	1
Input capacitance ($\overline{\text{RAS}}$)	C _{I3}	—	83	pF	1
Input capacitance ($\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I4}	—	146	pF	1
Output capacitance (DQ)	C _{I/O}	—	27	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = \text{V}_{\text{IH}}$ to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 5.0 V ±5%) (HB56S864ESN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	180	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I2}	—	48	pF	1
Input capacitance ($\overline{\text{RAS}}$)	C _{I3}	—	76	pF	1
Input capacitance ($\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I4}	—	132	pF	1
Output capacitance (DQ)	C _{I/O}	—	27	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = \text{V}_{\text{IH}}$ to disable Dout.

AC Characteristics ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0 \text{ V}$) *¹, *², *¹⁸, *¹⁹
Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period (4,096 cycles)	t_{REF}	—	64	—	64	ms	

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Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCD}	60	—	70	—	ns	

Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	t_{OEH}	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

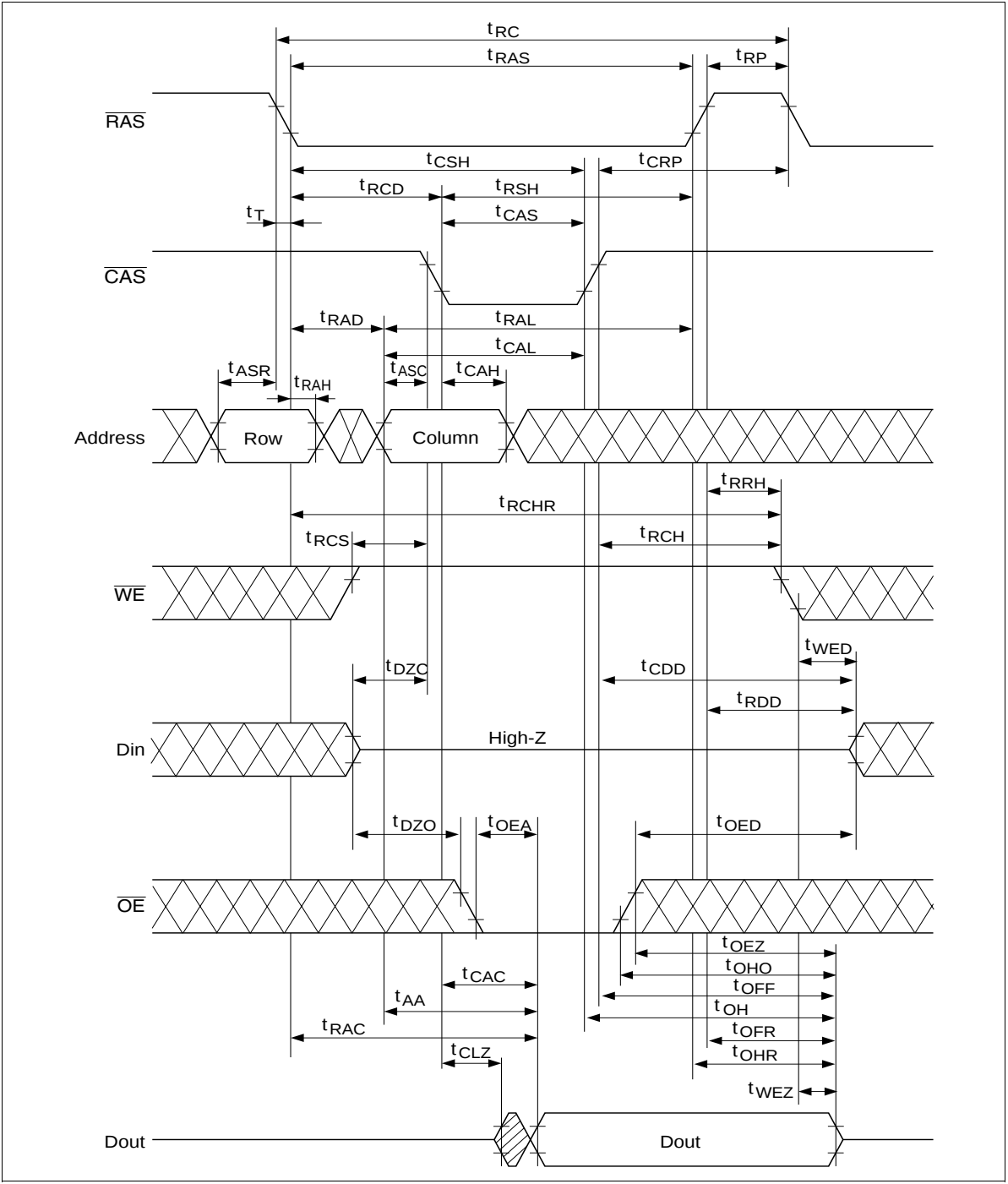
Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	ns	14

- Notes:
1. AC measurements assume $t_T = 2$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh cycle or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max) - t_{CAC} (max), then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
 11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

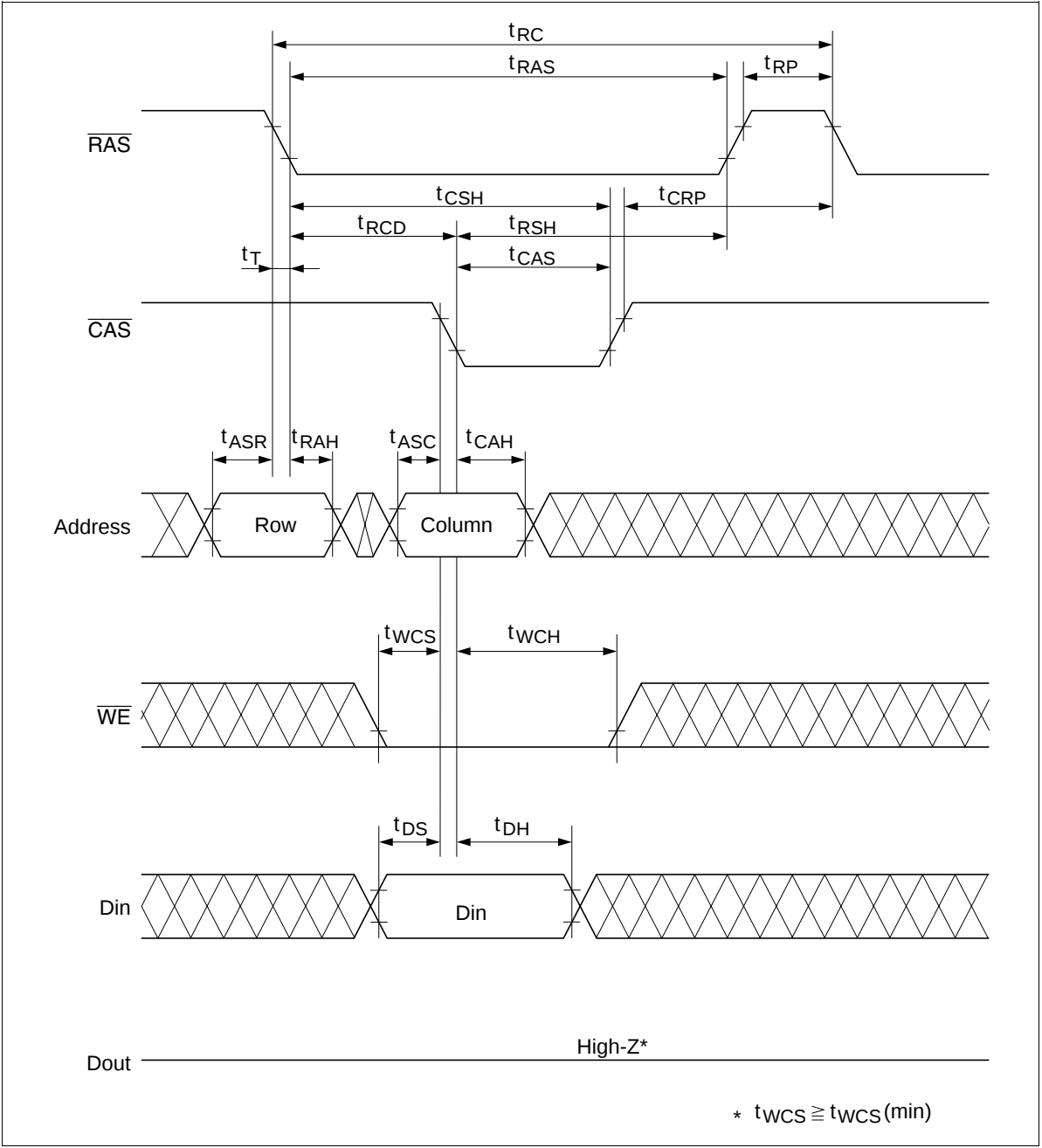
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, and $t_{AWD} \geq t_{AWD}(\text{min})$ or $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the DQ pin will remain open circuit (high impedance); $t_{\text{OEH}} < t_{\text{OEH}}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. $t_{\text{HPC}}(\text{min})$ can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2t_{\text{T}}$) becomes greater than the specified $t_{\text{HPC}}(\text{min})$ value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade $V_{\text{IH min.}} / V_{\text{IL max.}}$ level.
22. Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} , and between t_{OFFR} and t_{OFF} .
23. XXX: H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)
 // // // // //: Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*23

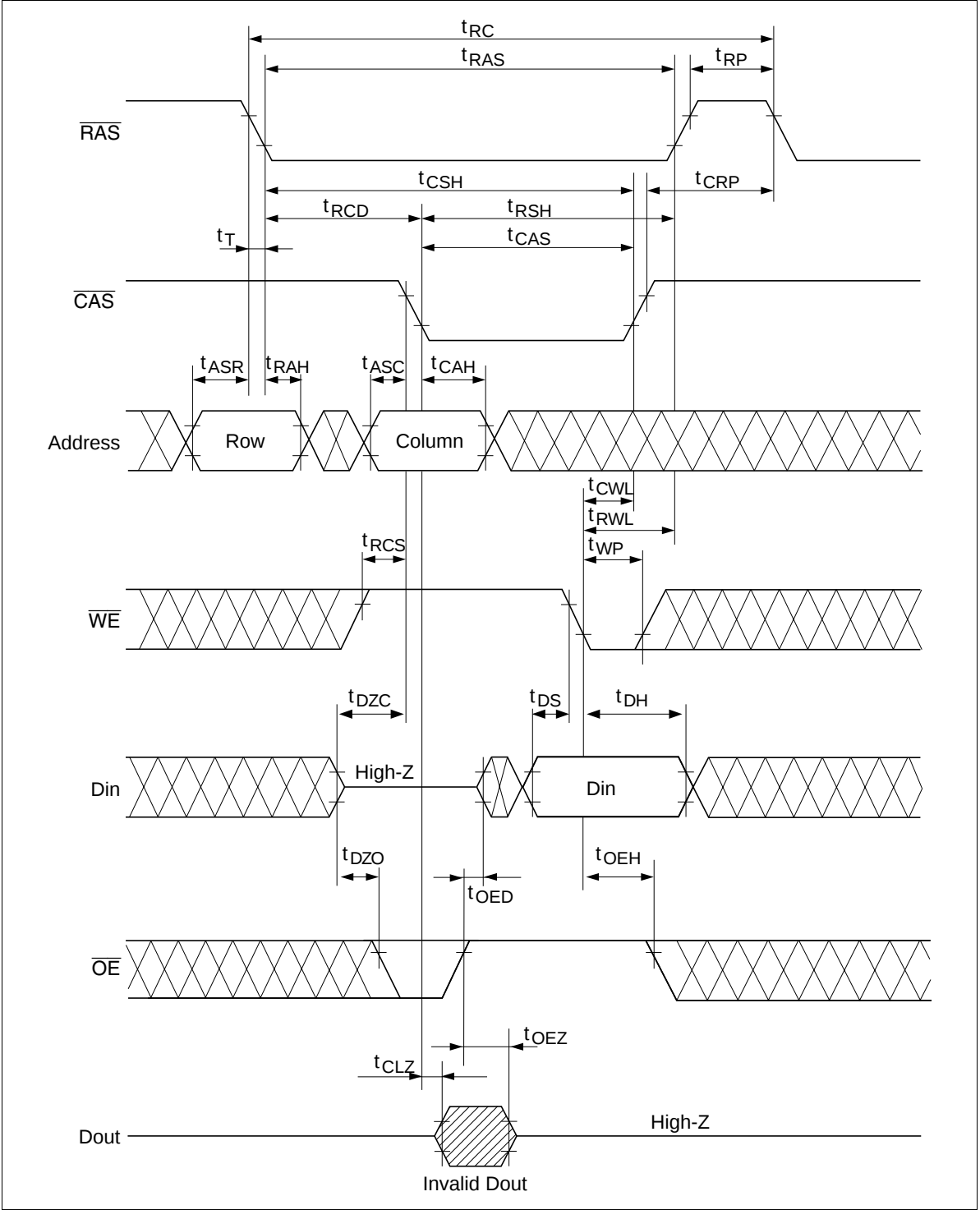
Read Cycle



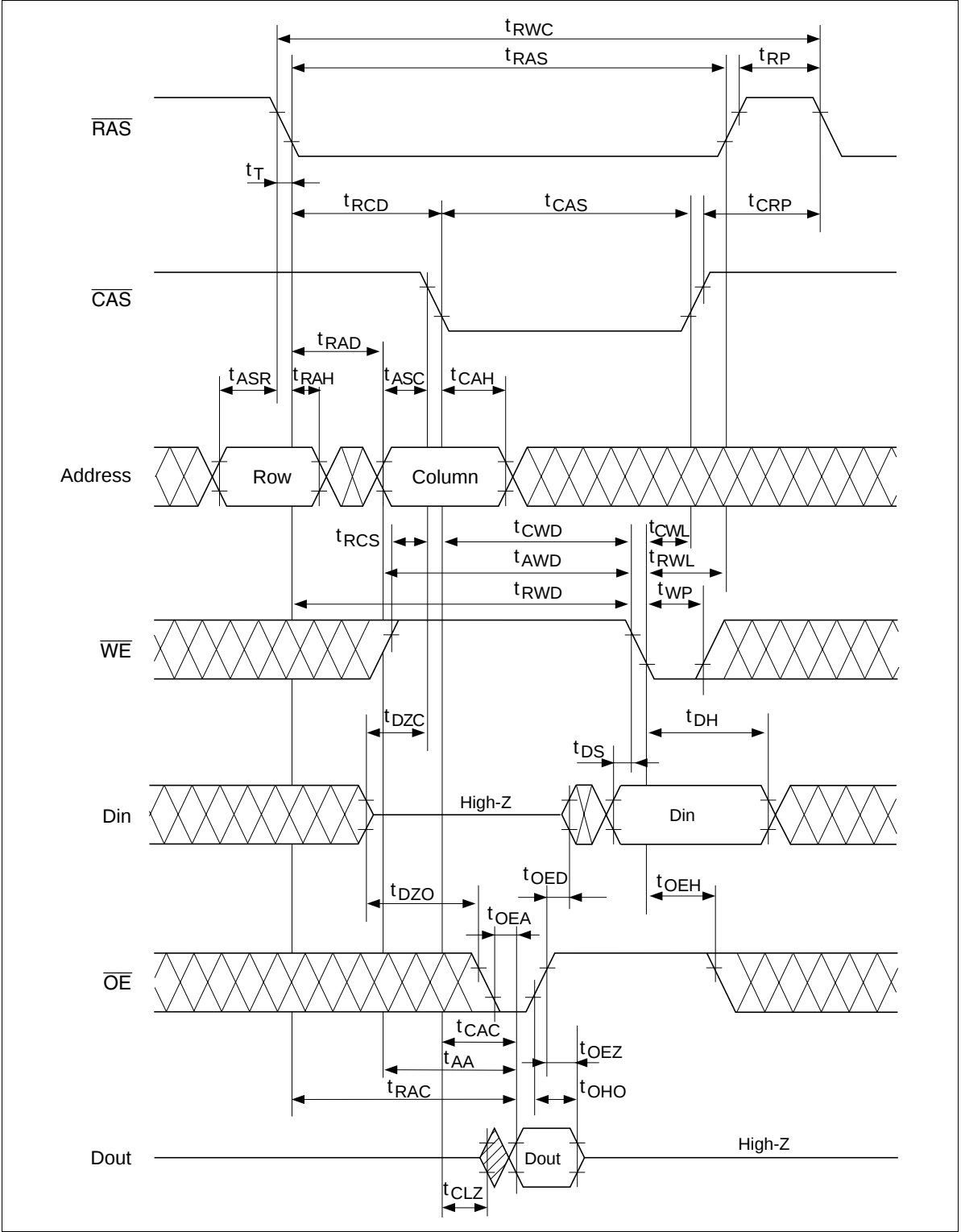
Early Write Cycle



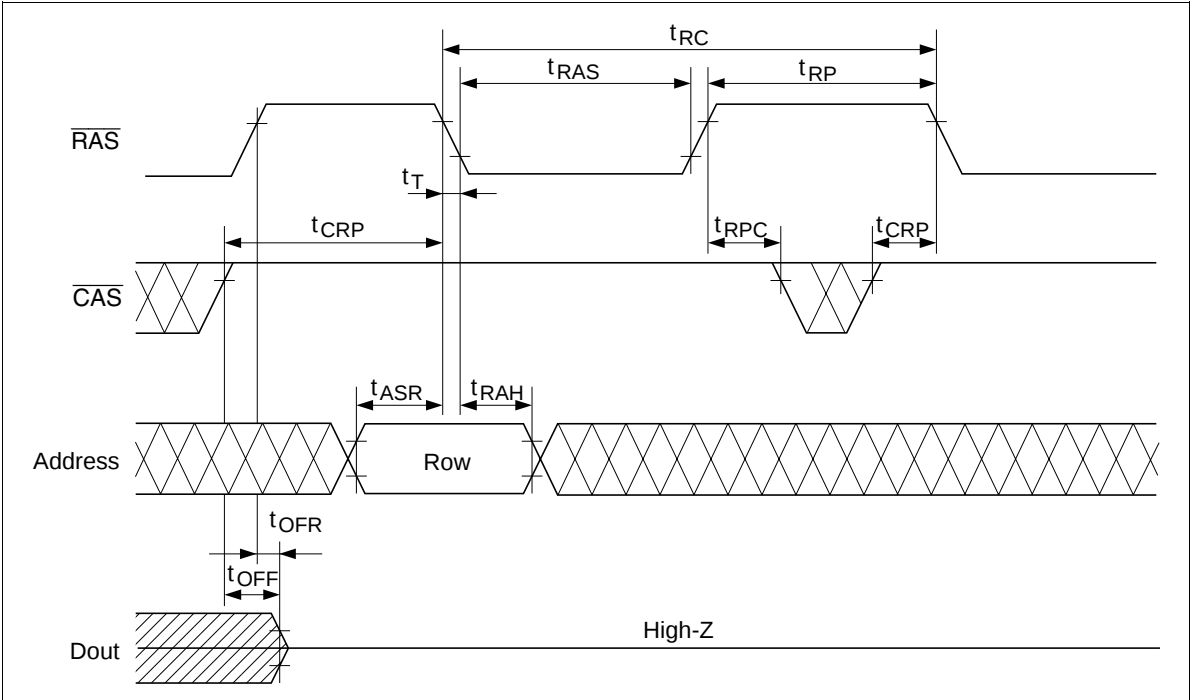
Delayed Write Cycle*18



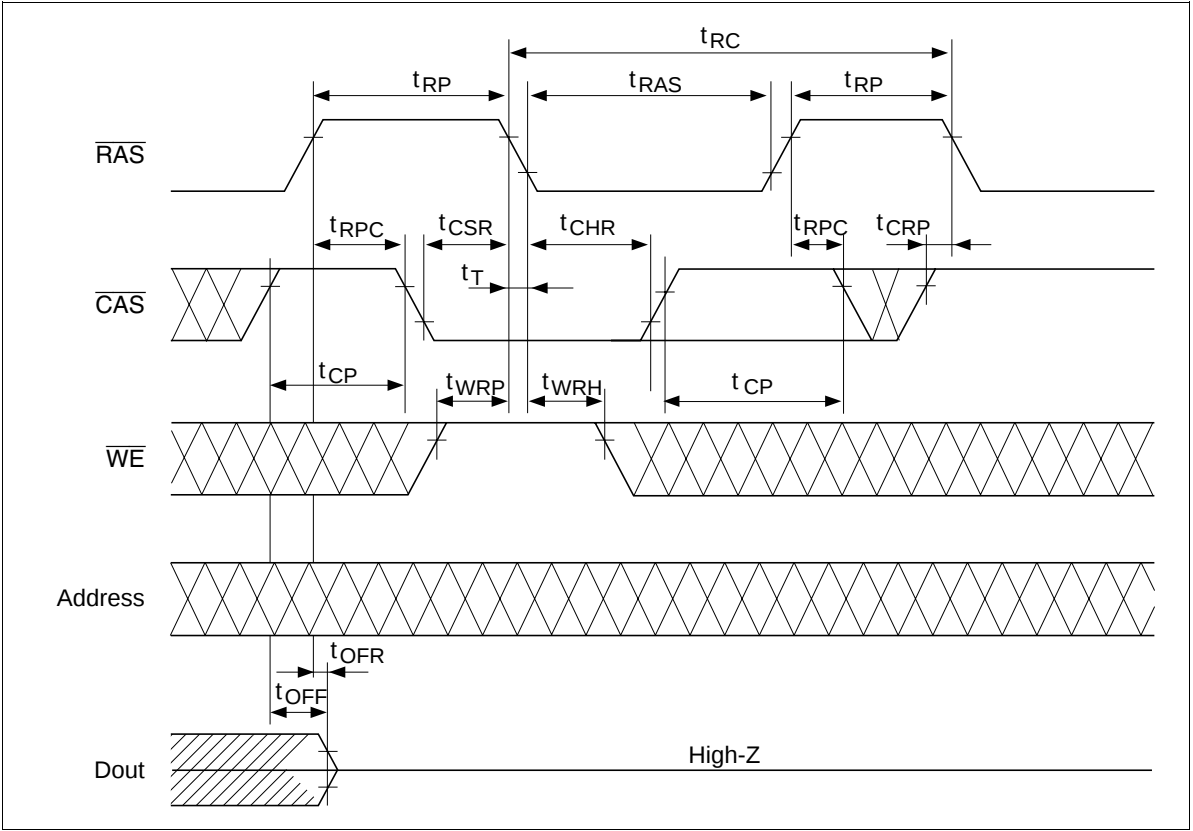
Read-Modify-Write Cycle*18



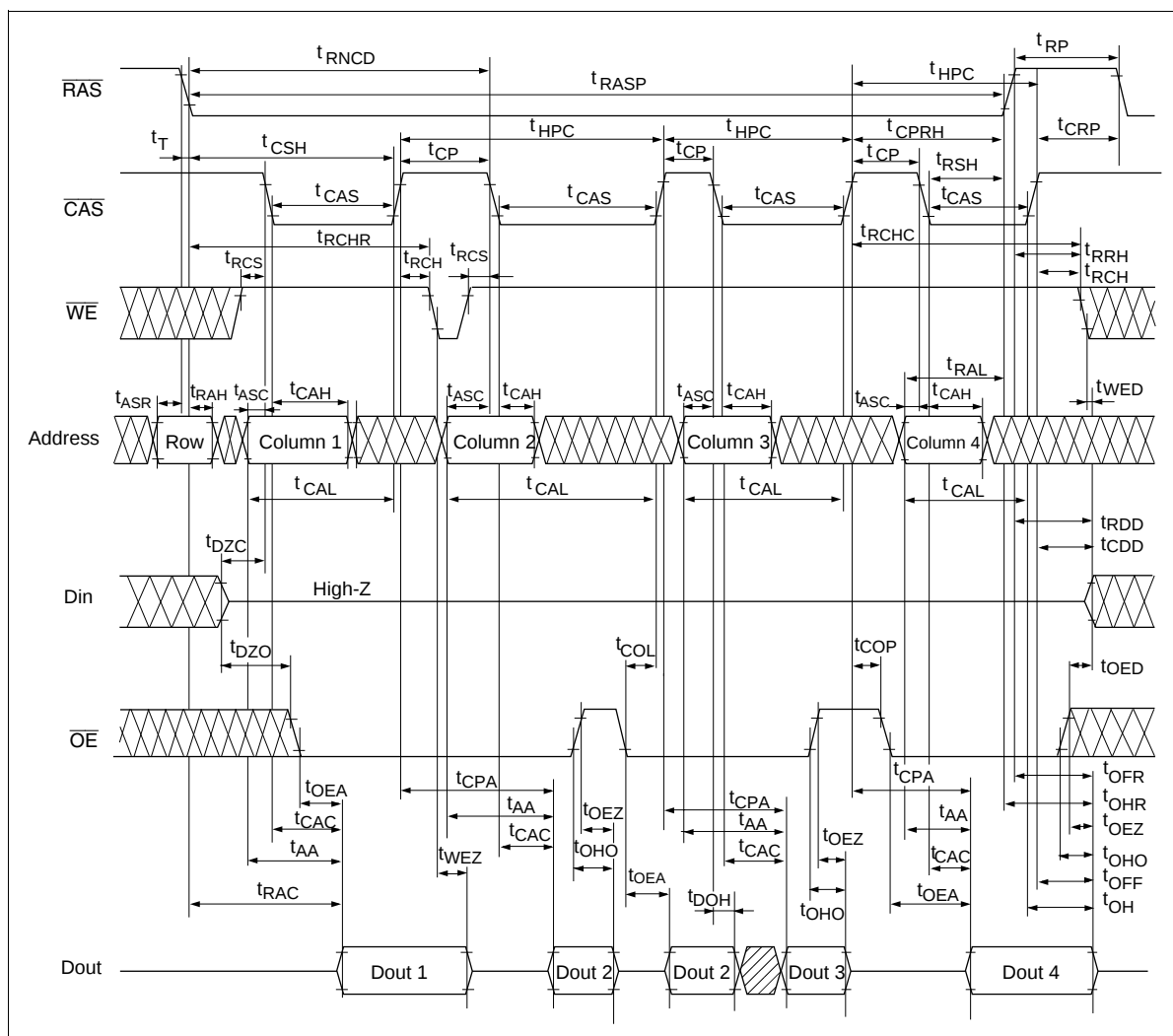
RAS-Only Refresh Cycle



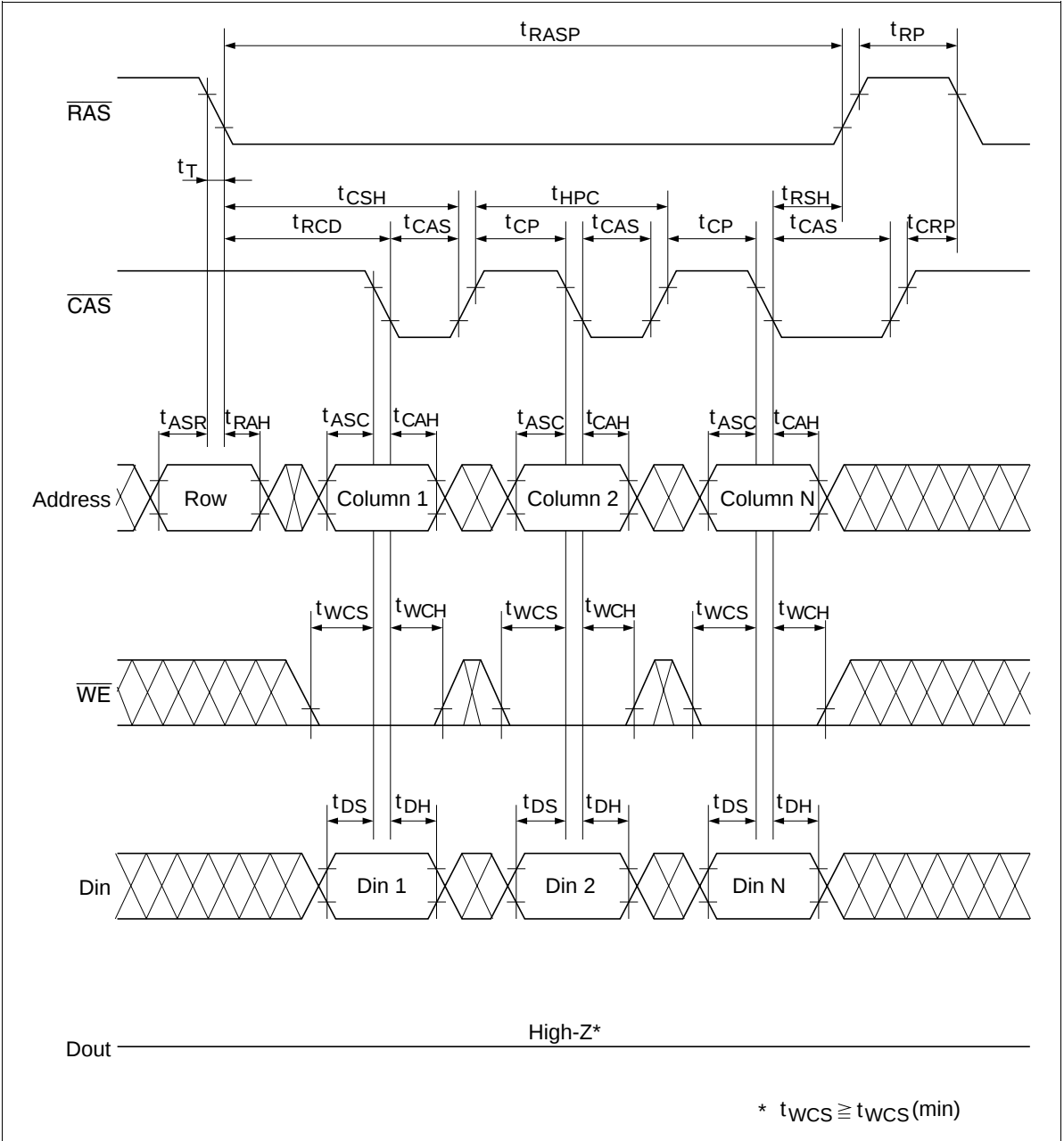
CAS-Before-RAS Refresh Cycle



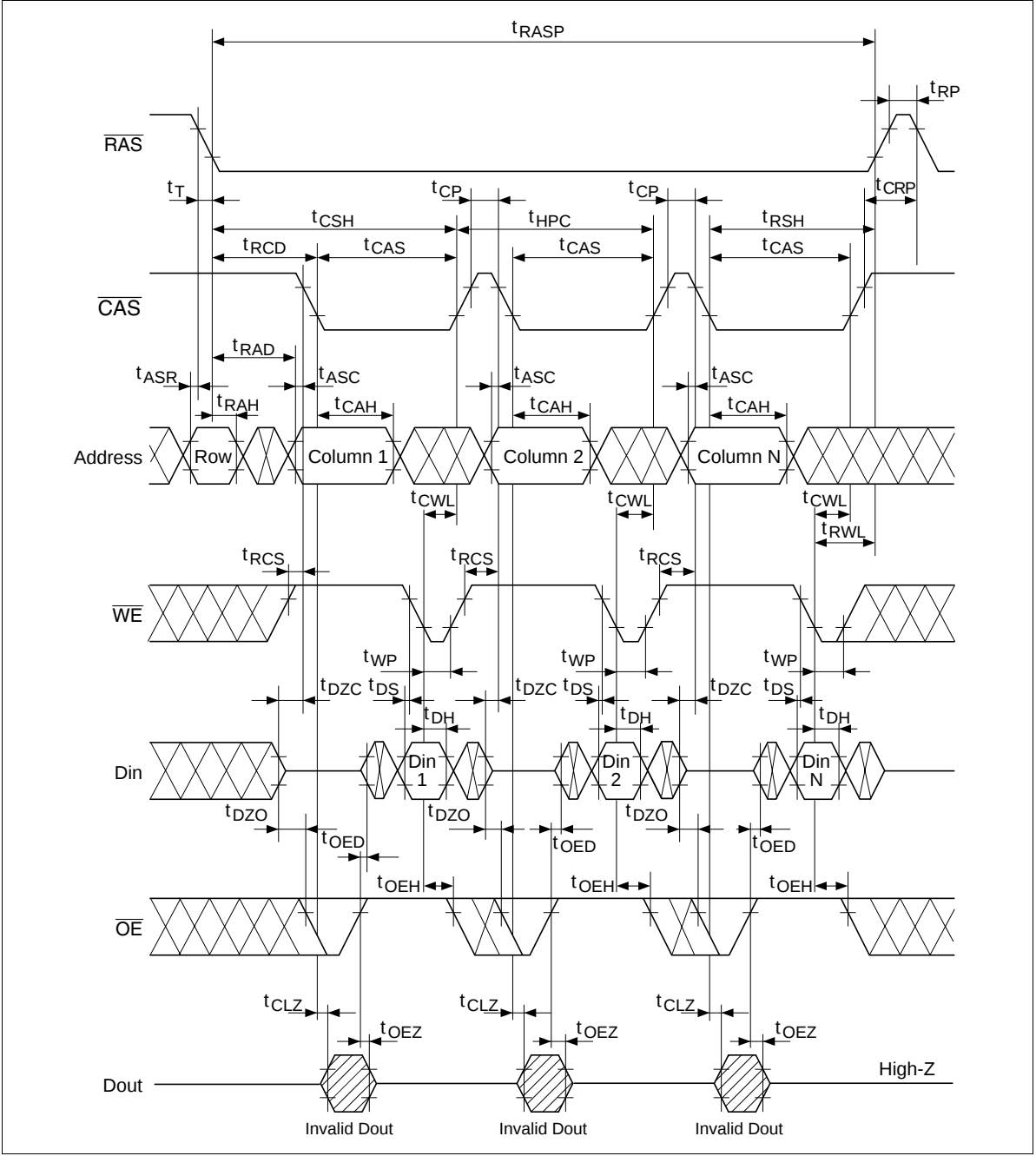
EDO Page Mode Read Cycle



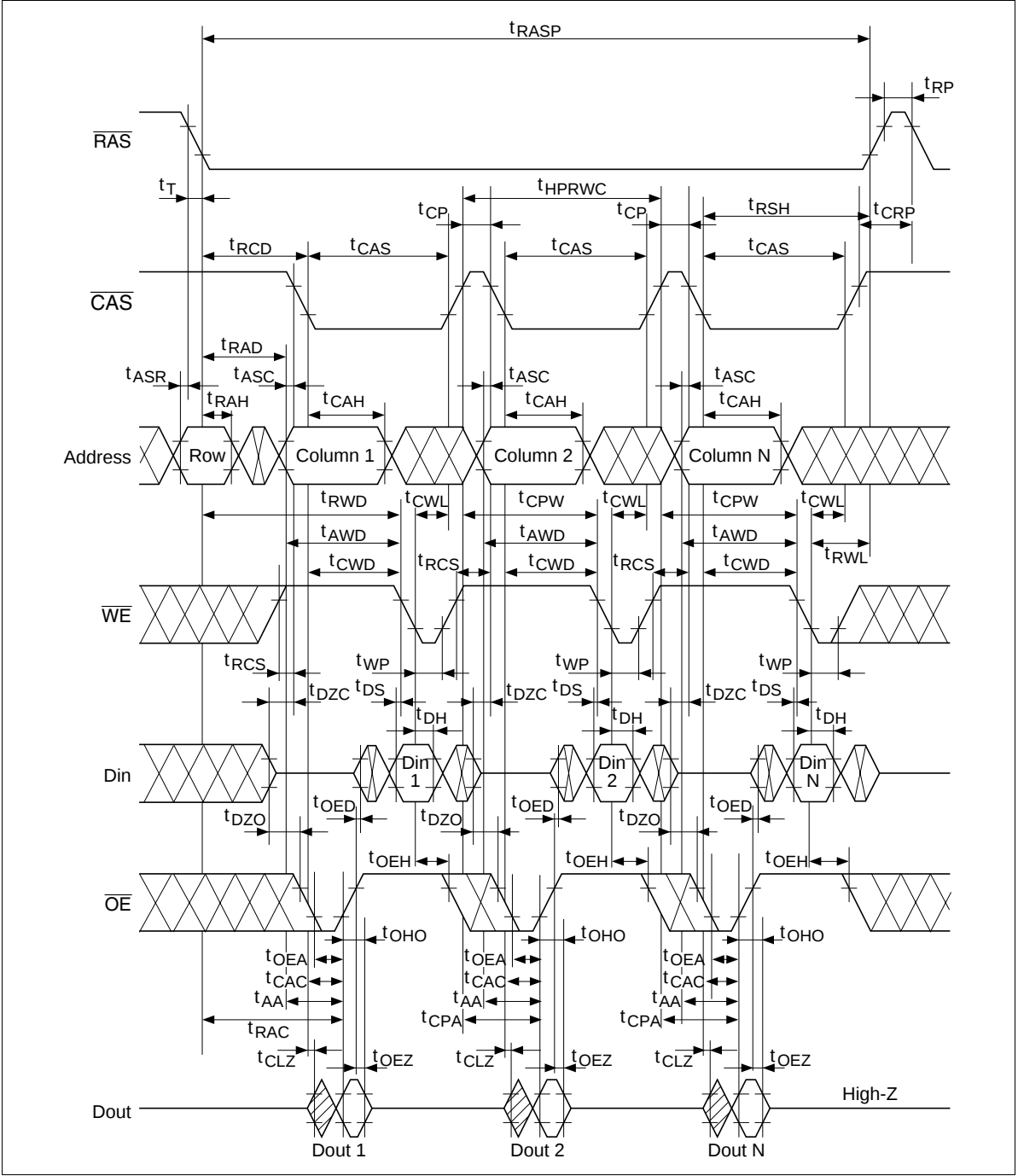
EDO Page Mode Early Write Cycle



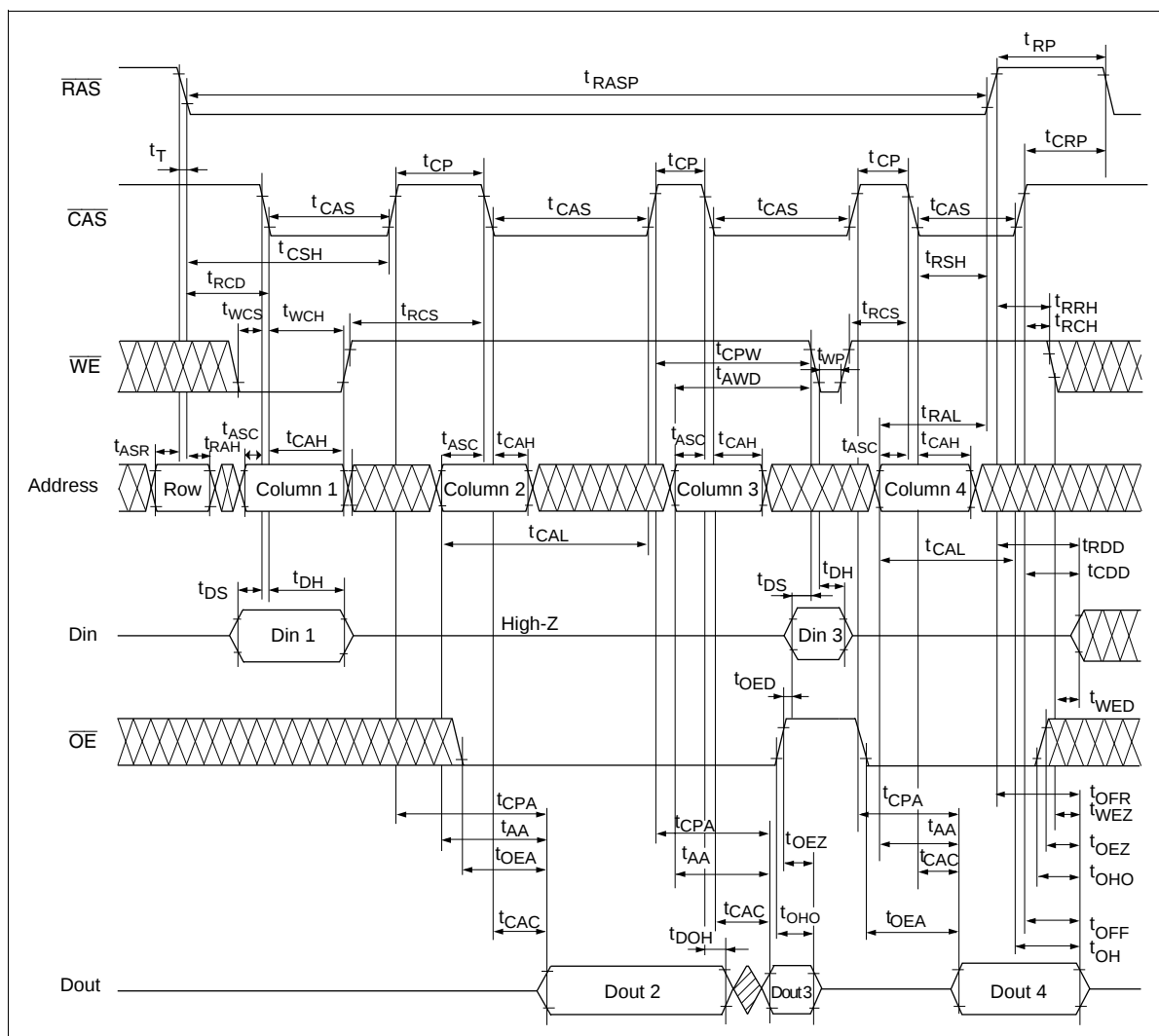
EDO Page Mode Delayed Write Cycle*18



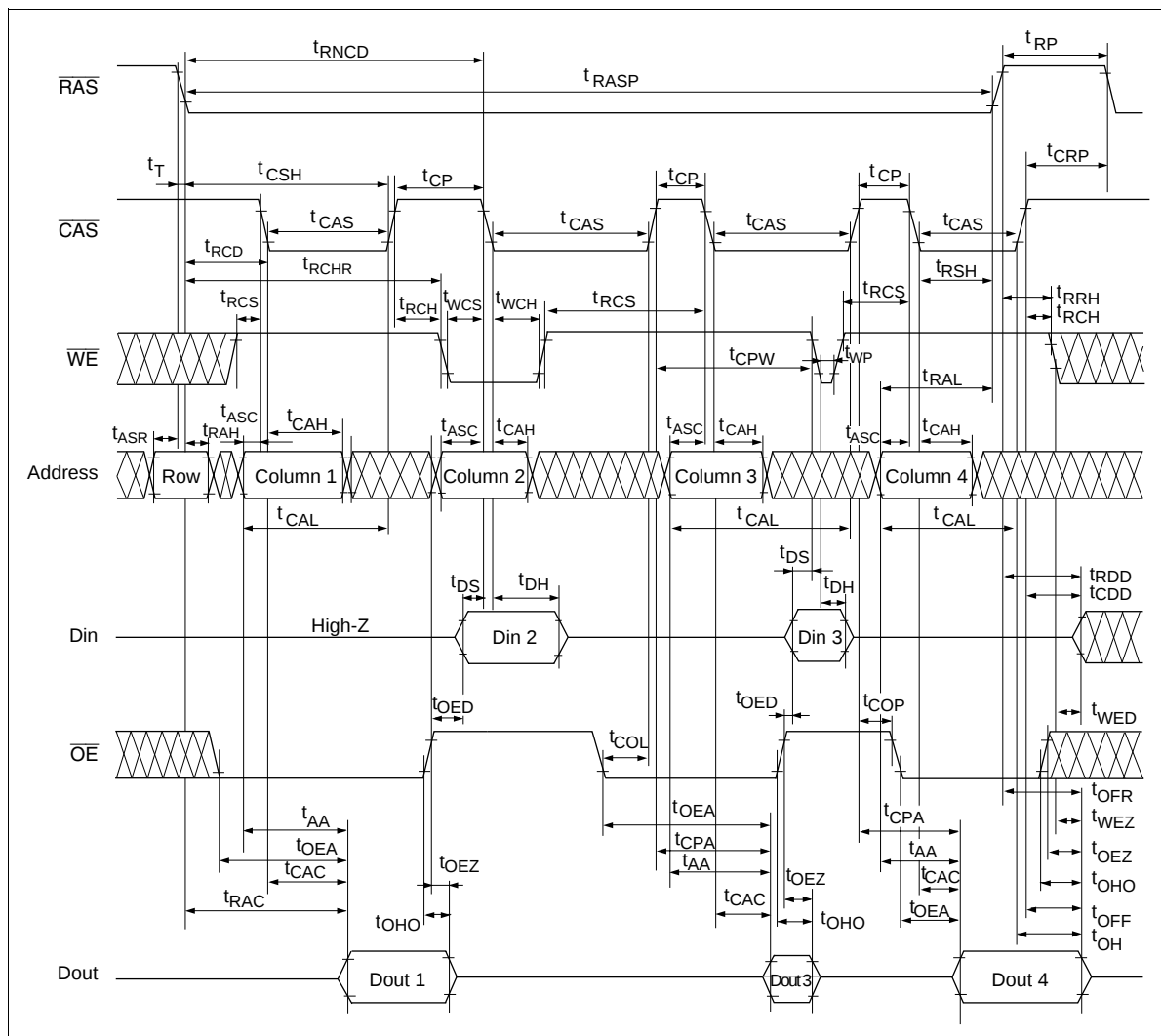
EDO Page Mode Read-Modify-Write Cycle*18



EDO Page Mode Mix Cycle (1)

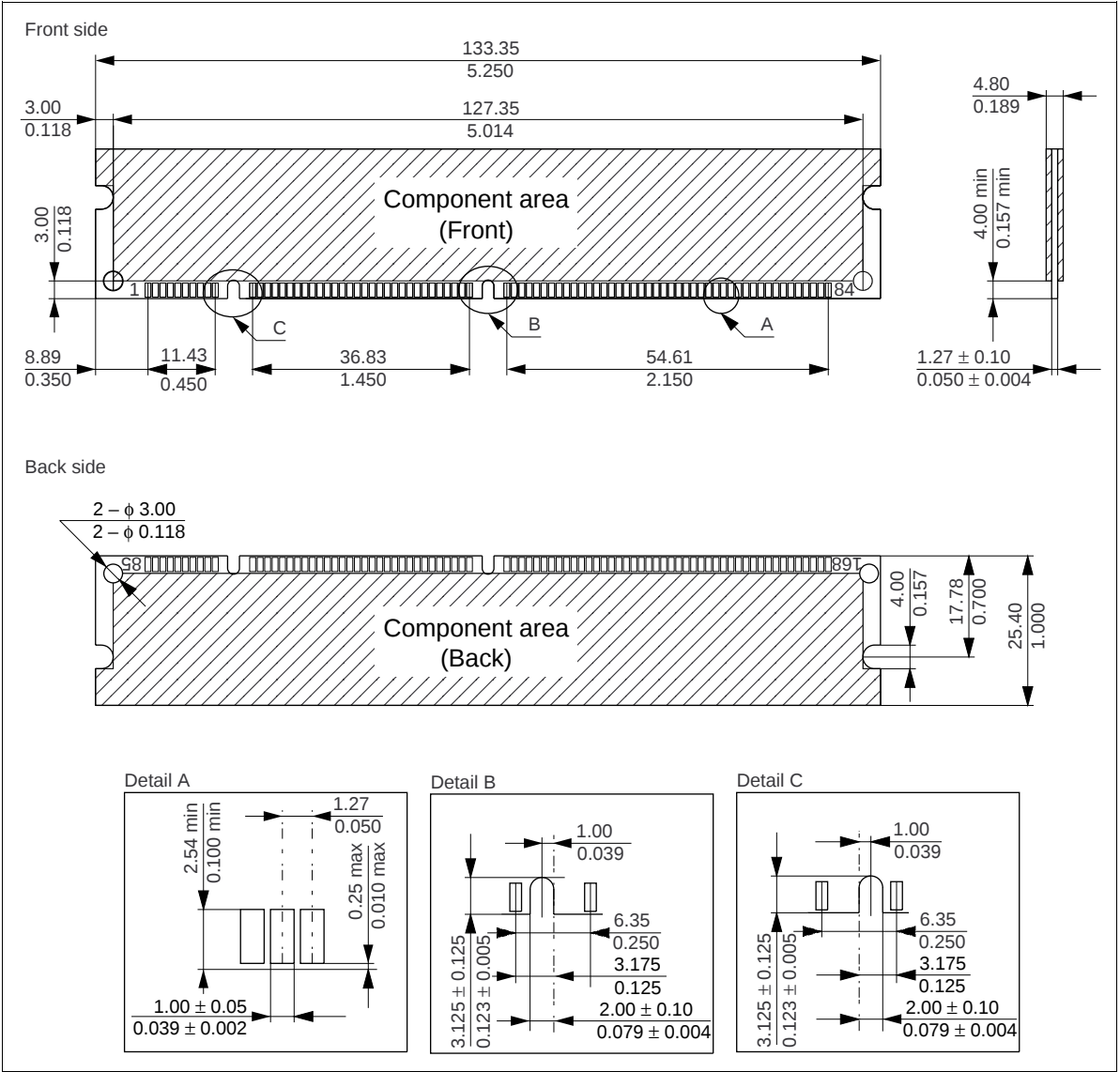


EDO Page Mode Mix Cycle (2)



Physical Outline

Unit: mm/inch



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1.0	Apr. 30, 1997	Initial issue		
