HB56U264EJ Series

2,097,152-word × 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-714A (Z)
Rev. 1.0
Jan. 27, 1997

Description

The HB56U264EJ belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56U264EJ is a 2M × 64 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117805) sealed in SOJ package and 2 pieces of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package. The HB56U264EJ offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56U264EJ is 168-pin socket type package (dual lead out). Therefore, the HB56U264EJ makes high density mounting possible without surface mount technology. The HB56U264EJ provides common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 168-pin socket type package (Dual lead out)
  - — Outline: 133.35 mm (Length) × 25.40 mm (Height) × 5.28 mm (Thickness)
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 50/60/70 ns (max)
    t_{CAC} = 18/20/23 ns (max)
- Low power dissipation
  - — Active mode: 4.96/4.54/4.12 W (max)
  - — Standby mode (TTL): 420 mW (max)
    (CMOS): 378 mW (max)
- Buffered input except $\overline{RAS}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- JEDEC standard outline buffered 8-byte DIMM
- EDO page mode capability
- 2,048 refresh cycles: 32 ms

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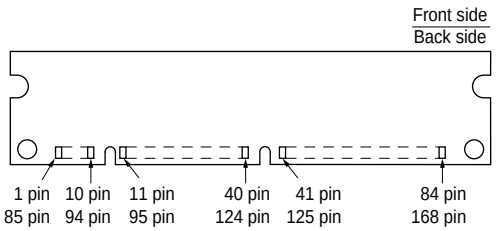
- 2 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56U264EJ-5	50 ns	168-pin dual lead out socket type	Gold
HB56U264EJ-6	60 ns		
HB56U264EJ-7	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE2}$	86	DQ36	128	NC
3	DQ1	45	$\overline{RE2}$	87	DQ37	129	NC
4	DQ2	46	$\overline{CE4}$	88	DQ38	130	$\overline{CE5}$
5	DQ3	47	$\overline{CE6}$	89	DQ39	131	$\overline{CE7}$
6	V_{CC}	48	$\overline{WE2}$	90	V_{CC}	132	$\overline{PDE}$
7	DQ4	49	V_{CC}	91	DQ40	133	V_{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	NC	53	DQ19	95	NC	137	DQ55
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V_{CC}	101	DQ49	143	V_{CC}
18	V_{CC}	60	DQ24	102	V_{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	NC	64	NC	106	NC	148	NC
23	V_{SS}	65	DQ25	107	V_{SS}	149	DQ61
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ27	109	NC	151	DQ63
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE0}$	69	DQ28	111	NC	153	DQ64
28	$\overline{CE0}$	70	DQ29	112	$\overline{CE1}$	154	DQ65
29	$\overline{CE2}$	71	DQ30	113	$\overline{CE3}$	155	DQ66
30	$\overline{RE0}$	72	DQ31	114	NC	156	DQ67
31	$\overline{OE0}$	73	V_{CC}	115	NC	157	V_{CC}
32	V_{SS}	74	DQ32	116	V_{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
35	A4	77	NC	119	A5	161	NC
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V_{CC}	82	PD7	124	V_{CC}	166	PD8
41	NC	83	ID0 (V_{SS})	125	NC	167	ID1 (V_{SS})
42	NC	84	V_{CC}	126	B0	168	V_{CC}

Pin Description

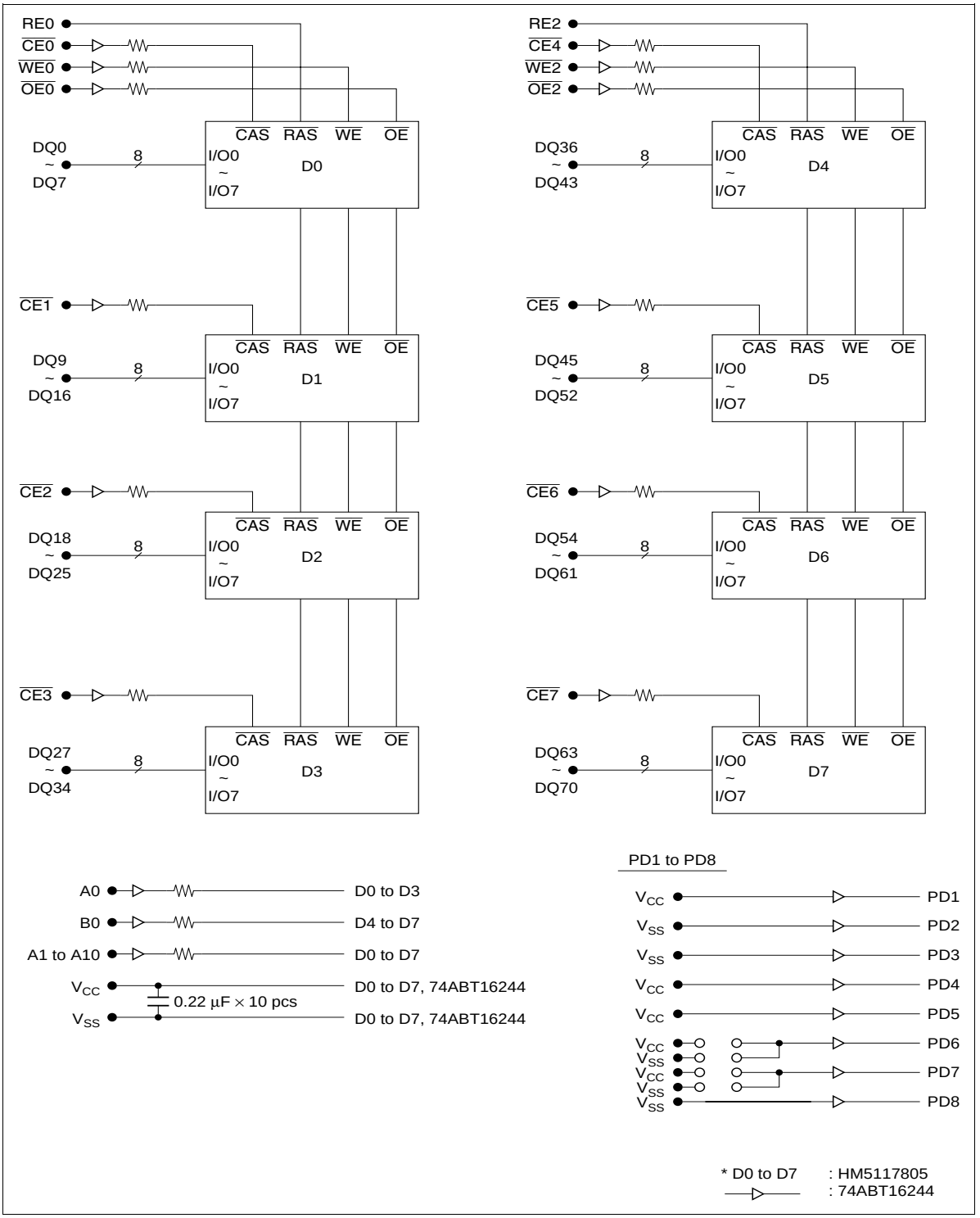
Pin name	Function
A0 to A10, B0	Address input — Row address : A0 to A10, B0 — Column address : A0 to A9, B0 — Refresh address : A0 to A10, B0
DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34, DQ36 to DQ43, DQ45 to DQ52, DQ54 to DQ61, DQ63 to DQ70	Data-in/data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE7}$	Column address strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/Write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence detect enable
NC	No connection

Presence Detect Pin Assignment

		$\overline{\text{PDE}}$ = Low			$\overline{\text{PDE}}$ = High
Pin name	**Pin No.**	**50 ns**	**60 ns**	**70 ns**	**All**
PD1	79	1	1	1	High-Z
PD2	163	0	0	0	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	1	1	1	High-Z
PD6	165	0	1	0	High-Z
PD7	82	0	1	1	High-Z
PD8	166	1	1	1	High-Z

Note: 1: High level (Driver output)
0: Low level (Driver output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	9	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–0.5	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	944	—	864	—	784	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	80	—	80	—	80	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	72	—	72	—	72	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	944	—	864	—	784	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	104	—	104	—	104	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	944	—	864	—	784	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	864	—	784	—	744	mA	t_{HPC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	48	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)[*1, *2, *18, *19]

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	7	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	11	32	14	40	14	47	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	9	20	12	25	12	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	18	—	20	—	23	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	

Read Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	18	—	20	—	23	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	18	—	20	—	23	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	2	—	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	22
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	18	—	20	—	20	ns	13, 22
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	18	—	20	—	20	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	18	—	20	—	23	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	13	—	15	—	15	ns	22
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	18	—	20	—	20	ns	
$\overline{WE}$ to Din delay time	t_{WED}	18	—	20	—	23	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{RAS}$ next $\overline{CAS}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	7	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	12	—	15	—	18	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7	—	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	12	—	15	—	18	—	ns	15

Read-Modify-Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	111	—	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	57	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	7	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	7	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

EDO Page Mode Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	33	—	40	—	45	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	33	—	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time refferd $\overline{OE}$	t_{COL}	7	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPRWC}	57	—	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	54	—	62	—	ns	14

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max)- t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

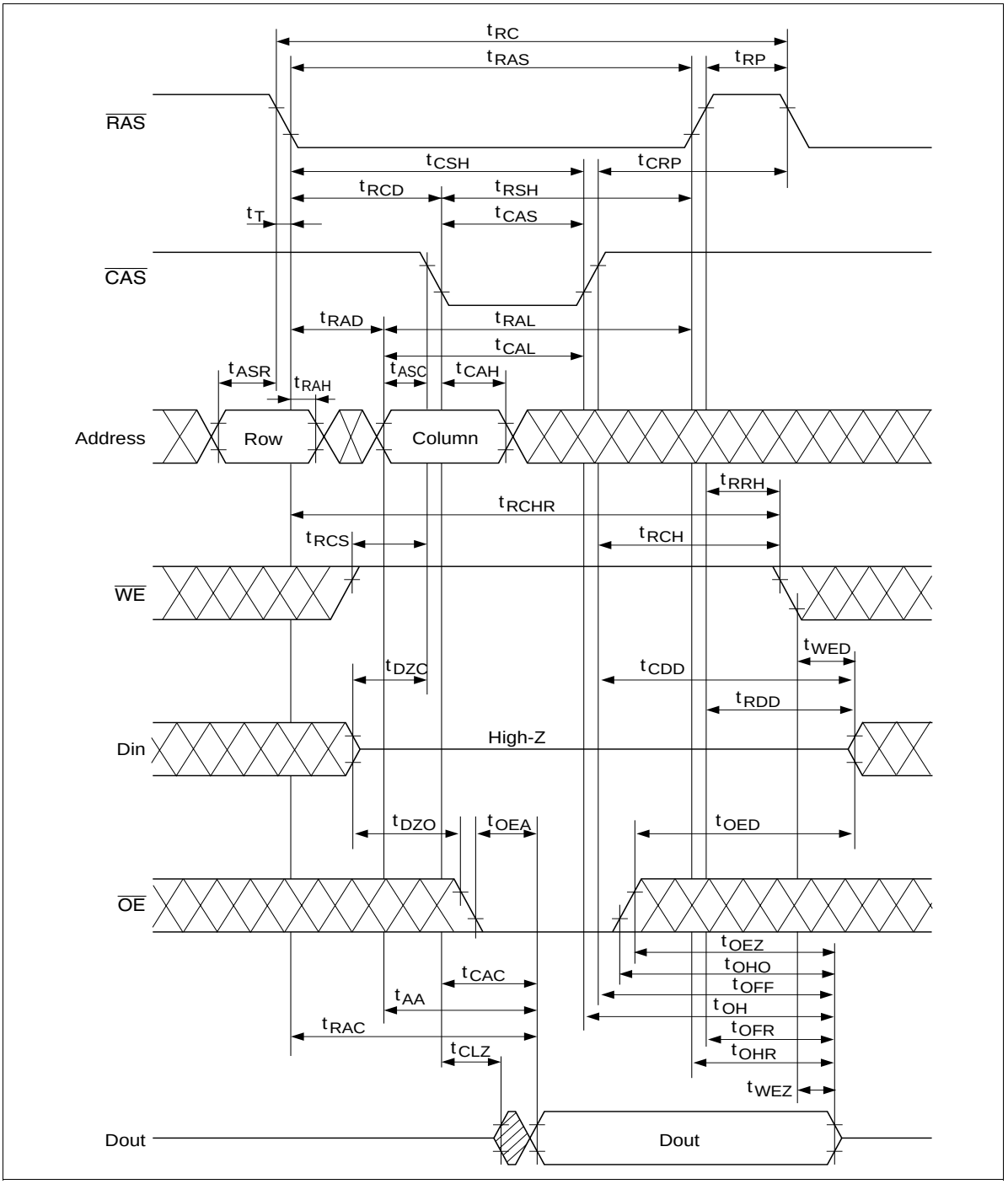
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics onry; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); $t_{OEH} < t_{OEH}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
22. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
23. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

    ///////: Invalid Dout

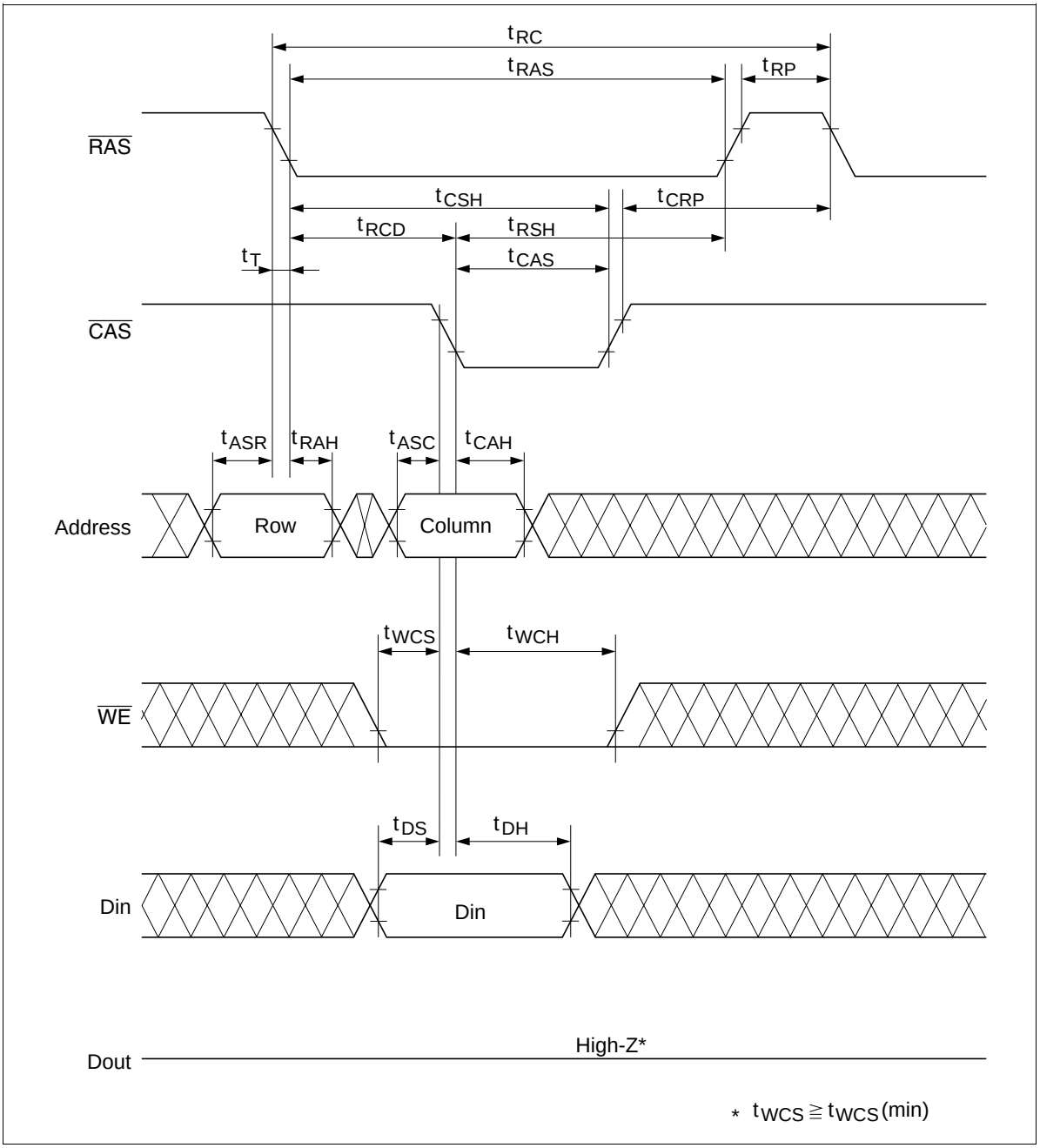
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[23]

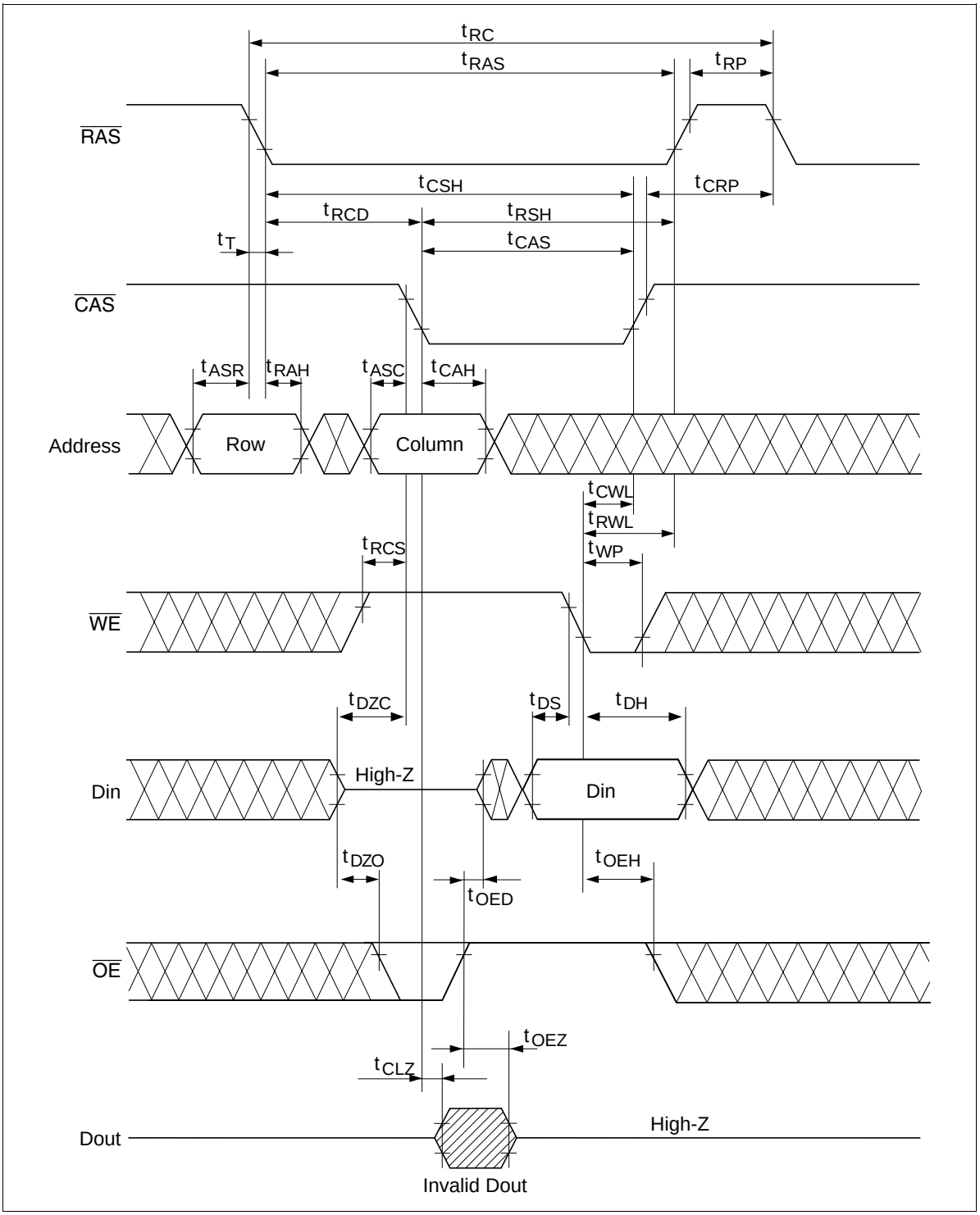
Read Cycle



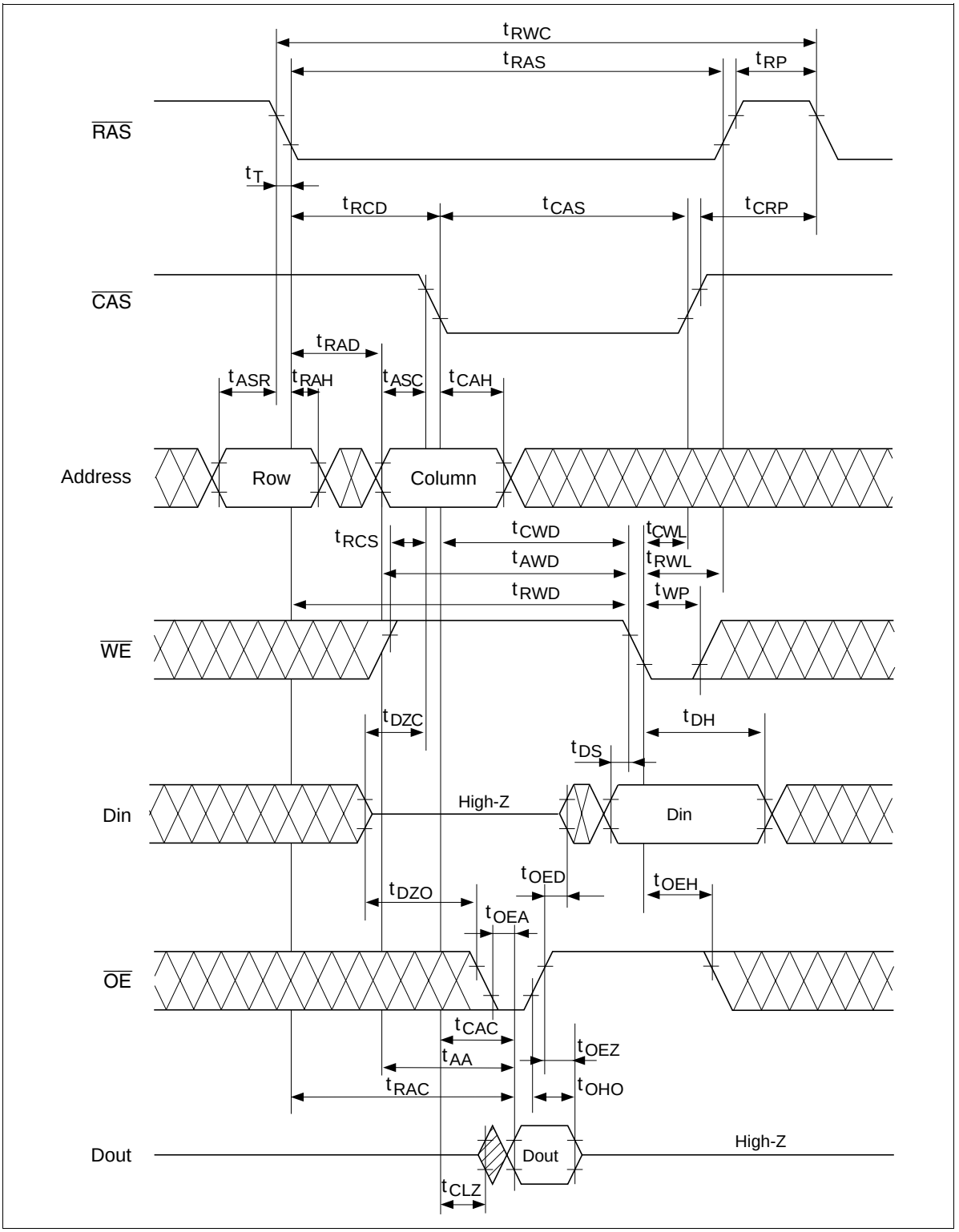
Early Write Cycle



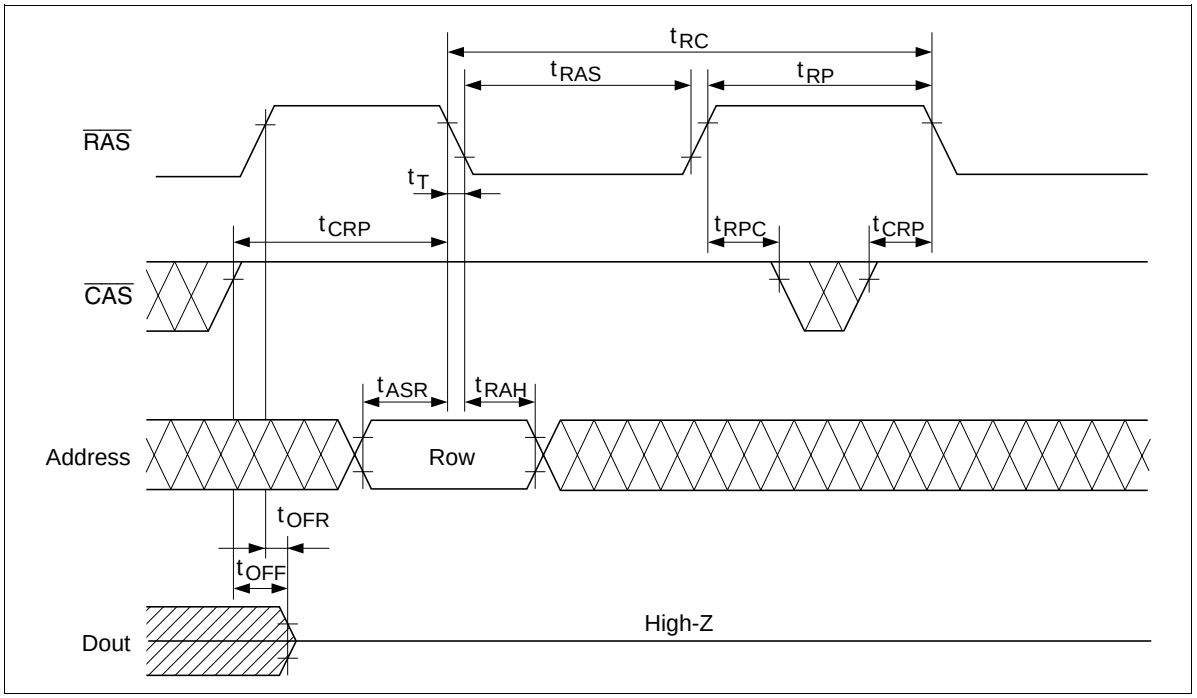
Delayed Write Cycle*[18]



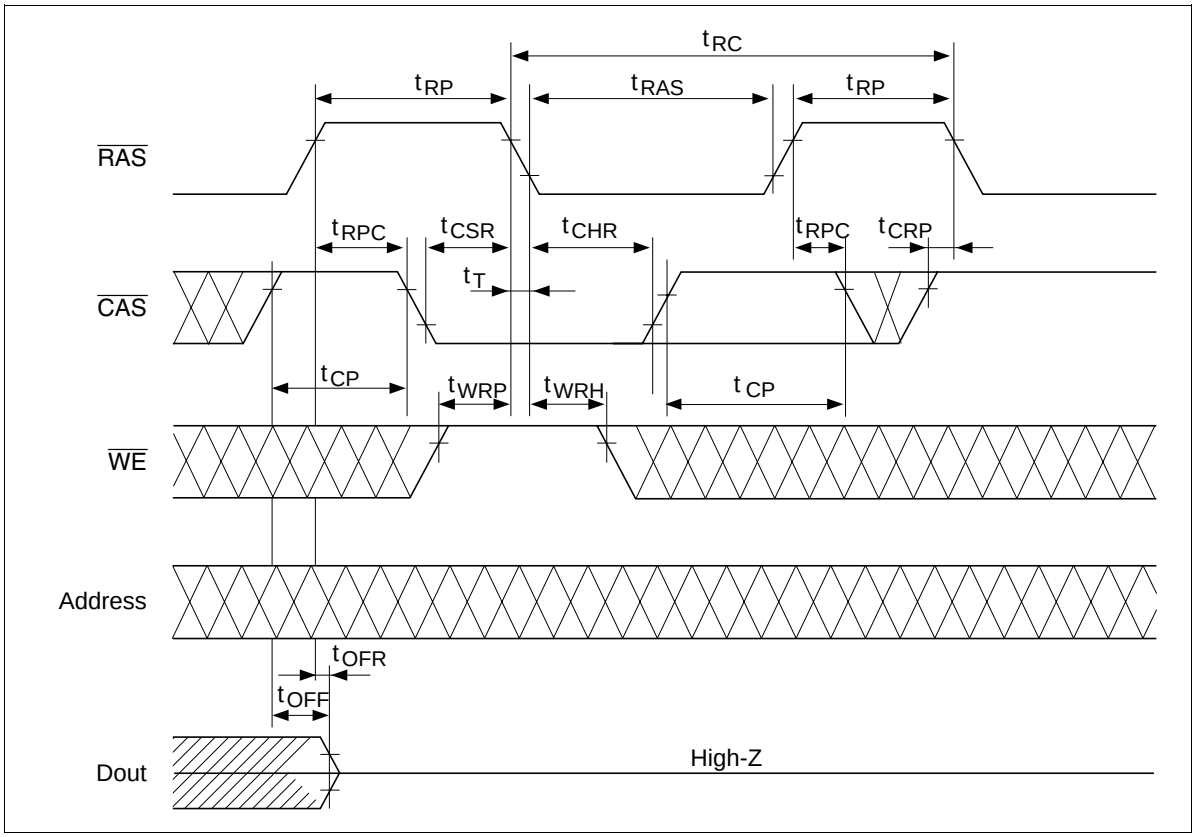
Read-Modify-Write Cycle*[18]



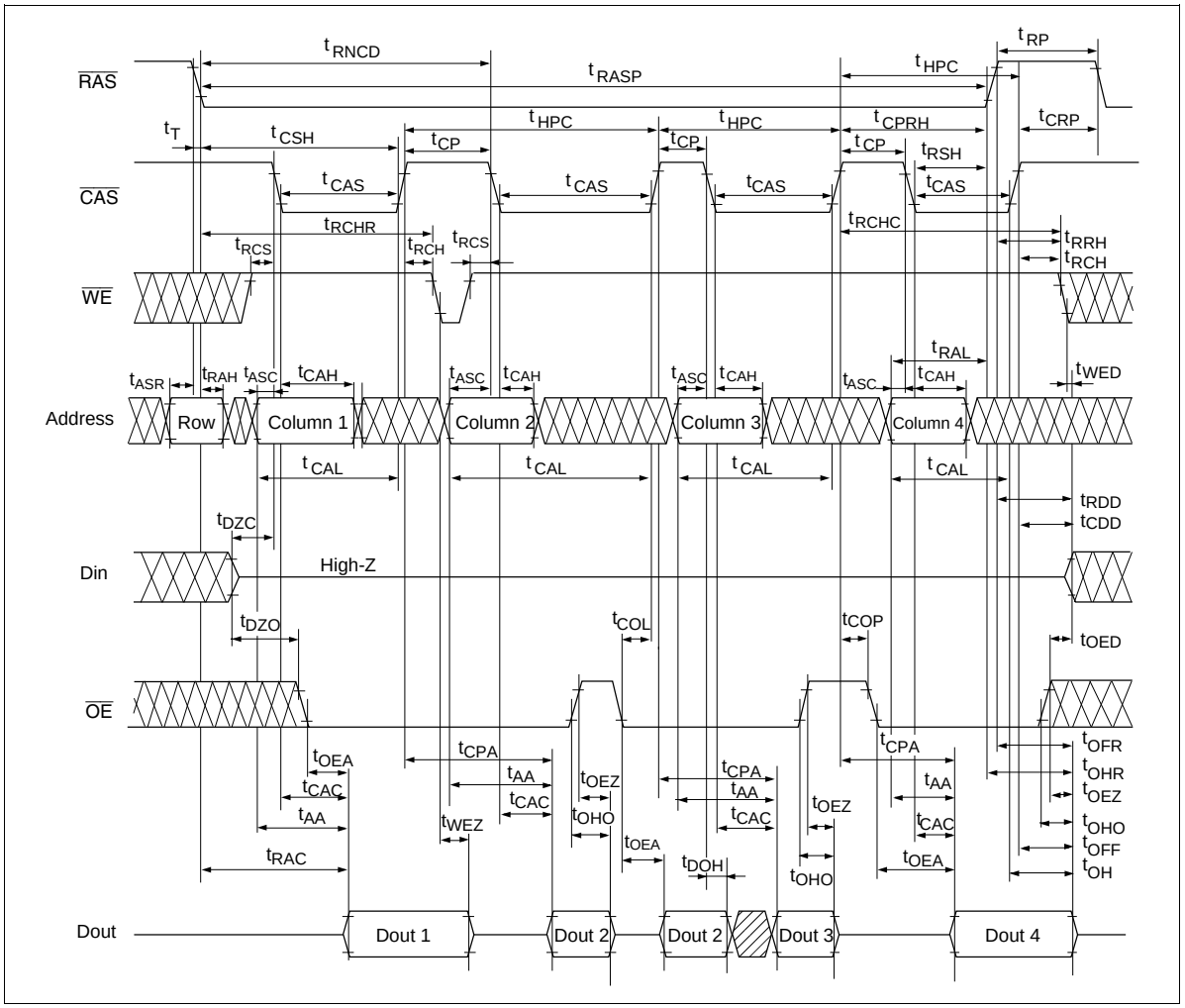
$\overline{\text{RAS}}$-Only Refresh Cycle



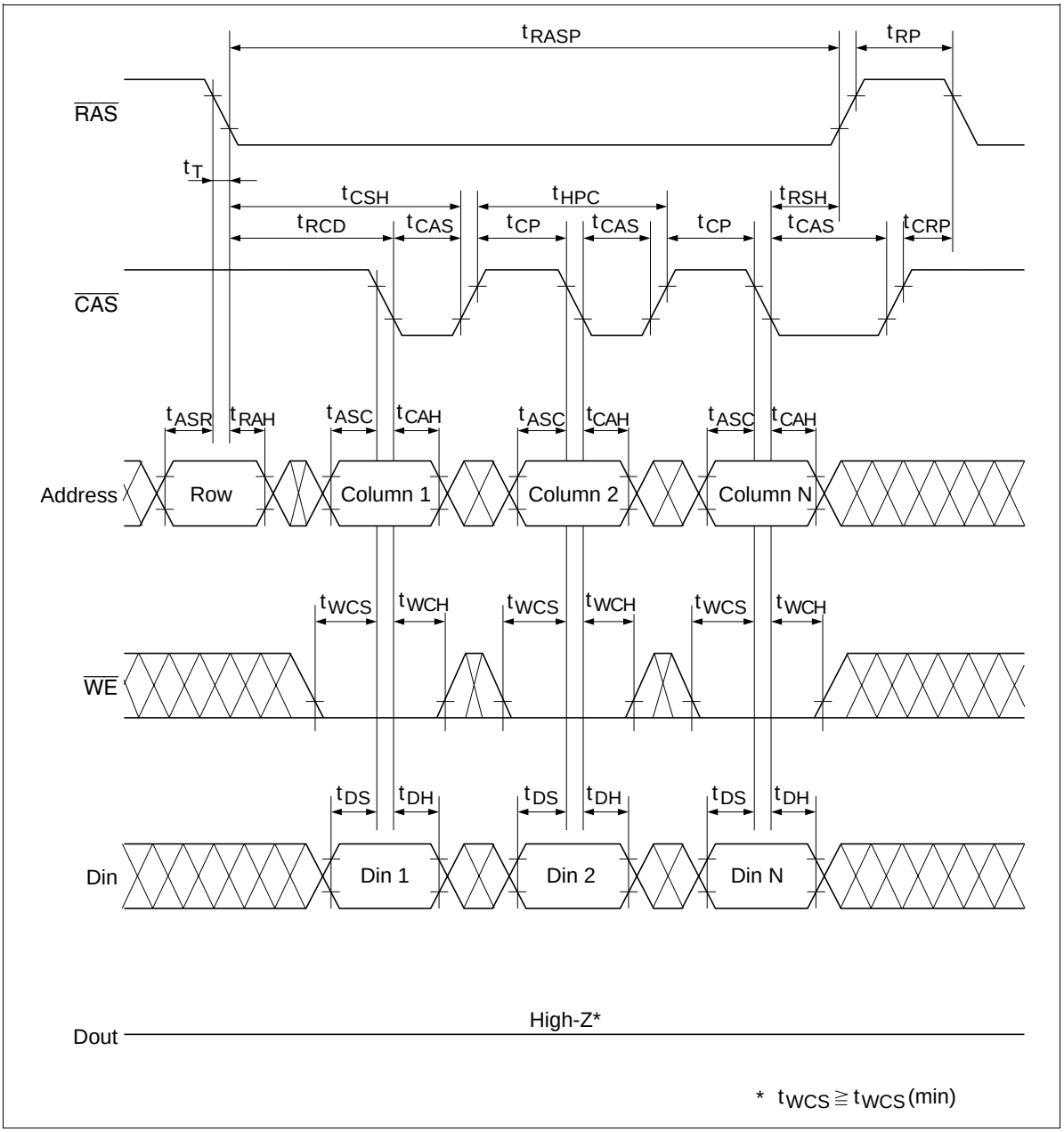
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



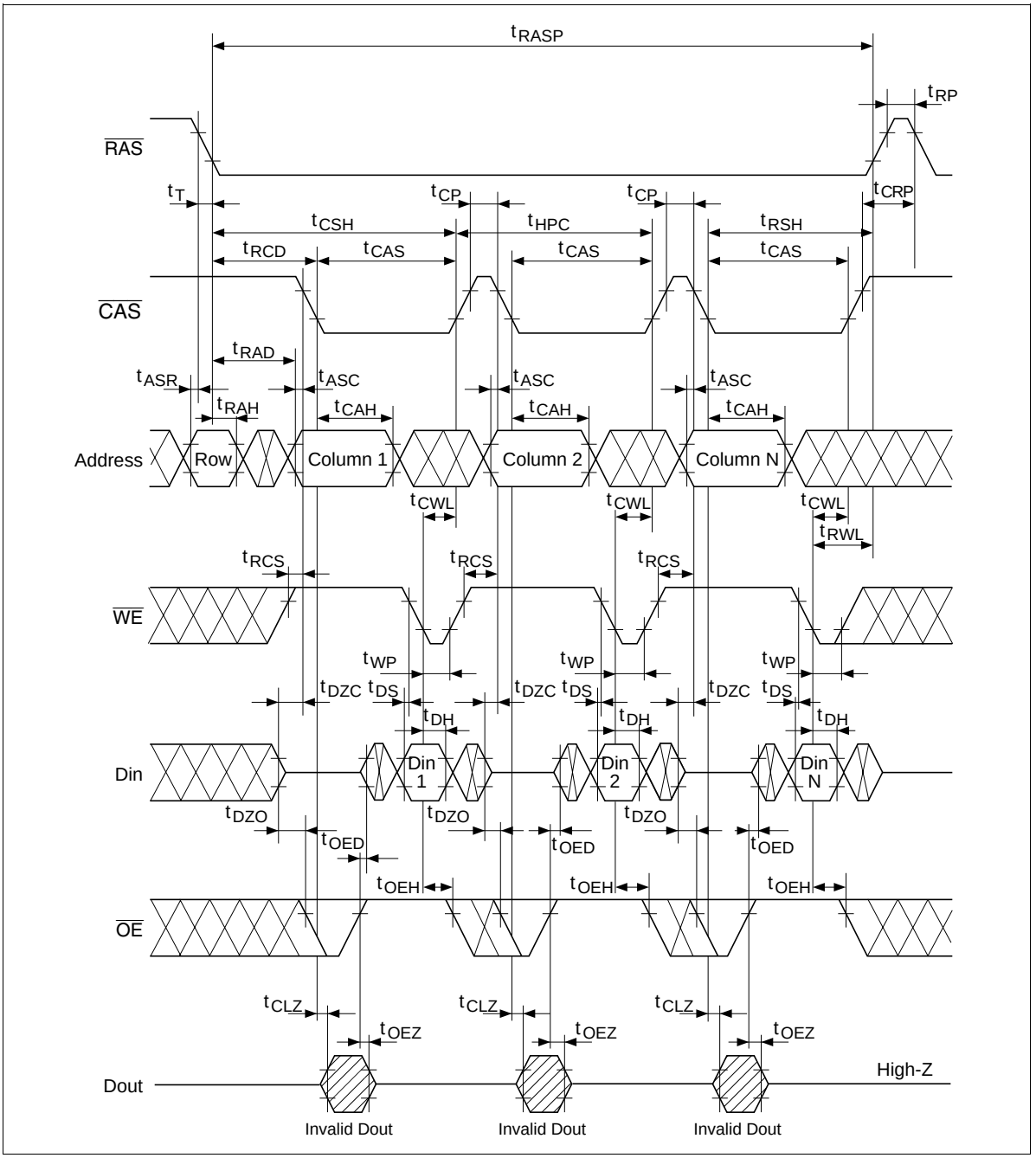
EDO Page Mode Read Cycle



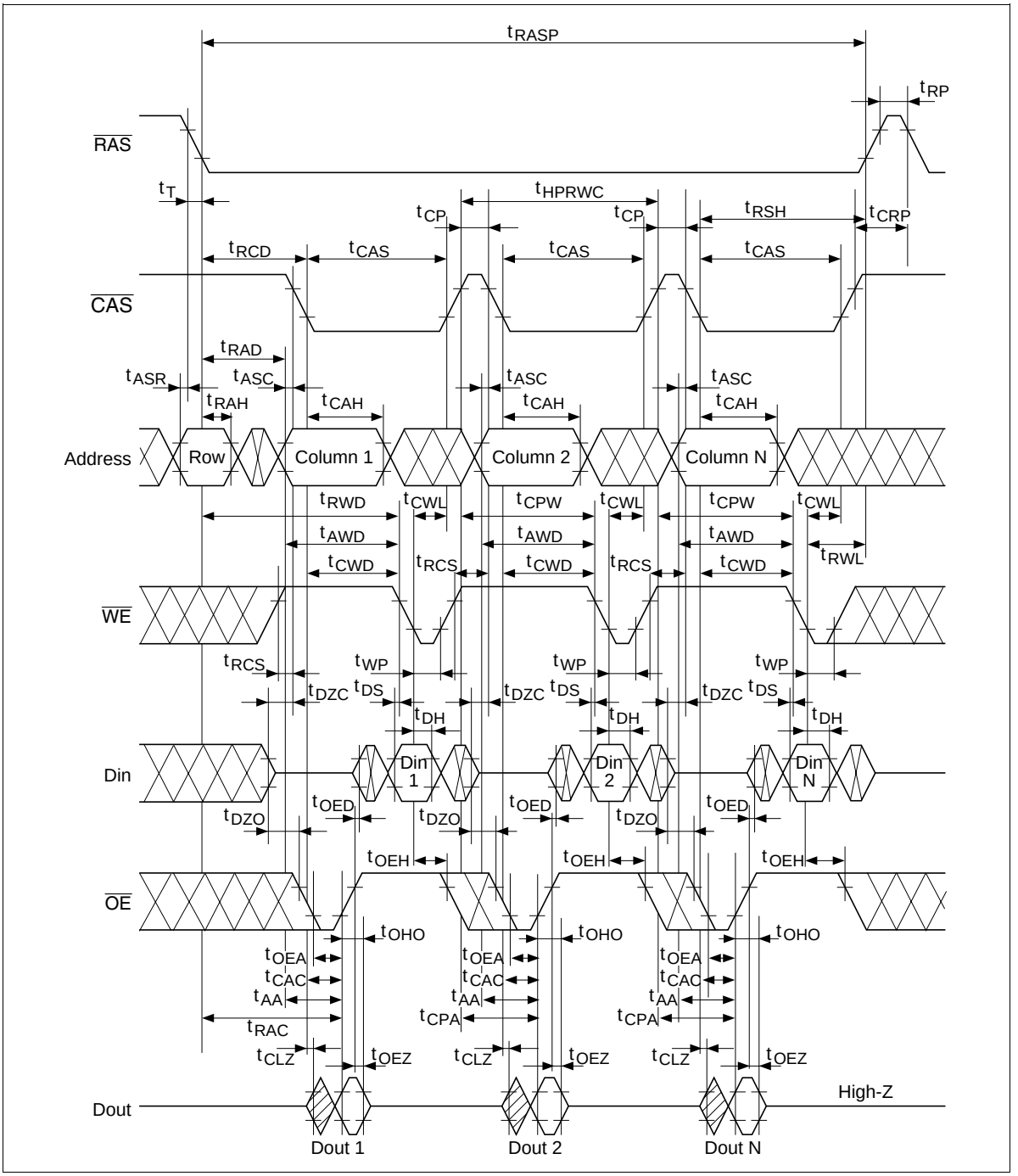
EDO Page Mode Early Write Cycle



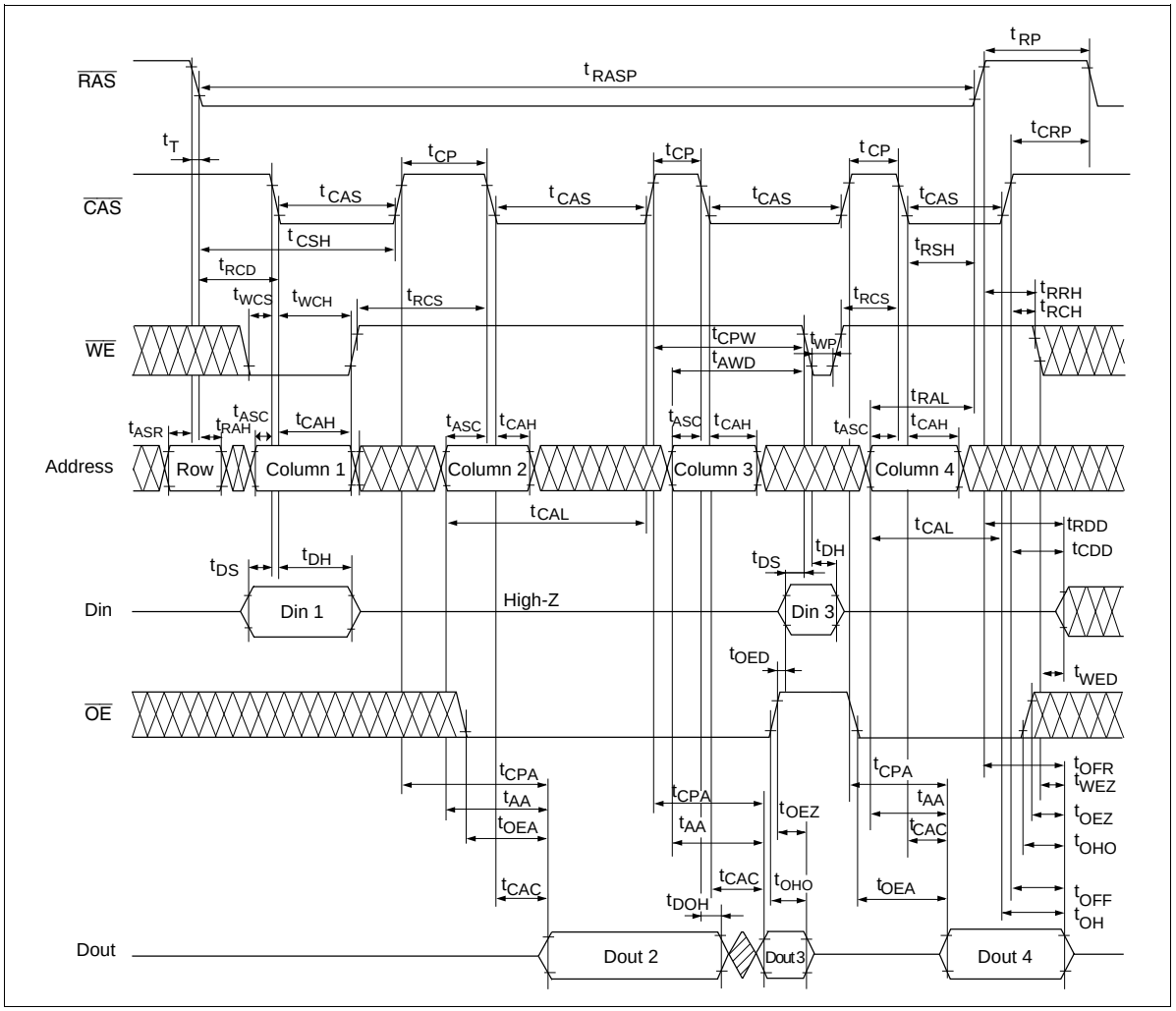
EDO Page Mode Delayed Write Cycle*[18]



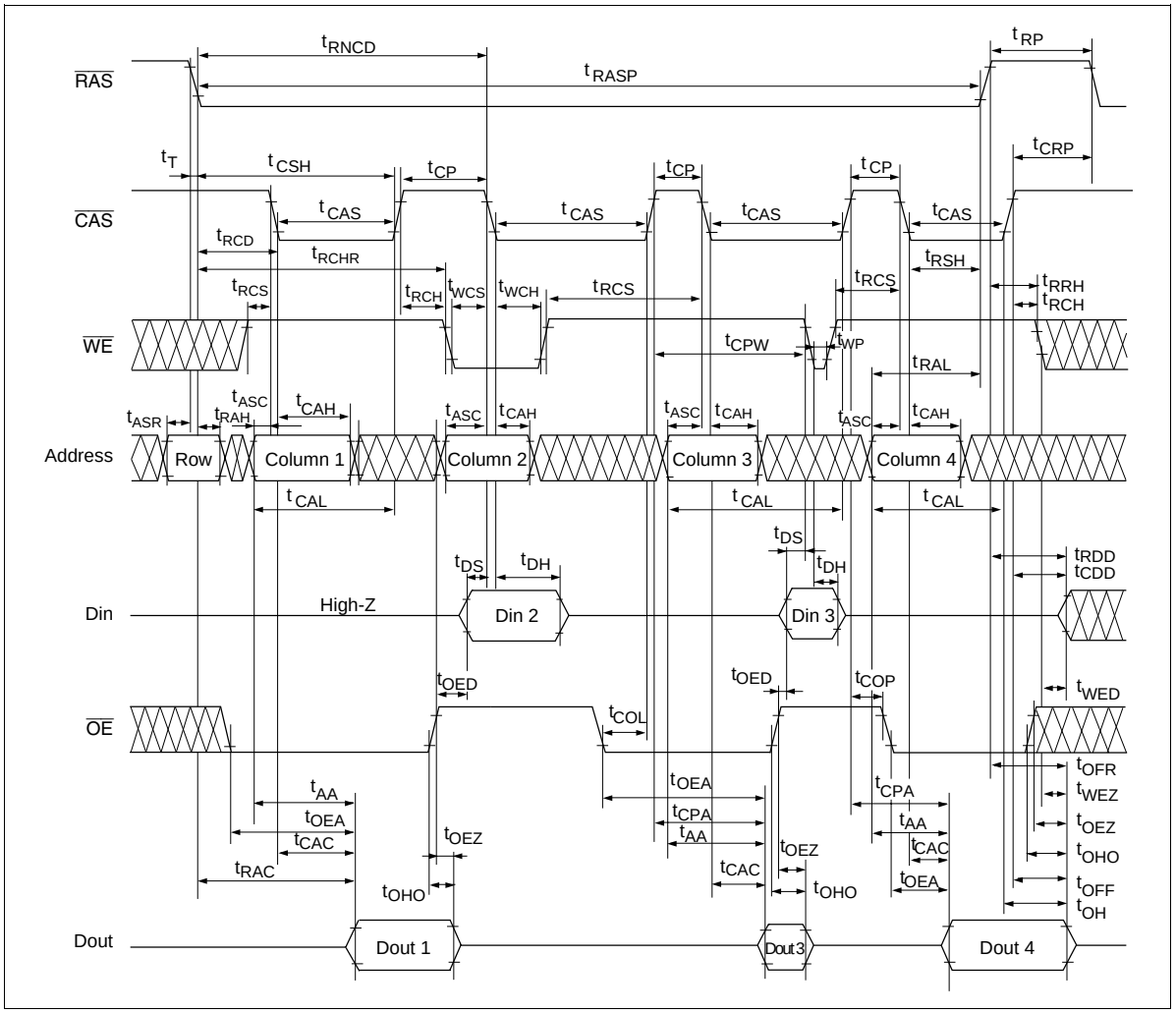
EDO Page Mode Read-Modify-Write Cycle*[18]



EDO Page Mode Mix Cycle (1)

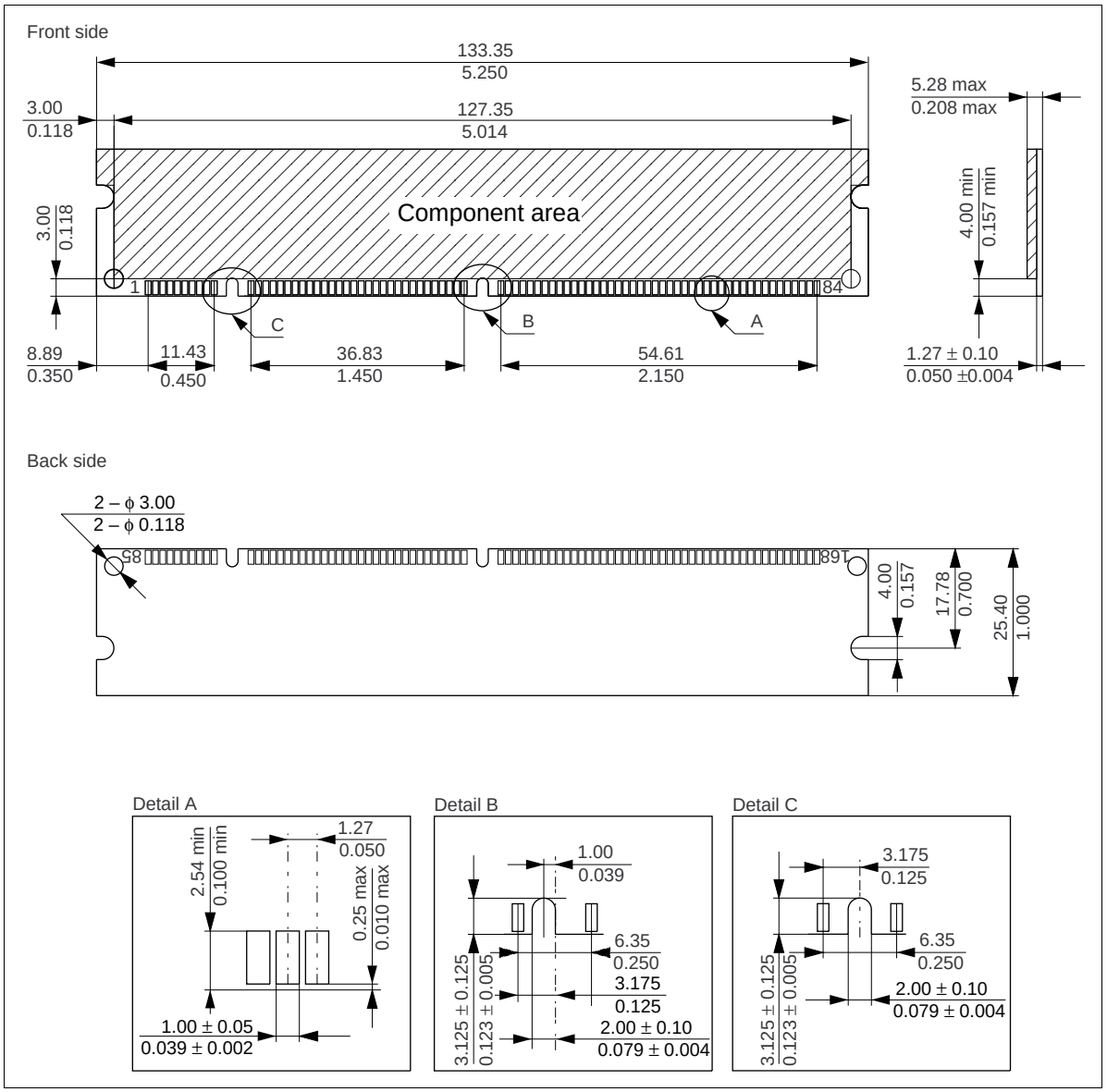


EDO Page Mode Mix Cycle (2)



Physical Outline

Unit: mm/inch



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Jan. 27, 1997	Initial issue		