
HB56UW865DB Series

8388608-word $\times$ 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-665A (Z)

Rev. 1.0

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Description

The HB56UW865DB Series is a 8 M $\times$ 64 Dynamic RAM Small Outline Dual In-line Memory Module (S. O. DIMM), mounted 8 pieces of 64-Mbit DRAM (HM5165805ATT/ALTT) sealed in TSOP package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW865DB Series offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW865DB Series is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56UW865DB Series makes high density mounting possible without surface mount technology. The HB56UW865DB Series provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the its module board.

Features

- 144-pin Zig Zag Dual tabs socket type
 - Outline: 67.60 mm (Length) $\times$ 25.40 mm (Height) $\times$ 3.80 mm (Thickness)
 - Lead pitch : 0.80 mm
- Single 3.3 V (± 0.3 V)
- High speed
 - Access time: $t_{\text{RAC}} = 60$ ns/70 ns (max)
 - Access time: $t_{\text{CAC}} = 15$ ns/18 ns (max)
- Low power dissipation
 - Active mode: 4.76 W/4.18W (max)
 - Standby mode (TTL): 57.6 mW (max)
 - Standby mode (CMOS) : 28.8 mW (max)
: 5.8 mW (max) (L-version)
- JEDEC standard outline S. O. DIMM
- EDO page mode capability
- 4096 refresh cycles: 64 ms
128 ms (L-version)

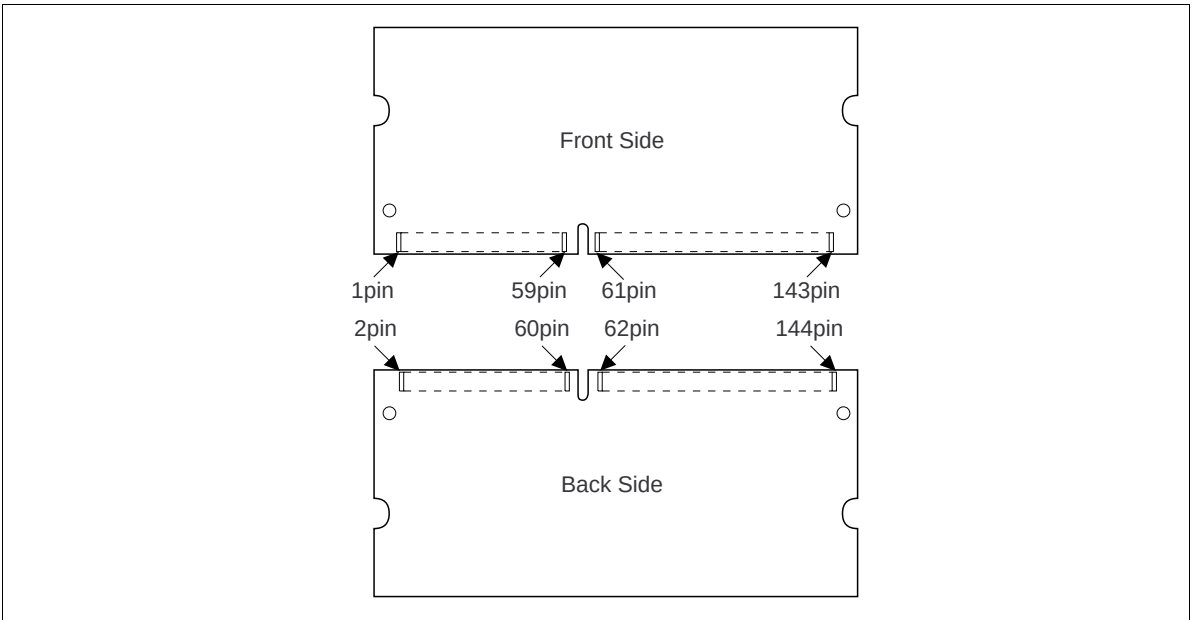
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- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW865DB-6A	60 ns	144-pin small outline DIMM	Gold
HB56UW865DB-7A	70 ns		
HB56UW865DB-6AL	60 ns		
HB56UW865DB-7AL	70 ns		

Pin Arrangement



Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V_{SS}	73	$\overline{\text{OE}}$	2	V_{SS}	74	NC
3	DQ0	75	V_{SS}	4	DQ32	76	V_{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V_{CC}	10	DQ35	82	V_{CC}

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Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
11	V _{CC}	83	DQ16	12	V _{CC}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V _{SS}	20	DQ39	92	V _{SS}
21	V _{SS}	93	DQ20	22	V _{SS}	94	DQ52
23	$\overline{\text{CE0}}$	95	DQ21	24	$\overline{\text{CE4}}$	96	DQ53
25	$\overline{\text{CE1}}$	97	DQ22	26	$\overline{\text{CE5}}$	98	DQ54
27	V _{CC}	99	DQ23	28	V _{CC}	100	DQ55
29	A0	101	V _{CC}	30	A3	102	V _{CC}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11
35	V _{SS}	107	V _{SS}	36	V _{SS}	108	V _{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10	40	DQ41	112	NC
41	DQ10	113	V _{CC}	42	DQ42	114	V _{CC}
43	DQ11	115	$\overline{\text{CE2}}$	44	DQ43	116	$\overline{\text{CE6}}$
45	V _{CC}	117	$\overline{\text{CE3}}$	46	V _{CC}	118	$\overline{\text{CE7}}$
47	DQ12	119	V _{SS}	48	DQ44	120	V _{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V _{SS}	127	DQ27	56	V _{SS}	128	DQ59
57	NC	129	V _{CC}	58	NC	130	V _{CC}
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	V _{CC}	135	DQ30	64	V _{CC}	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63
67	$\overline{\text{WE}}$	139	V _{SS}	68	NC	140	V _{SS}
69	$\overline{\text{RE0}}$	141	SDA	70	NC	142	SCL
71	NC	143	V _{CC}	72	NC	144	V _{CC}

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Pin Description

Pin name	Function
A0 to A11	Address input Row address A0 to A11 Column address A0 to A10 Refresh address A0 to A11
DQ0 to DQ63	Data input/output
$\overline{RE}0$	Row address strobe ($\overline{RAS}$)
$\overline{CE}0$ to $\overline{CE}7$	Column address strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
SDA	Serial data for PD
SCL	Serial clock for PD
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Serial PD Matrix*¹

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	0	1	0	02	EDO
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	1	0B	11
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	0	0	0	0	40	64 bits
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	$\overline{\text{RAS}}$ access time -6A/-6AL	0	0	1	1	1	1	0	0	3C	$t_{\text{RAC}} = 60 \text{ ns}$
	$\overline{\text{RAS}}$ access time -7A/-7AL	0	1	0	0	0	1	1	0	46	$t_{\text{RAC}} = 70 \text{ ns}$
10	$\overline{\text{CAS}}$ access time -6A/-6AL	0	0	0	0	1	1	1	1	0F	$t_{\text{CAC}} = 15 \text{ ns}$
	$\overline{\text{CAS}}$ access time -7A/-7AL	0	0	0	1	0	0	1	0	12	$t_{\text{CAC}} = 18 \text{ ns}$
s11	Module configuration type	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type -6A/-7A	0	0	0	0	0	0	0	0	00	Normal (15.625 μs)
	Refresh rate/type -6AL/-7AL (L-version)	1	0	0	0	0	0	1	1	83	Self refresh (31.3 μs)
13	DRAM width	0	0	0	0	1	0	0	0	08	8M $\times$ 8
14	Error checking DRAM data width	0	0	0	0	0	0	0	0	00	
15 to 31	Reserved for future offerings	0	0	0	0	0	0	0	0	00	
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future offerings
62	SPD revision	0	0	0	0	0	0	0	1	01	Rev. 1
63	Checksum for bytes 0 to 62 -6A	0	0	1	1	0	1	1	1	37	
	Checksum for bytes 0 to 62 -7A	0	1	0	0	0	1	0	0	44	
	Checksum for bytes 0 to 62 -6AL	1	0	1	1	1	0	1	0	BA	
	Checksum for bytes 0 to 62 -7AL	1	1	0	0	0	1	1	1	C7	

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Serial PD Matrix*1 (cont)

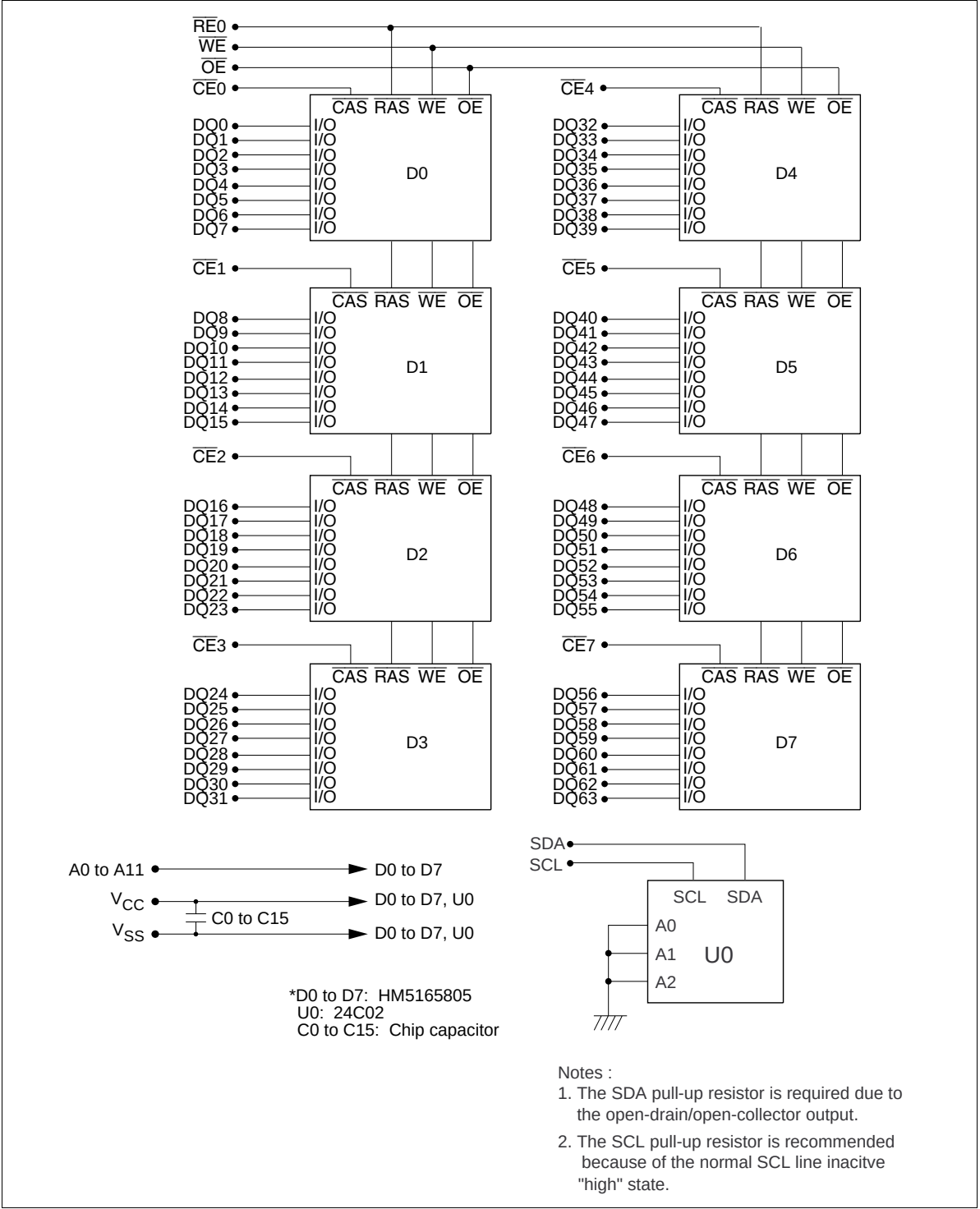
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	Hitachi
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	×	*2 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
77	Manufacturer's part number	0	1	0	1	0	1	0	1	55	U
78	Manufacturer's part number	0	1	0	1	0	1	1	1	57	W
79	Manufacturer's part number	0	0	1	1	1	0	0	0	38	8
80	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
82	Manufacturer's part number	0	1	0	0	0	1	0	0	44	D
83	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
84	Manufacturer's part number	0	1	0	1	1	1	1	1	5F	—
85	Manufacturer's part number -6A/-6AL	0	0	1	1	0	1	1	0	36	6
	Manufacturer's part number -7A/-7AL	0	0	1	1	0	1	1	1	37	7
86	Manufacturer's part number	0	1	0	0	0	0	0	1	41	A
87	Manufacturer's part number -6A/-7A	0	0	1	0	0	0	0	0	20	(Space)
	Manufacturer's part number -6AL/-7AL (L-version)	0	1	0	0	1	1	0	0	4C	L
88 to 90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date (year code)	×	×	×	×	×	×	×	×	×	Year code*3 (binary)
94	Manufacturing date (week code)	×	×	×	×	×	×	×	×	×	Week code*4 (binary)

Serial PD Matrix*¹ (cont)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
95 to 98	Assembly serial number	* ⁵									
99 to 125	Manufacturer specific data	* ⁶									
126	Reserved	0	0	0	0	0	0	0	0	00	
127	Reserved	0	0	0	0	0	0	0	0	00	

- Notes:
- 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High”
 - 2. Byte 72 is manufacturing location code. (ex: in case of Japan, byte 72 is 4Ah. 4Ah shows “J” on ASCII code.)
 - 3. Byte 93 (Manufacturing date-year code) ex: 61h shows year ‘97. 62h shows year ‘98.
 - 4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11. 24h shows week 36.
 - 5. Byte 95 through 98 are assembly serial number.
 - 6. All bits of byte 99 through 125 are not defined (“1” or “0”).

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	8.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

- Notes: 1. All voltage referred to V_{SS} .
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

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Parameter	Symbol	60 ns		70 ns		Unit	Test conditions
		Min	Max	Min	Max		
Operating current* ¹ , * ²	I _{CC1}	—	1320	—	1160	mA	t _{RC} = min
Standby current	I _{CC2}	—	16	—	16	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	8	—	8	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	1.6	—	1.6	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	1320	—	1160	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	40	—	40	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	1120	—	960	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	1000	—	880	mA	t _{HPC} = min
Battery backup current* ⁴ (Standby with CBR refresh) (L-version)	I _{CC10}	—	5.2	—	5.2	mA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	4	—	4	mA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ V _{CC} Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

- Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less within one page mode cycle t_{HPC}.
4. V_{IH} ≥ V_{CC} − 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	60	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I2}	—	76	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I3}	—	22	pF	1
I/O capacitance (DQ)	C _{I/O}	—	17	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = \text{V}_{\text{IH}}$ to disable Dout.

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AC Characteristics (Ta = 0 to +70°C, VCC = 3.3 V ± 0.3 V, VSS = 0 V) *1, *2, *3, *18

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: VIL = 0 V, VIH = 3 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + CL (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	104	—	124	—	ns	
RAS precharge time	t _{RP}	40	—	50	—	ns	
CAS precharge time	t _{CP}	10	—	13	—	ns	
RAS pulse width	t _{RAS}	60	10000	70	10000	ns	
CAS pulse width	t _{CAS}	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	ns	
RAS to CAS delay time	t _{RCD}	20	45	20	52	ns	3
RAS to column address delay time	t _{RAD}	15	30	15	35	ns	4
RAS hold time	t _{RSH}	15	—	18	—	ns	
CAS hold time	t _{CSH}	48	—	58	—	ns	20
CAS to RAS precharge time	t _{CRP}	5	—	5	—	ns	
OE to Din delay time	t _{OED}	15	—	18	—	ns	5
OE delay time from Din	t _{DZO}	0	—	0	—	ns	6
CAS delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	ns	7

Read Cycle

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 16
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 16
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13, 19
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	19
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	

Write Cycle

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	14
Write command hold time	t _{WCH}	10	—	13	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	10	—	13	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	10	—	13	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	
Data-in hold time	t _{DH}	10	—	13	—	ns	

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Read-Modify-Write Cycle

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	149	—	175	—	ns	
RAS to $\overline{WE}$ delay time	t _{RWD}	78	—	91	—	ns	14
CAS to $\overline{WE}$ delay time	t _{CWD}	33	—	39	—	ns	14
Column address to $\overline{WE}$ delay time	t _{AWD}	48	—	56	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t _{OEH}	15	—	18	—	ns	

Refresh Cycle

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{\text{WE}}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{\text{WE}}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	0	—	0	—	ns	

EDO Page Mode Cycle

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	25	—	30	—	ns	18
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	ns	15
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	35	—	40	ns	9, 16
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	35	—	40	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	ns	9, 16
$\overline{\text{CAS}}$ hold time referred $\overline{\text{OE}}$	t _{COL}	10	—	13	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	t _{COP}	10	—	10	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHC}	35	—	40	—	ns	
Write pulse width during $\overline{\text{CAS}}$ precharge	t _{WPE}	10	—	10	—	ns	
$\overline{\text{OE}}$ precharge time	t _{OEP}	10	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HB56UW865DB					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode read- modify-write cycle time	t _{HPRWC}	68	—	79	—	ns	
WE delay time from CAS precharge	t _{CPW}	54	—	62	—	ns	14

Refresh

Parameter	Symbol	Max	Unit	Notes
Refresh period	t _{REF}	64	ms	4096 cycles
Refresh period (L-version)	t _{REF}	128	ms	4096 cycles

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Self Refresh Mode (L-version)

HB56UW865DB							
Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{\text{RAS}}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	μs	22
$\overline{\text{RAS}}$ precharge time (self refresh)	t_{RPS}	110	—	130	—	ns	22
CAS hold time (self refresh)	t_{CHS}	−50	—	−50	—	ns	

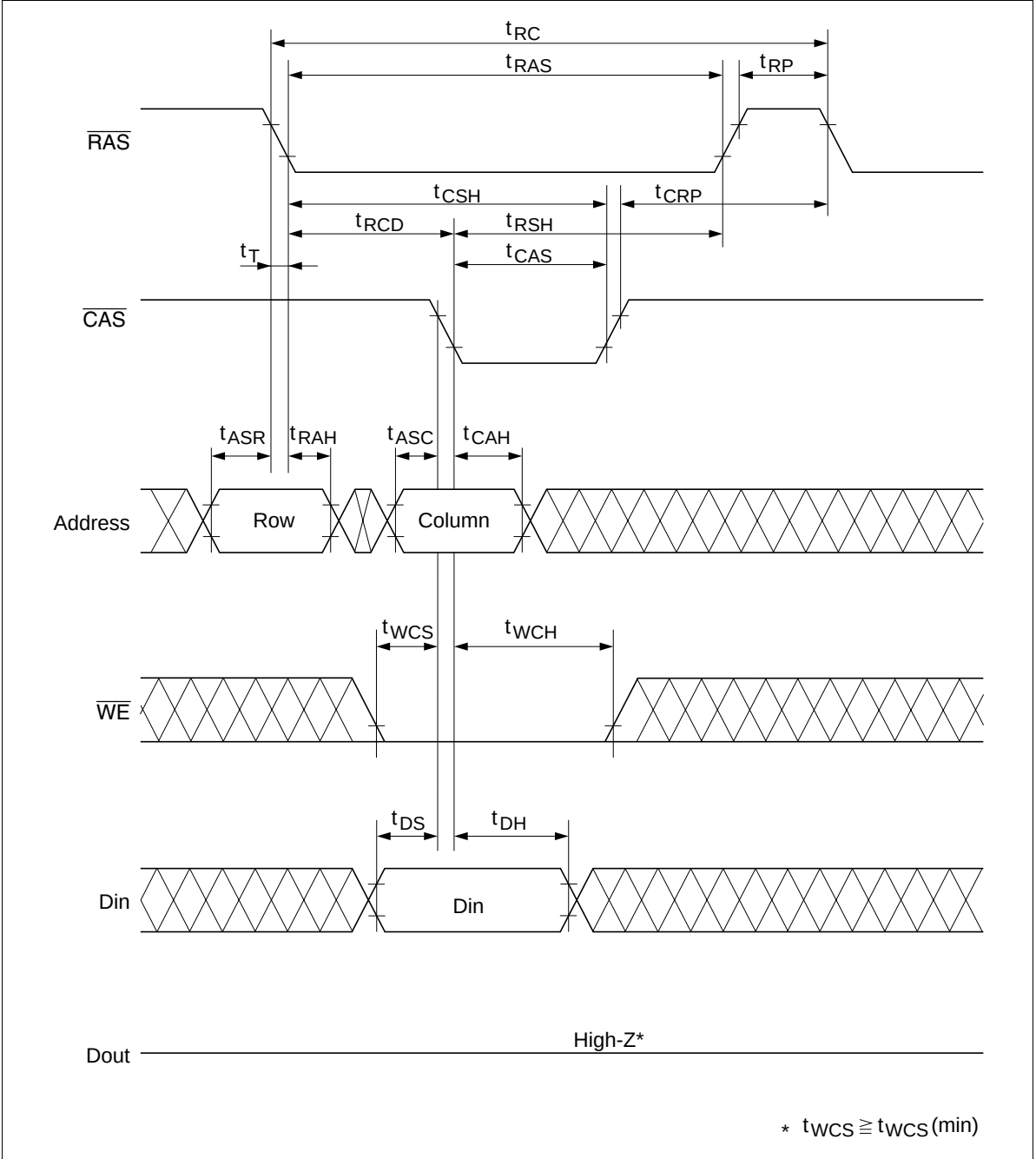
- Notes:
1. AC measurements assume $t_r = 2 \text{ ns}$.
 2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh).
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 16. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 17. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 19. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2 t_r$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
 20. Output is disable after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.
 21. t_{CSH} (min) can be achieved when $t_{\text{RCD}} \leq t_{\text{CSH}}$ (min) $- t_{\text{CAS}}$ (min).

- 22. Please do not use t_{RASS} timing, $10\ \mu\text{s} \leq t_{\text{RASS}} \leq 100\ \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} \geq 100\ \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .
- 23. CBR burst refresh or 4096 cycles of distributed CBR refresh with $15.6\ \mu\text{s}$ interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
- 24. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
- 25. XXX: H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)

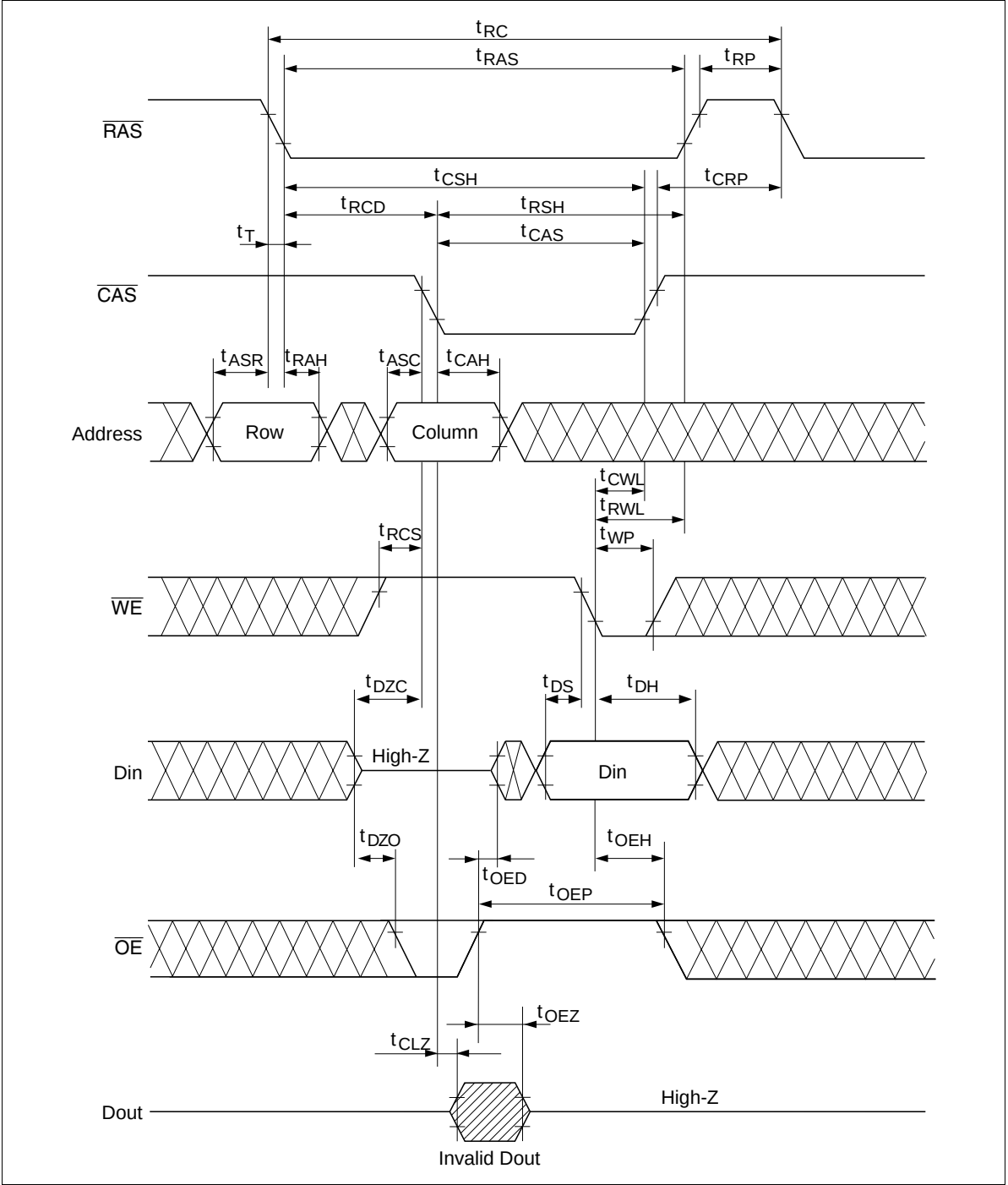
///////: Invalid Dout

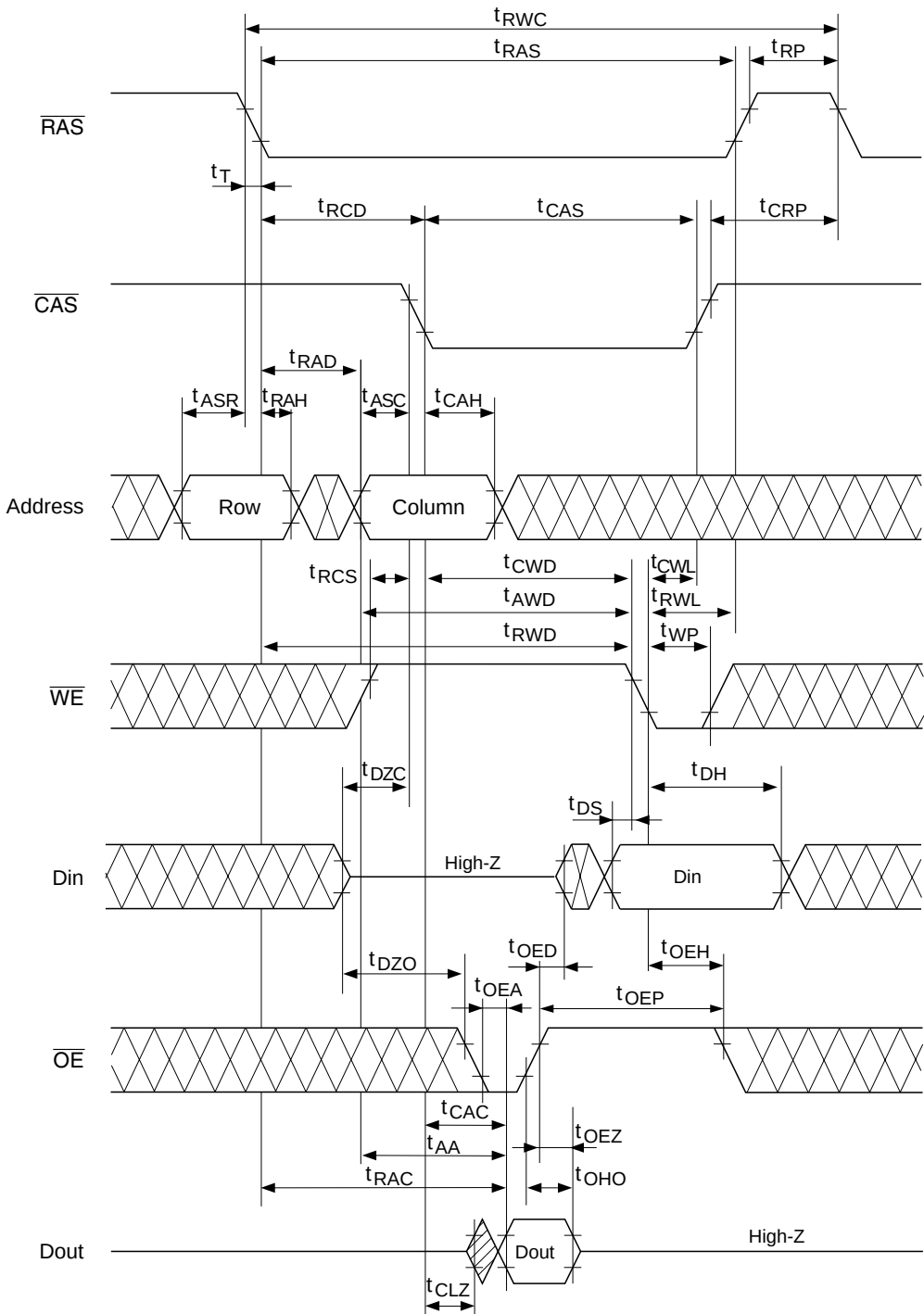
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Early Write Cycle

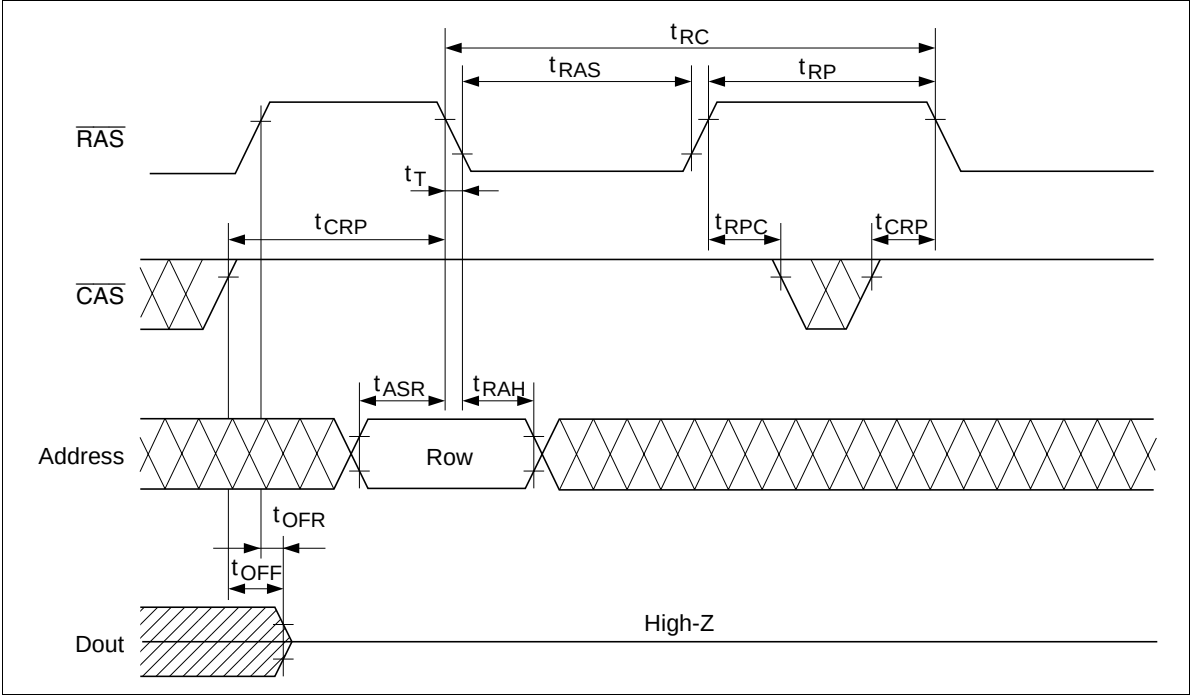


Delayed Write Cycle*18

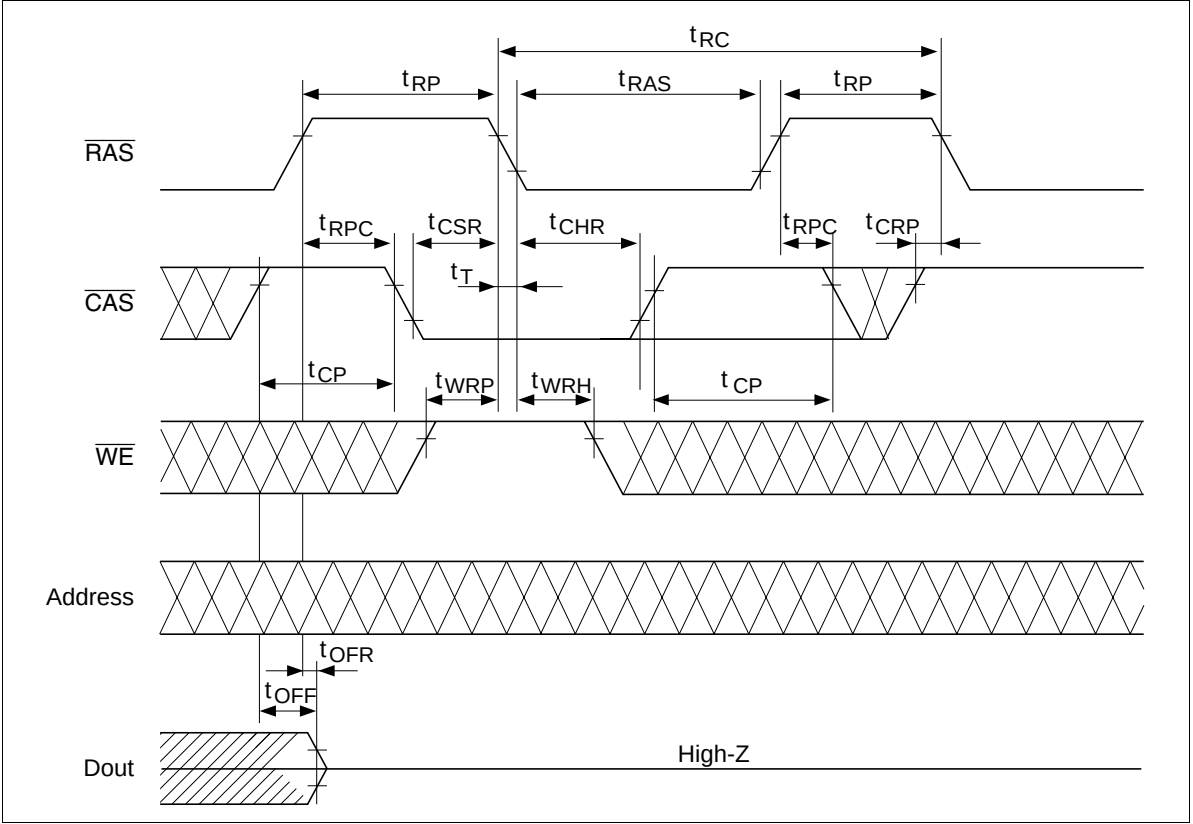




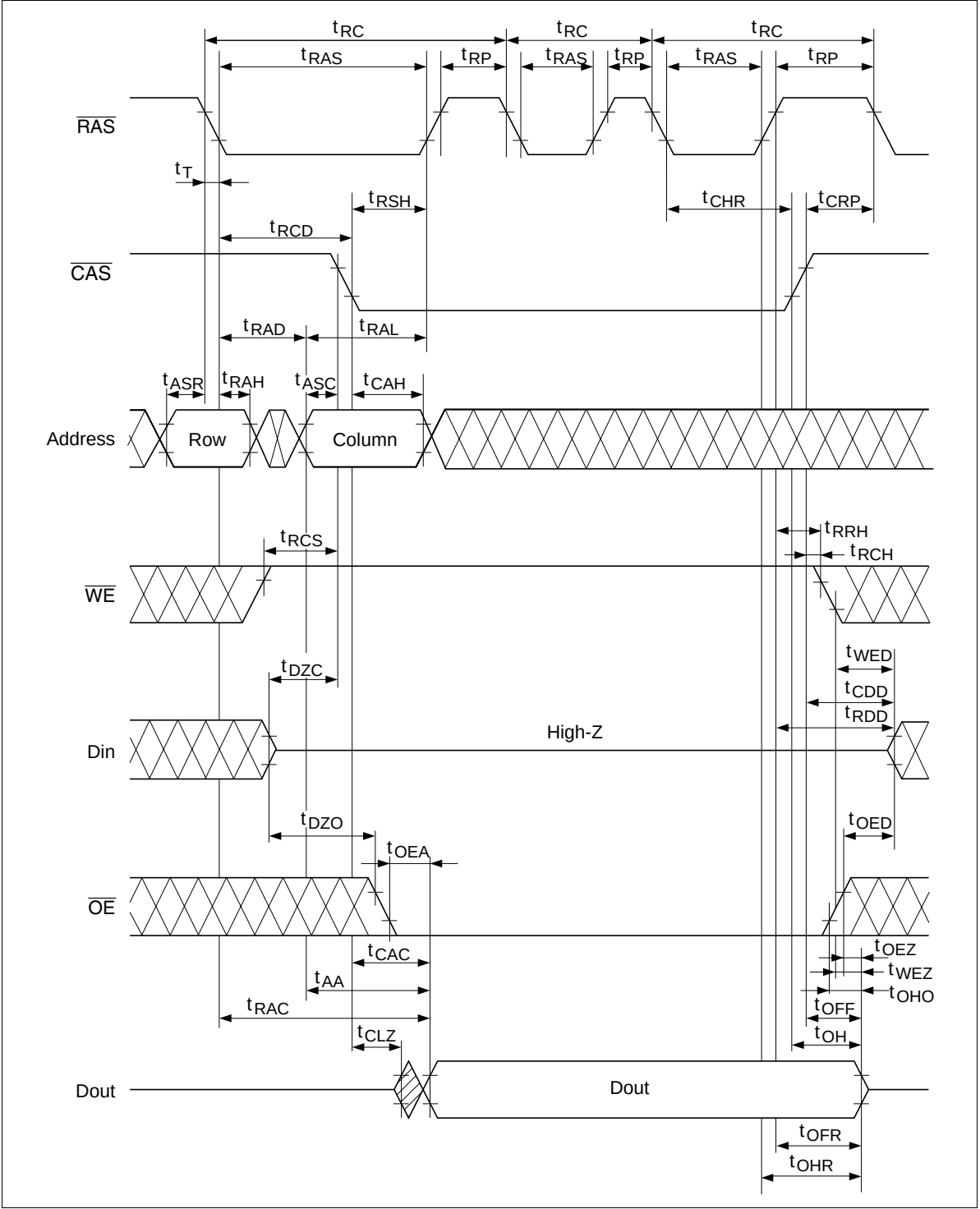
RAS-Only Refresh Cycle



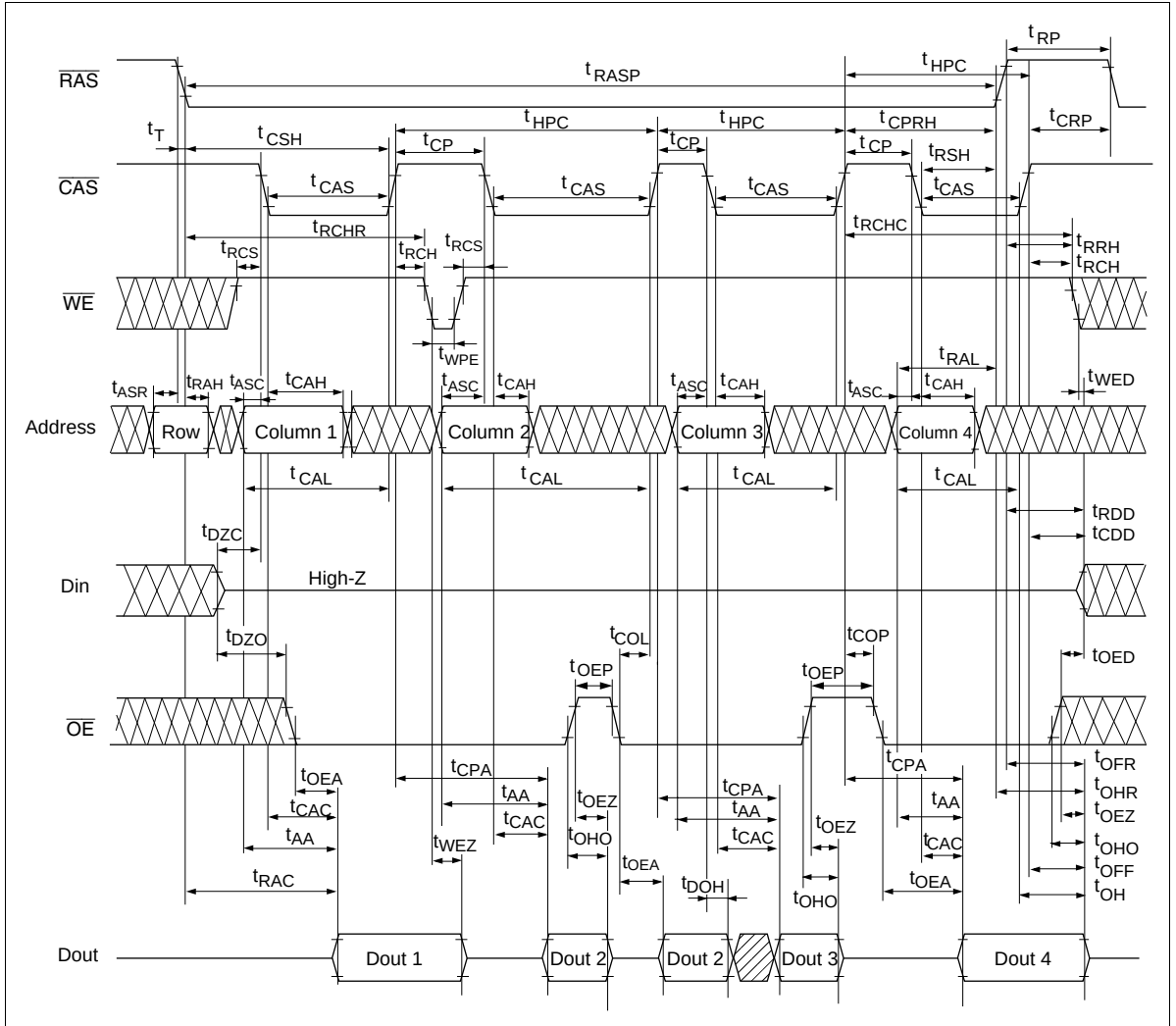
CAS-Before-RAS Refresh Cycle



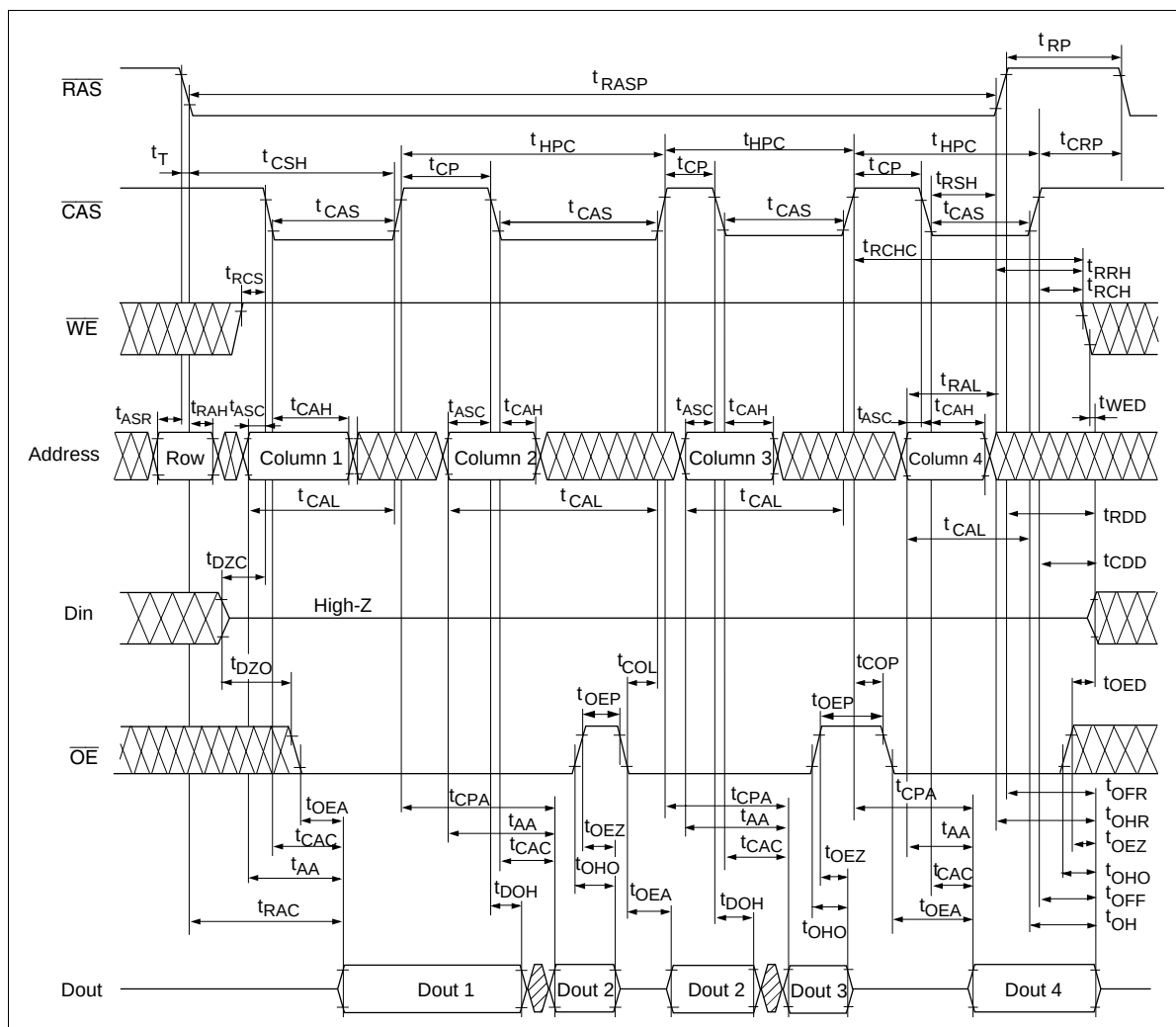
Hidden Refresh



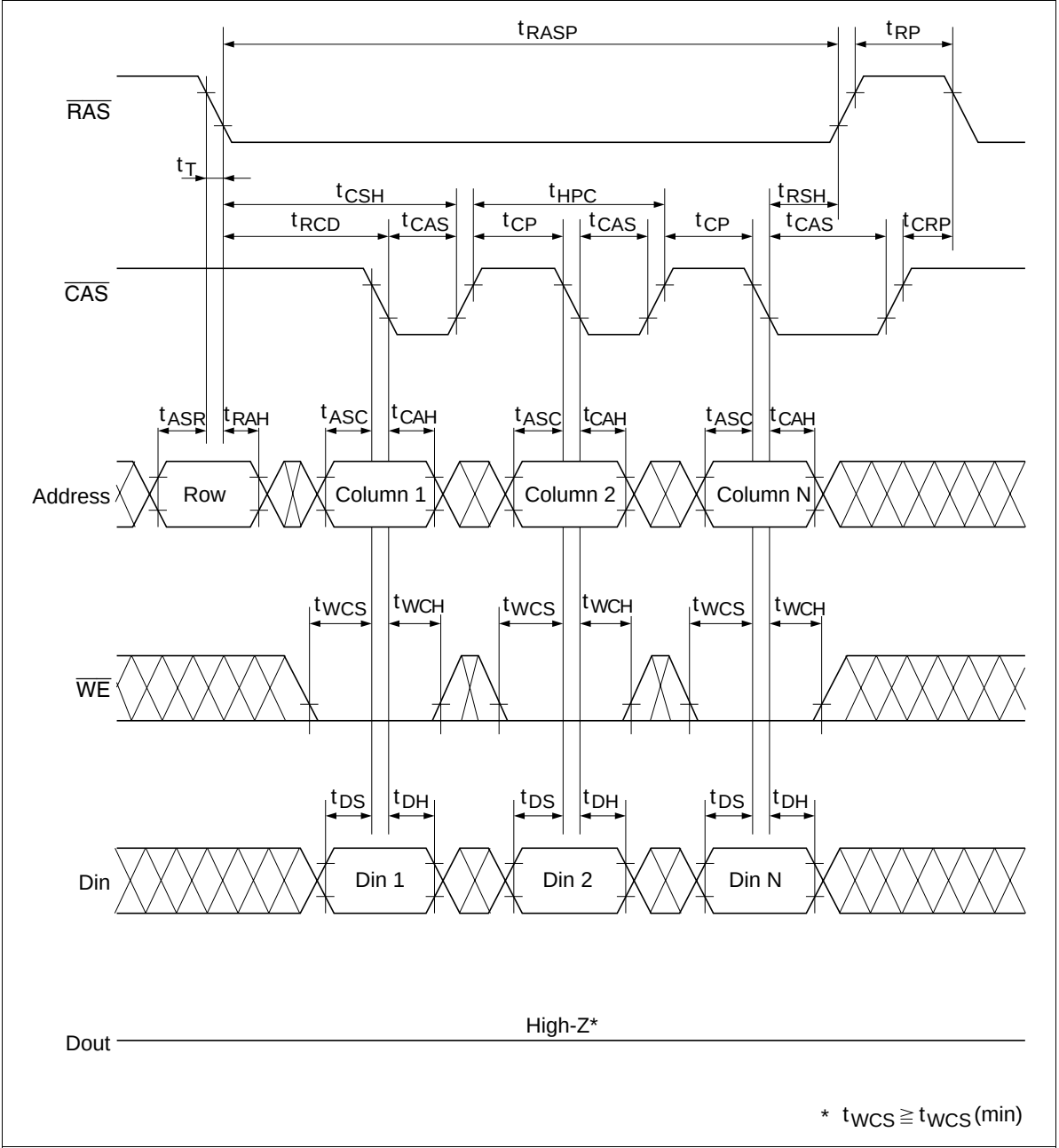
EDO Page Mode Read Cycle (1)

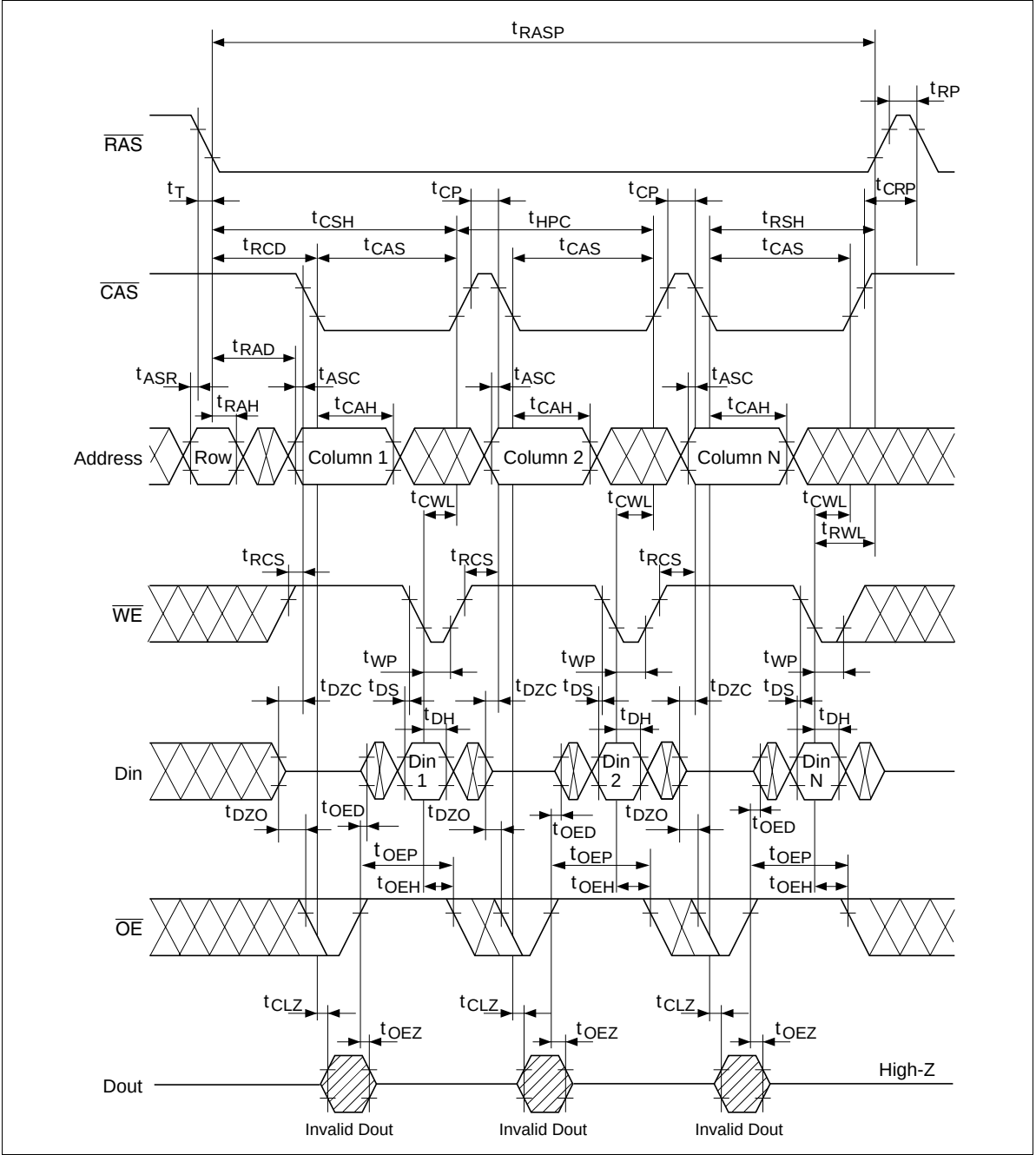


EDO Page Mode Read Cycle (2)

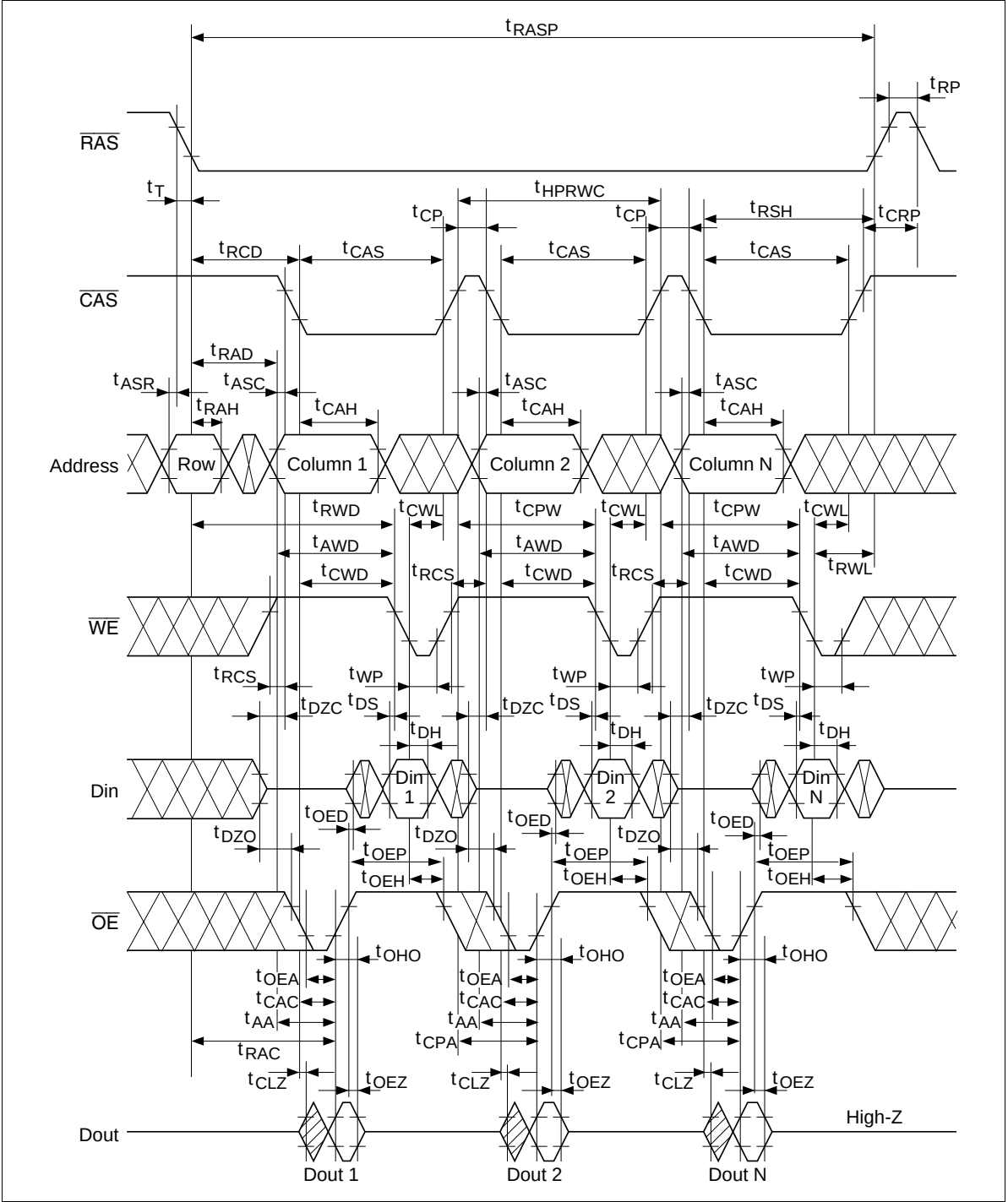


EDO Page Mode Early Write Cycle

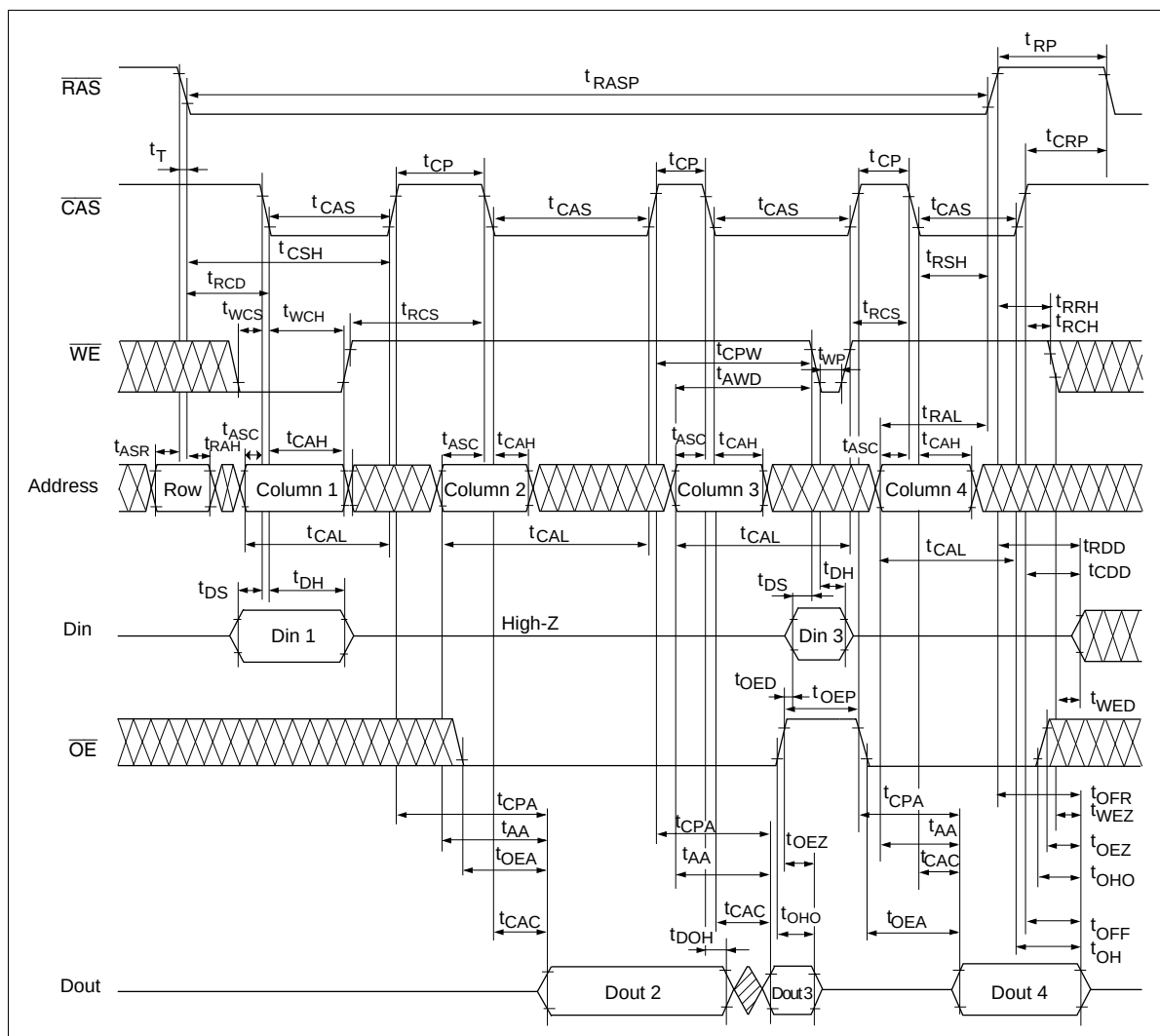




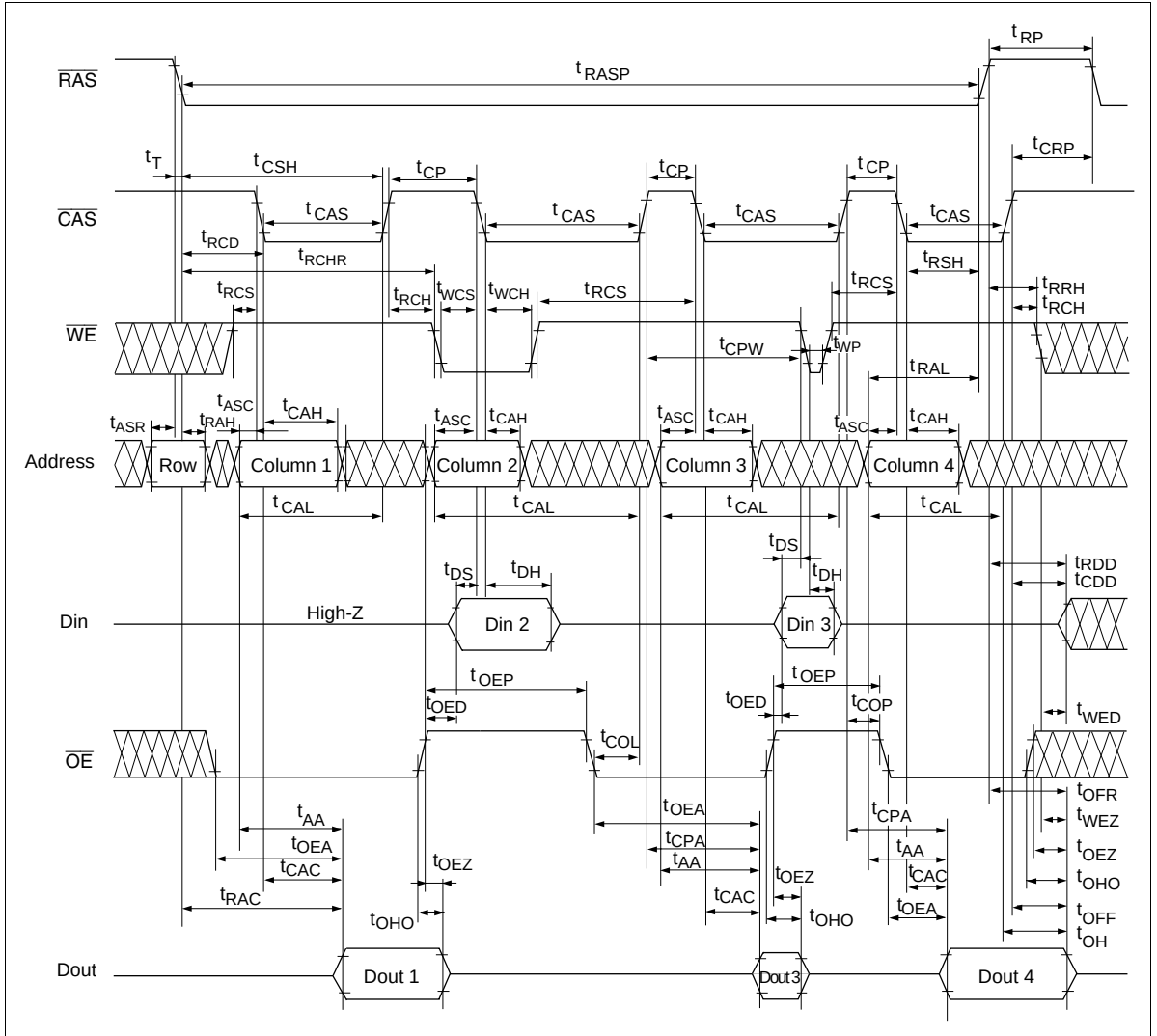
EDO Page Mode Read-Modify-Write Cycle*18



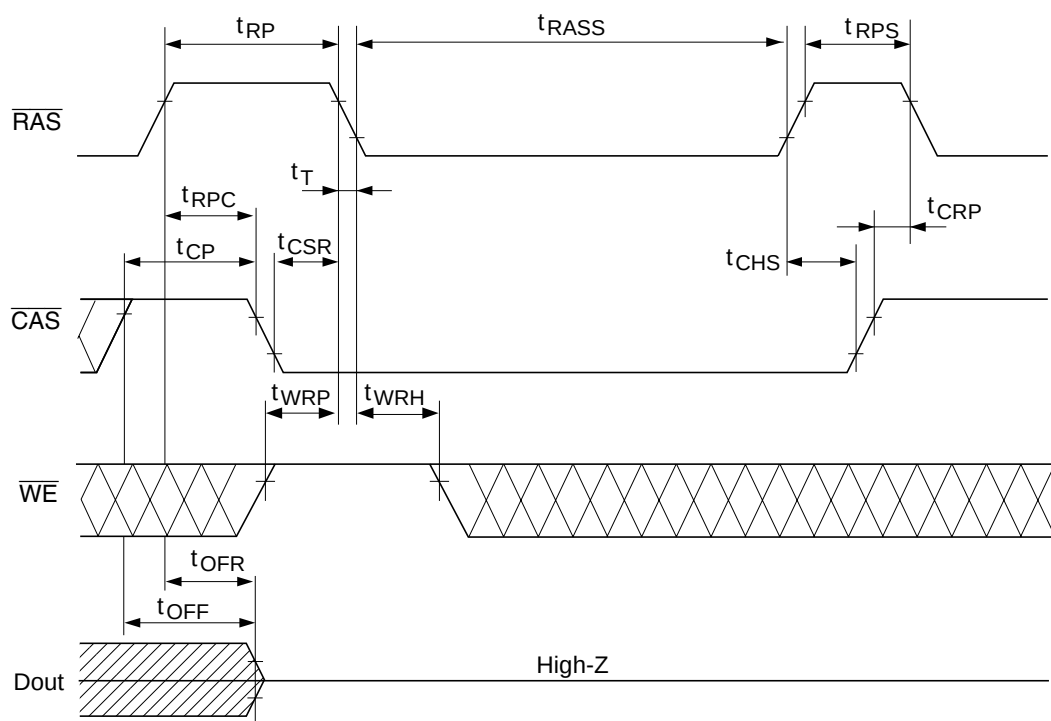
EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)



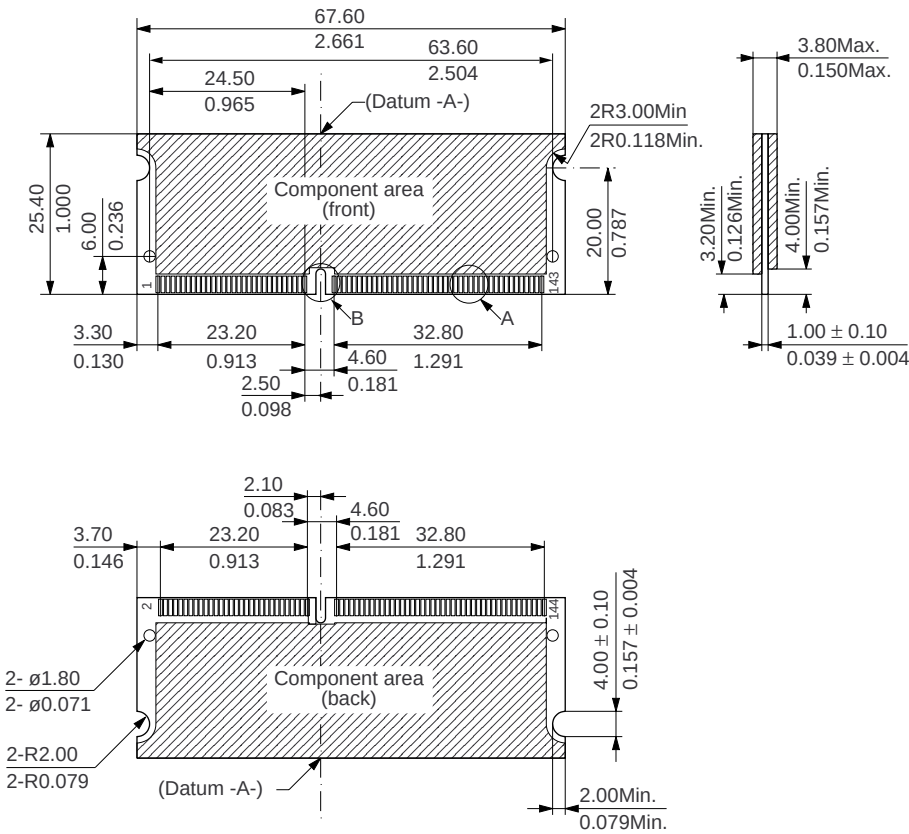
Self Refresh Mode Cycle*^{22, 23, 24}



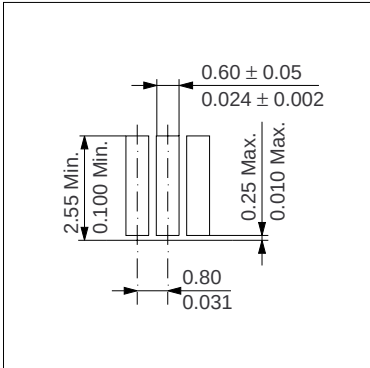
Physical Outline

HB56UW865DB Series

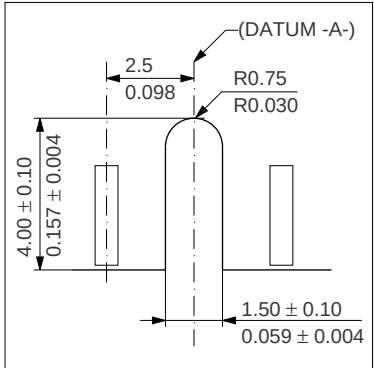
Unit: mm/inch



Detail A



Detail B



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 9, 1996	Initial issue	S. Tsukui	K. Tsuneda
1.0	May. 20, 1997	Addition of HB56UW865DB-6AL/7AL Series Addition of Self refresh mode (L-version) Change of Serial PD Matrix DC Characteristics I_{CC1} max: 1480/1320 mA to 1320/1160 mA I_{CC3} max: 1480/1320 mA to 1320/1160 mA I_{CC6} max: 1200/1040 mA to 1120/960 mA I_{CC7} max: 1160/1000 mA to 1000/880 mA Addition of I_{CC2} max (L-version): 1.6/1.6 mA Addition of I_{CC10} max: 5.2/5.2 mA Addition of I_{CC11} max: 4/4 mA I_{LI} Test conditions: $0\text{ V} \leq V_{out} < 4.6\text{ V}$ to $0\text{ V} \leq V_{out} < V_{CC} + 0.3\text{ V}$ I_{LO} Testconditions: $0\text{ V} \leq V_{out} < 4.6\text{ V}$ to $0\text{ V} \leq V_{out} < V_{CC}$ Addition of note 4 Timing Waveforms Addition of Self refresh cycle		
