KESRX04

260 to 470MHz. ASK Receiver with Power Down

Preliminary Information

DS4997 - 1.5 August 1998

The KESRX04 is a single chip ASK (Amplitude Shift Key) Receiver IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control, RF tagging and local paging systems.

The receiver offers an exceptionally high level of integration and performance to meet the local oscillator radiation requirements of regulatory authorities world-wide. Functionally the device works in the same way as the KESRX01 with the added features of low supply voltage, in-band interference rejection (anti-jamming detector), a 2 stage power down to enable receiver systems to be implemented with less than 1mA supply, and a wide IF bandwidth and drive stage to interface to an external ceramic IF band pass filter at intermediate frequencies from 0.2MHz to 15MHz.

The KESRX04 is an ideal receiver for difficult reception areas where high level interferers would jam the wanted signal. The anti-jamming circuit allows operation to be possible with interfering signals which are more than 14dB stronger than the wanted signal, without the cost penalties of increased IF selectivity and frequency accuracy.

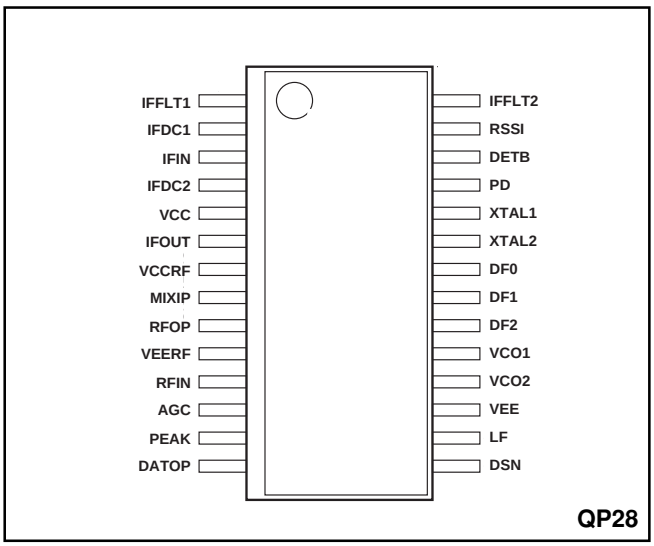


Figure 1 Pin Connections (top view)

FEATURES

- In-band interference rejection (typ. 14dB)
- -103dBm Sensitivity (IF BW = 470kHz)
- AGC around LNA and Mixer
- Low supply voltage (3 to 6V)
- 2 stage power-down for low current applications
- Interface for ceramic IF filters up to 15MHz

APPLICATIONS

- Remote Keyless Entry
- Security, tagging
- Remote Controlled equipment

ORDERING INFORMATION

KESRX04/IG/QP1S (anti-static tubes)
KESRX04/IG/QP1T (tape and reel)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc	-0.5V to +7V
Storage temperature,Tstg	-55 to 150°C
Junction Temperature, Tj	-55 to 150°C
RF Input power	+20dBm from 50Ω

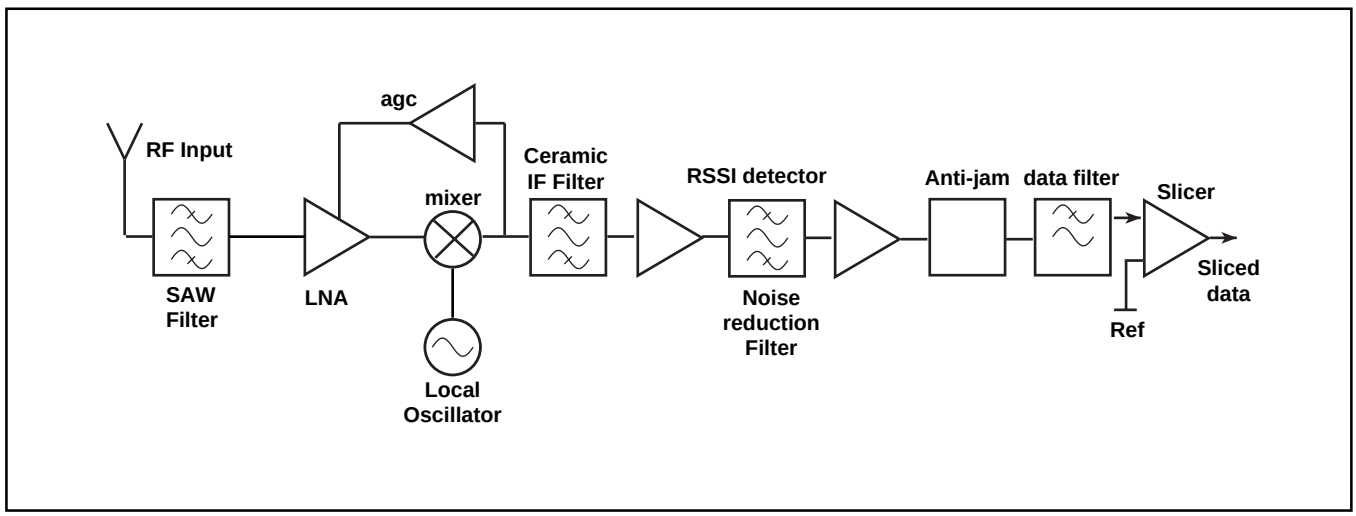


Figure 2 Typical system application

PIN DESCRIPTION

Pin	Symbol	Function
1	IFFLT1	Noise reducing IF filter
2	IFDC1	Log amp dc stability capacitor
3	IFIN	Log amp input
4	IFDC2	Log amp dc stability capacitor
5	VCC	Positive supply
6	IFOUT	IF output to external IF filter
7	VCCRF	Positive supply for RF circuits
8	MIXIP	Mixer input
9	RFOP	Output from LNA
10	VEERF	Negative supply for RF circuits
11	RFIN	Input to LNA
12	AGC	RF AGC time constant
13	PEAK	Data signal peak detect
14	DATOP	Sliced data output
15	DSN	Data slice level
16	LF	PLL loop filter
17	VEE	Negative supply
18	VCO2	Voltage controlled oscillator
19	VCO1	Voltage controlled oscillator
20	DF2	Data filter
21	DF1	Data filter
22	DF0	Data filter
23	XTAL2	Crystal oscillator
24	XTAL1	Crystal oscillator
25	PD	Power down
26	DETB	Anti-jam detector input
27	RSSI	RSSI output
28	IFFLT2	Noise reducing IF filter

DESCRIPTION

The single-conversion super-heterodyne receiver approach is now generally considered the way forward for ISM band type applications because of lower cost, superior selectivity, lower radiation, and flexibility over other techniques. For power-conscious, hand-held applications KESRX04 provides improved performance and flexibility on a lower 3.0V supply and a power-down feature allows faster switch-on times for use in a pulsed power saving mode.

Although this is a relatively simple receiver, the flexibility of using an external IF filter allows the designer to choose both the selectivity and the IF in order to optimise the performance for a wide range of applications and locations world wide.

The KESRX04, with its Anti-jamming detector circuit, is an ideal ASK / OOK receiver for difficult reception areas caused by interference such as “Amateur Radio Repeater Stations” and Wireless Stereo Head-Phones”. Operation is possible with interfering signals which are more than 14dB stronger that the wanted signal (IF bandwidth = 470kHz.), without the cost penalities of increased IF selectivity and frequency accuracy.

Figure 2 is the system block diagram for the device with an external ceramic IF filter, SAW fillter and noise reduction filter.

ELECTRICAL CHARACTERISTICS Test conditions
T amb = –40°C to + 85°C, V_{CC} = 3.0V to 6.0V. These characteristics are guaranteed by either device characterisation, production test and or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated using test circuit Figure 12.

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	3.0		6.0	V	
Ambient temperature	Ta	–40		+85	°C	
Test Frequency			470		MHz	
local Oscillator		480.7			MHz	local oscillator frequency configured for high side injection, except where otherwise specified

ESD Protection: All pins meet 2kV Human Body Model requirement. Except pins 9 and 11, which are limited to 700V and pins 18 and 19 which are limited to 1.00kV.

ELECTRICAL CHARACTERISTICS D.C.
T amb = –40°C to + 85°C, V_{CC} = 3.0V to 6.0V. These characteristics are guaranteed by either device characterisation production test and or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Condition
		Min	Typ	Max		
Supply Current						
Receive mode (PD2)	Icc		3.7	4.5	mA	All. PD=High. RF input <-50dBm.
Power down (PD1)	Icc1		0.33	0.5	mA	All. PD=Vcc/2 or high impedance source. Vcc = 3 to 6.0V (4)
Power down (PD0)	Icc2		33	50	µA	All. PD=low

ELECTRICAL CHARACTERISTICS A.C

Parameter	Symbol	Value			Units	Condition
		Min	Typ	Max		
Input frequency range	fs	260		470	MHz	All
Intermediate Frequency	IF	0.2		15.0	MHz.	All. (8)
Sensitivity (test fixture)	Vin(min)		8.0	23.0	µVrms	20kB/s data rate at 470MHz. (1)
Sensitivity (application)	Vin(min)		1.5		µVrms	Circuit as Figure 11 with SAW filter removed1kB/s data rate at 433.92MHz. (3)
Overload Performance	Vin(max)	0.5	2.23		Vrms	20kB/s data rate at 470MHz. (2)
PLL control line (pin 16) To achieve 90% of final value PD0 to PD2	ts2		2.0	4.0	mS	All. Circuit as Figure 11 (5) Local Oscillator low side Injection 423.33 MHz.
PLL control line (pin 16) To achieve 90% of final value PD1 to PD2	ts3		1.0	3.0	mS	All. Circuit as Figure 11 (5) Local Oscillator low side Injection 423.33 MHz.
Data output Voltage High	Voh	Vcc-0.7V			Volt	Ioh=+10µA
Data output Voltage Low	Vol			0.7	Volt	Iol=-10µA
Conducted emissions	Antenna (LO)		5.6	100	µVrms	All Figure 11 (6), local Osc. low side injection = 423.3MHz

ELECTRICAL CHARACTERISTICS A.C.(continued)

These characteristics are typical values measured for a limited sample size. They are not guaranteed by production test. They are only given as a design guide to assist during the design-in phase of KESRX04.

Parameter	Symbol	Value			Units	Condition
		Min	Typ	Max		
Anti-jam rejection			+14		dB	Unmodulated interfering signal = -76dBm 433.82MHz. OOK modulated wanted signal = -90dBm 433.92MHz Figure 5 (7)
Internal RF Amplifier						
Parallel input impedance	Rfin		1.0 // 1.8		KΩ // pF	Fs=434MHz, Vcc= 5V, Tamb =25°C
Parallel input impedance	Rfin		1.6 // 1.9		KΩ // pF	Fs=315MHz, Vcc= 5V, Tamb =25°C
Parallel output impedance	Rfout		8.8 // 1.7		KΩ // pF	Fs=434MHz, Vcc= 5V, Tamb =25°C
Parallel output impedance	Rfout		18 // 1.8		KΩ // pF	Fs=315MHz, Vcc= 5V, Tamb =25°C
Noise Figure	NF		4.5		dB	Fs=434MHz; Vcc= 5V, Tamb =25°C matched 50ohm environment input and output
Noise matching Impedance	Rfin		1.0 // 4.6		KΩ // nH	Fs=434MHz, Vcc= 5V, Tamb =25°C
1dB compression point (input referred)	Rfin		-20		dBm	Fs=434MHz, Vcc= 5V, Tamb =25°C matched 50ohm environment input and output
Amplifier gain	RFamp		13		dB	Fs=434MHz., Vcc= 5V, Tamb =25°C O/P matched to Mixer input impedance RF Amplifier is **conditionally stable**
MIXER						
Parallel input impedance	MIXIP		1.6 // 1.8		KΩ // pF	Fs=434MHz, Vcc= 5V, Tamb =25°C
Parallel input impedance	MIXIP		1.6 // 1.8		KΩ // pF	Fs=315MHz, Vcc= 5V, Tamb =25°C
Output impedance	IF1		300		Ω	Fs=10.7MHz, Vcc= 5V, Tamb =25°C
Noise Figure (Double side band measurement)	NF		10		dB	Fs=434MHz; Vcc= 5V, Tamb =25°C matched 50ohm environment input and output
Mixer conversion gain	Amix		9		dB	Fs=434MHz., Vcc= 5V, Tamb =25°C Measured at input to ceramic filter. Includes 6dB matching loss
IF Strip (RSSI)						
IF2 input impedance			4.0		KΩ	IF=10.7MHz, Vcc= 5V, Tamb =25°C
IF gain of log amp	Alog		80		dB	All, Vcc= 5V, Tamb =25°C

Notes:

1. The Sensitivity of the test fixture Figure 12 is degraded by loading the input to RF amplifier with 50 ohms, lack of image rejection and increasing the data filter bandwidth to 50kHz. Sensitivity is defined as the average signal level measured at the input necessary to achieve a bit error ratio of 0.01 where the input signal is a return to zero pulse at 470MHz.,with an average duty cycle of 50%, 20kB/s data rate with the receiver bandwidth set to 470kHz.

2. Peak RF input level, pin RFIN, to overload the demodulator with the AGC operating. Equivalent to +7dBm for 50 ohm input impedance. Where the input signal is a return to zero pulse at 470MHz. with an average duty cycle of 50%. 20kB/s data rate with the receiver bandwidth set to 470kHz.

3. Sensitivity is defined as the average signal level measured at the input necessary to achieve a bit error ratio of 0.01 where the input signal is a return to zero pulse with an average duty cycle of 50%, 1kB/s data rate. Equivalent to -103dBm for 50ohm input impedance. Does not include insertion loss of SAW filter at RF input but does include IF filter of 470kHz 3dB bandwidth and a data filter bandwidth of 5kHz. This equates closely to a measurement of tangential sensitivity.

4. The performance of the power down option PD1 to PD2 cannot be guaranteed below 3V for temperatures less than 0°C

5. Time taken for PLL lock voltage to achieve 90% transition point of the control signal and the VCO frequency to achieve within 470kHz of the final frequency. The time taken to acquire PLL acquisition is governed by the PLL loop filter (C12, C1 and R2) and the crystal oscillator components (XTAL1, C13 and C14). The dominant term for PLL aquistion is the start-up time of the crystal oscillator circuit, provided the PLL loop filter settling time is much less than the crystal oscillator start-up time. Figure 6 illustrates a suitable test setup for measuring the acquisition time of the PLL. The electrical characterisation parameters are based on the following set of conditions:

   Crystal Oscillator circuit
   C13 = C14 = 15pF
   XTAL 1

Freq.	6.6128 MHz.
ESR	15.3 Ω
L	85.36 mH
C0	1.83 pF
C1	6.8 fF

   PLL loop filter
   C12 = 1.5 nF,
   C1 = 180pF
   R1 = 10KΩ

6. Local oscillator power fed back into 50ohm source at antenna input (RF input). Measured with RF input matching network shown in Figure 11.

7. In-band interference rejection for an unmodulated interfering signal at 100kHz. low side from the wanted modulated signal at 433.92MHz. to achieve a Bit Error Rate =0.01. Figure 5 illustrates a suitable test set-up for measuring the interference rejection and selectivity of the receiver.

   Wanted signal = -90dBm at 433.92MHz.
   (1kB/s. 50% duty cycle)

   Interfering signal = -76dBm at 433.82MHz.
   (unmodulated)

   Interference rejection typically equals +14dBm.

i.e. in-band interfering signal is 14dBm above the wanted signal level at –90dBm.

8. Actual intermediate frequency determined by choice of crystal and external ceramic filter.

Functional Operation

Power Down

The PD pin, a tristate input, provides a 2 stage power down for the receiver. The receiver is fully operational when the pin is held high and is fully powered down when the pin is taken to ground.

Status	PD Pin	Status
PD0	Low (0V)	Receiver powered down
PD1	Vcc/2	Crystal oscillator running
PD2	High (Vcc)	Receive mode

PD0 = Low.

None of the receiver circuits are functional. Current, Icc2, is reduced to its lowest level, <50µA (Vcc applied). A longer settling time (ts2) is required to restore full performance after switching to receive mode, PD0 to PD2 (Figure 6).

PD1 = Vcc/2 or high impedance source (CMOS tristate).

A non-receiving state with some critical circuits running including the crystal oscillator. Current consumption, Icc1, is reduced to about 330µA. When switching to the receive state, PD1 to PD2 (Figure 6), data can start to be recovered within 1ms (ts3) for signals close to maximum sensitivity.

PD2 = High.

The receiver is fully functional ready to receive data.

RF down-converter

An internal RF amplifier is designed to interface to an input SAW filter with a maximum insertion loss of 3dB.

The RF amplifier gain is about 13dB at 460MHz when matched into the mixer, while the RF amplifer noise figure is about 4.5dB when fed from a 50 ohm source. The internal RF amplifier is **conditionally stable** and feeds a double balanced mixer through an external impedance matching circuit, RFOP to MIXIP.

The AGC circuit monitors the mixer signal output level. Control is fed back, applying AGC to the RF amplifier to prevent overloading in the mixer and the generation of unwanted distortion products. This also has the effect of reducing the RSSI characteristic slope and extending its range of operation by more than 20dB at high signal levels, compare Figure 9B and Figure 9C.

The AGC circuit also applies mixer booster current to improve the linearity of the mixer at high signal levels. This can be confirmed by monitoring the current consumption of the receiver with applied RF signal level Figure 9D.

The AGC circuit comes into operation at input signals greater than ~ -35dBm and reduces the RF amplifer gain by 6dB at an input signal level of ~ -25dBm. Since the AGC operates on the mixer output signal level then the exact point where the AGC comes into operation depends on the RF amplifer to mixer matching circuits and RF amplifer gain.

IF interface

Unlike KESRX01 there is no internal integrated IF filter. This is to provide a more flexible design and allows the system designer to use a low IF or high IF up to 15MHz. Typically, a 10.7MHz Ceramic IF filter connected between IFOUT and IFIN would be used together with an input RF SAW filter to give very good image channel rejection. The choice of bandwidth for the 10.7MHz ceramic filter depends on frequency tolerancing of the transmitter, receiver, data rate and component cost.

The IF filter drive, IFOUT, is a voltage drive with a 300 ohm series resistance. This allows impedance matching to the ceramic IF filter to be set by an external series resistor. A 10.7MHz ceramic filter with, typically, a 300 ohm input impedance does not require an external matching resistor at IFOUT.

The input to the log amp, IFIN, is high impedance with an internal 4Kohm shunt resistor. Impedance matching to the output of the ceramic filter is achieved by an external shunt resistor R9 between IFIN and IFDC1.

Phase Lock Loop VCO

The local oscillator (LO) is a VCO locked to a crystal reference by a phase lock loop (PLL). The VCO gain is nominally 40MHz/Volt depending on the external varactor used. The LO frequency is divided by 64 and fed into the phase-frequency detector, where the reference frequency is provided from the crystal oscillator. The phase detector output current into the PLL loop filter is nominally ±30µA. The max loop filter bandwidth is 50kHz.

Conducted LO signals capable of being radiated from the antenna of the complete receiver are suppressed to a level of <-65dBm into 50ohms.

Voltage Controlled Oscillator (VCO) Circuit Design / Layout

The Local Oscillator (LO) frequency is controlled by a parallel resonant tuned circuit. The frequency of the local oscillator is controlled by a Phase Locked Loop (PLL), referenced to the crystal frequency.

Designing for VCO Track Parasitics

To remove the effect of track parasitics the following procedure should be adopted.

1. Open circuit the control feed back from the PLL control loop by removing R1.
2. Connect an external Power Supply Unit (PSU = VCC/2) in place of R1, LF output Figure 3.
3. Using a spectrum analyser, monitor the LO level at the RFin port. Alternatively use a small pick-up coil to loosely couple to the signal generated across L2.
4. Note :- LO level is < -65 dBm, Range = 300 to 500MHz.
5. Vary the value of the PSU input to confirm that there is a corresponding change in LO frequency. Set the PSU at VCC/2. If the VCO does not oscillate at VCC/2, characterise the LO at an alternative voltage.
6. Using a plot of the varactor characteristic determine the varactor capacitance at VCC/2. e.g. for a 2 volt VCC design the Siemens BB833 capacitance at 1Volt = 10pF (approx.).
7. Using the following equation deduce the value of the total stray parasitic capacitance (Cp).

$$Cp = \left(\left(\frac{1}{(2\pi * LO)^2 * L2} \right) - Cv \right)$$

Cv: Varactor capacitance at Vcc/2

8. Using the following equation select the nearest value for L2 to centre the VCO at VCC/2.

$$L2 = \frac{1}{(2\pi * LO)^2 * (Cp + Cv)}$$

9. By varying the PSU voltage confirm that the LO is centred correctly at VCC/2, and that the oscillator operates over the range 0 to Vcc.
10. Disconnect the PSU and reconnect R1. Measure the value at LF output using a x10 probe and an oscilloscope. This should be a direct voltage with no ripple at VCC/2 (+/- 0.3 volt). If not repeat steps 1 to 8. To compensate for non standard inductor values vary the value of C18 and C11 to vary the capacitance of the varactor to centre the VCO at VCC/2.

Note:
It is important to minimise stray capacitance in the VCO circuit to ensure that the VCO starts oscillating. The use of a varactor with a low capacitance at zero bias is advisable. Similarly, reducing the values of C11 and C18 whilst increasing L2 will help to reduce the capacitance of the varactor at 0 volts, improving the reliability of the oscillator**.** A compact design methodology is recommended for the VCO circuit components L2, C11, C18 and D1.

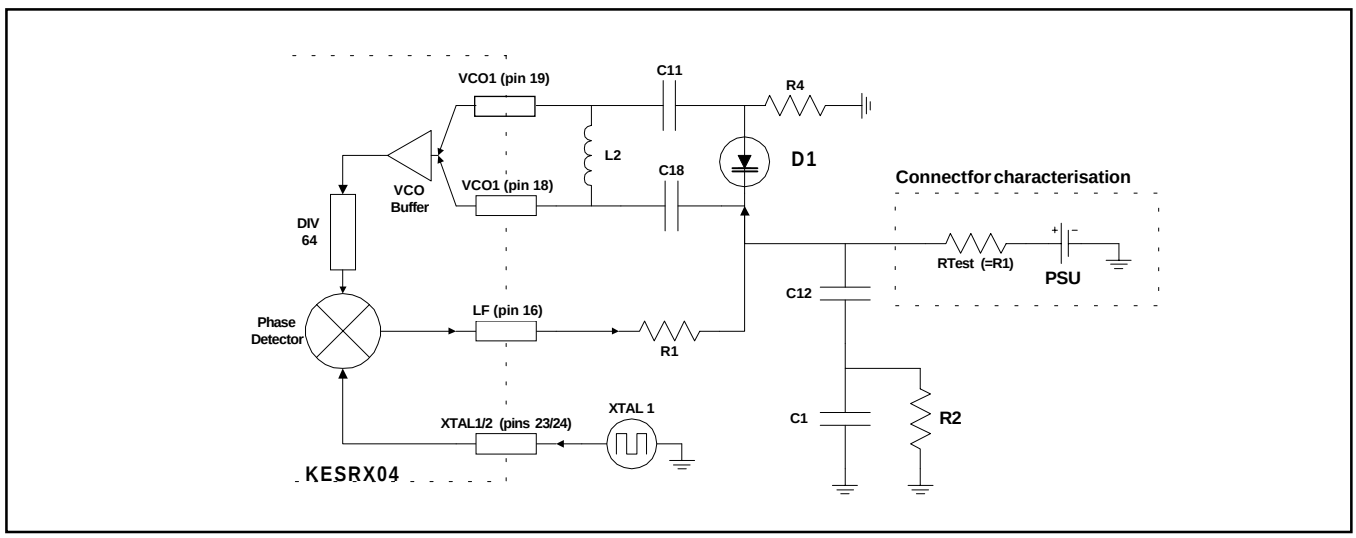


Figure 3 Characterising the VCO/PLL operation

IF amp/RSSI detector

This is a log amplifier with a gain > 80dB and an RSSI output used as the detector. The 3dB bandwidth of the IF log amplifier is typically 20MHz to allow for high IF's to be used. However, normally, this wide IF bandwidth would limit the overall sensitivity of the receiver due to the amplified wide band noise generated in the first IF stage.

The RSSI detector is not frequency selective so that any wide band noise introduced after the intermediate filter will be detected as signal. A simple LC noise reduction filter is therefore positioned part way down the log amplifier to reduce the noise power from the earlier stages. Typically this filter only needs to be a fixed component parallel LC filter (L5 // C7) between pins IFFLT1 and IFFLT2 with a 1MHz bandwidth (i.e. Q~10). There is an internal 20Kohm damping resistor across these pins which will determine the Q and the choice of L and C values.

i.e. $L = \frac{20000}{2.\pi.f_{IF}.Q};\qquad C = \frac{Q}{2.\pi.f_{IF}.20000}$

An external damping resistor should not be used as this will alter the gain of the log amplifier. A ceramic resonator or filter is not a suitable component here as a low impedance dc path must be maintained to remove dc voltage offsets in the high gain log amplifier. Further improvement in sensitivity can be gained by using a narrow band IF ceramic filter and a narrower noise reduction filter.

For a low IF receiver, <1MHz, a low pass filter can be used for both the IF and noise reduction filters. Such a receiver however will have virtually no image rejection capability, and will thus have a 3dB penality in noise factor impairing the ultimate sensitivity of the receiver by a minimum of 3dB.

The RSSI output transfer characteristic, at pin RSSI, has a slope of about 16mV/dB. A typical transfer characteristic from RF in input to RSSI output is plotted in Figure 9B, measured with a constant RF input signal. This shows the effect of the AGC in extending the range of the detector to +10dBm RF input signal and includes the effect of the AGC circuit adapting to this signal level.

Because the RF amplifier AGC has a fast attack time - slow decay time characteristic the gain of the stage remains constant during the data burst. This means that the change in output for a given extinction ratio also remains constant at approximately 16mV/dB up to peak input signal levels >+10dBm. This requires the decay time constant to exceed the transmitted bit period and no long period of zero signal power has been transmitted.

Increasing the decay time constant of the AGC circuit by increasing the value of C8 will impair the settling time (time to good data) of the receiver. When duty cycling the operation to the receiver between PD0 and PD2 to lower power consumption of the receiver. When Duty cycling the receiver between PD1 and PD2 the settling time of the receiver is independent of C8. In the application circuit Figure 11 the value of C8 is configured for minimum settling time.

Anti-jamming Circuit

The output of the RSSI is AC coupled into the Anti-jamming circuit where the signal is DC restored on the peak signal level Figure 7. The coupling capacitor charges to the appropriate DC level which is related to the final slice level for the data comparator. The anti-jamming circuit amplifies the peak of the signal to recover the data signal component even in the presence of CW jamming signals. The interferer causes modulation of the wanted signal at the beat frequency of the two signals and reduces the amplitude of the wanted data component making it more difficult to recover. By-passing the anti-jam circuit Figure 8 will result in data corruption for interfering RF signal levels 6dB below the wanted signal (Figure 5A)

The DC restoration circuit has a fast attack time and slow decay time, both controlled by the value of coupling capacitor chosen between RSSI and DETB pins.

Figure 5 illustrates a suitable test setup for characterising the interference rejection and selectivity of the receiver.

Figure 5A illustrates the in-band interference rejection with the anti-jam circuit connected Figure 7 and by-passed(Figure 8) at 3V Tamb = 25°C. Note, the improvement in interference rejection between the two modes of operation over the wanted signal range of -94 to -20dBm.

Figure 5B illustrates the difference in receiver selectivity with the ant-jam circuit connected (Figure 7) and by-passed (Figure 8). Note, the improvement in receiver selectivity between the two modes of operation. The selectivity curve with the anti-jam circuit by-passed is governed by the response of the front end SAW filter, IF ceramic filter and data filter. Providing no rejection for interfering signals within the pass band of the receiver. Whereas the receiver with the anti-jam circuit connected actively responds to the presence of the in-band interfering signal to recover the wanted OOK modulated signal. The action of the anti-jam circuit centres the bandwidth of the receiver around the wanted signal proportional to the data filter bandwidth to suppress the interfering beat frequency.

Figures 5A and 5B were recorded with the following component specification.

Component Specification (Figure 7)		Anti-Jam removed (Figure 8)	
R6	130KΩ	R6	12KΩ
C2	270pF	C2	removed
Data Filter BW	5kHz	Data Filter BW	5kHz
IFBW	470kHz	IF BW	470kHz
SAW BW	750kHz	SAW BW	750kHz
OOK modulation	4kB/s (50% duty cycle)	OOK modulation	4kB/S (50% duty cycle)

Component specification for Figure 5A and 5B

Interference rejection (dB) = Interferer (dBm) - Wanted (dBm)

The interference rejection of the receiver for different modulation schemes can be improved by:

- Changing the value of C2.
  Increasing the value of C2 will result in pulse stretching of the recovered signal

- Adjusting the comparator reference level (DSN) by offsetting the internal reference (Figure 4) by a high value resistor from the DSN pin to Vee and or the peak detector output. (Figure 11).

- Reducing the bandwidth of the data fillter, intermediate frequency filter and or the noise reduction filter (L5 // C7). Thebandwidth of the receiver must accommodate tolerancing of the data, transmitter and receiver.

- Increasing the value of AGC capacitor C8 to maintain the level of the AGC control during the "OFF" period of the wanted modulation signal. This will improve the interference rejection of the receiver but increase the time to good data from power-up PD0 to PD2. The application circuit Figure 11 has been optimised for time to good data.

Baseband

The RSSI output will contain wide band demodulated noise and signals which are within the RF and IF filter pass bands. An additional low pass data filter is therefore used to improve overall sensitivity.

KESRX04 has an integrated second-order Sallen-Key data filter whose characteristic is set by R10, R11, C5 and C6. Figure 7 shows the connections and calculation for the -3dB cut-off frequency and filter type, The cut-off frequency is determined from the data rate and the level of pulse distortion which can be tolerated. The data filter cut off frequency is usually set at 3 to 5 times the minimum pulse width period.

i.e. $$Fc = 5 * \frac{1}{(DataPulsewidth)}$$

The output from this filter, DF2, is directly coupled into the inverting input of the data comparator with a fixed slice level applied to the non-inverting input, DSN. A peak detector recovers the signal amplitude on the capacitor.

Normally, the comparator reference level used is the internal reference, a capacitor at Pin DSN serving to remove noise pick-up. In order to fine tune the slice level for sensitivity, squelch and optimum interference rejection the slice level can be offset from the internal reference by a high value resistor from the DSN pin to Vee and or the peak detector output (Figure 11).

The data comparator (slicer) output, DATOP, is CMOS compatible but is only capable of driving small capacitive loads, <20pF, depending on data rate. Data output has the **inverted sense** of the input signal at DF2.

The output drive current is nominally ±30µA so that a system using high data rates or higher capacitive loads, e.g. long track lengths, may need to incorporate a buffer transistor to provide the necessary edge speeds to the following logic circuits. The comparator has 20mV hysteresis built-in to reduce edge chatter.

The sense of the squelch on the data output is **LOW** when no signal is present. This may be confusing, as a **LOW** output during the data burst also corresponds to the 'ON' period, i.e. the MARK, of the RF OOK signal. However, it is the very first pulse of the data signal which causes the DC restoration capacitor of the anti-jamming circuit to charge to the correct level appropriate to the final slice level. As a consequence of this the very first pulse of the data transmission may be lost as the receiver adapts to the incoming signal level.

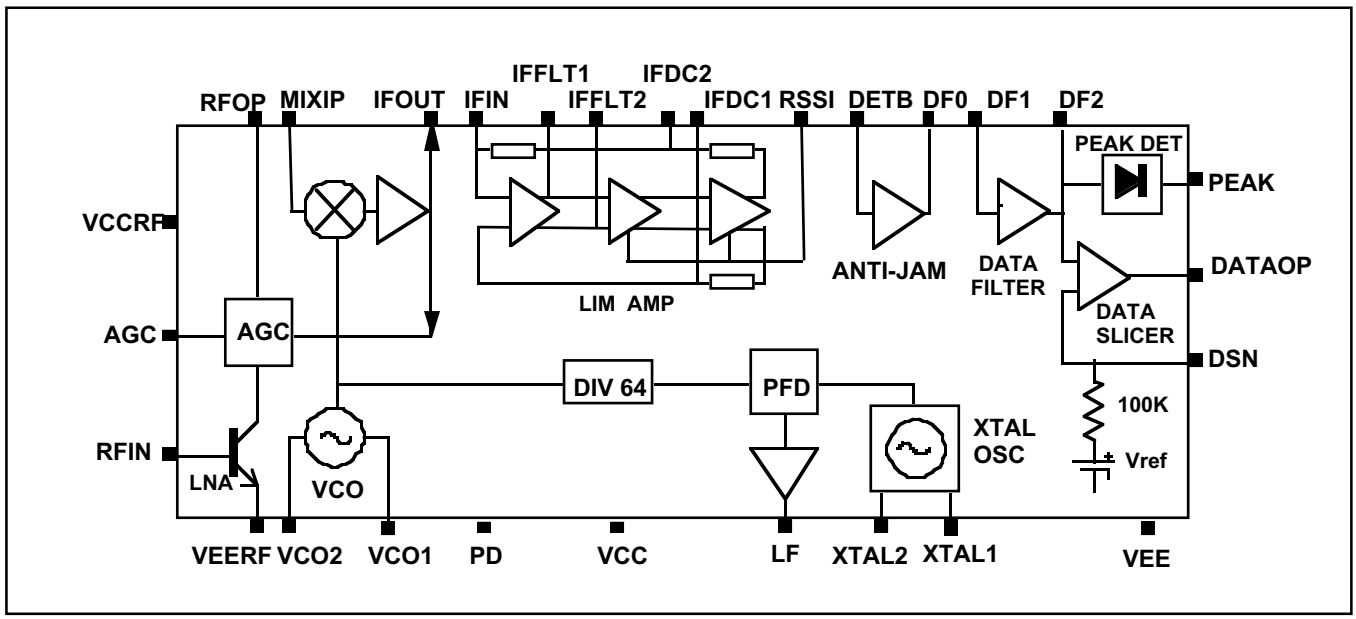


Figure 4 block schematic of KESRX04

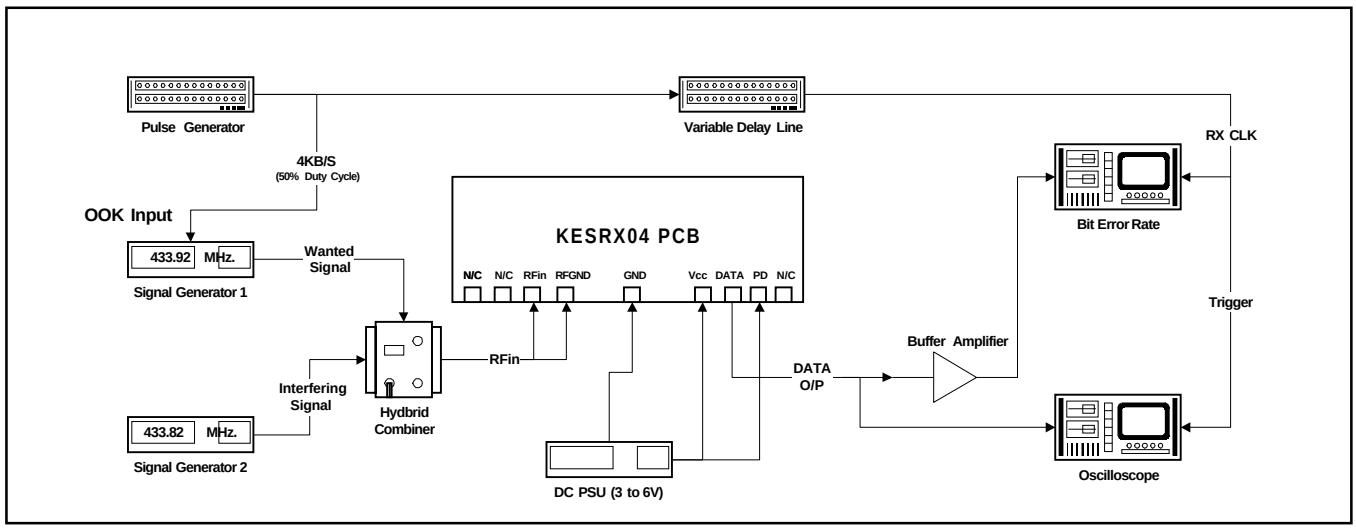


Figure 5 Characterising the selectivityand interference rejection

Note :

1 Variable delay line used to equalise the propagation delay of the receiver.
2 Buffer amplifier used to drive the low impedance input of the Bit Error Ratio analyser.
3 High impedance (*10 probe) oscilloscope probe recommended.

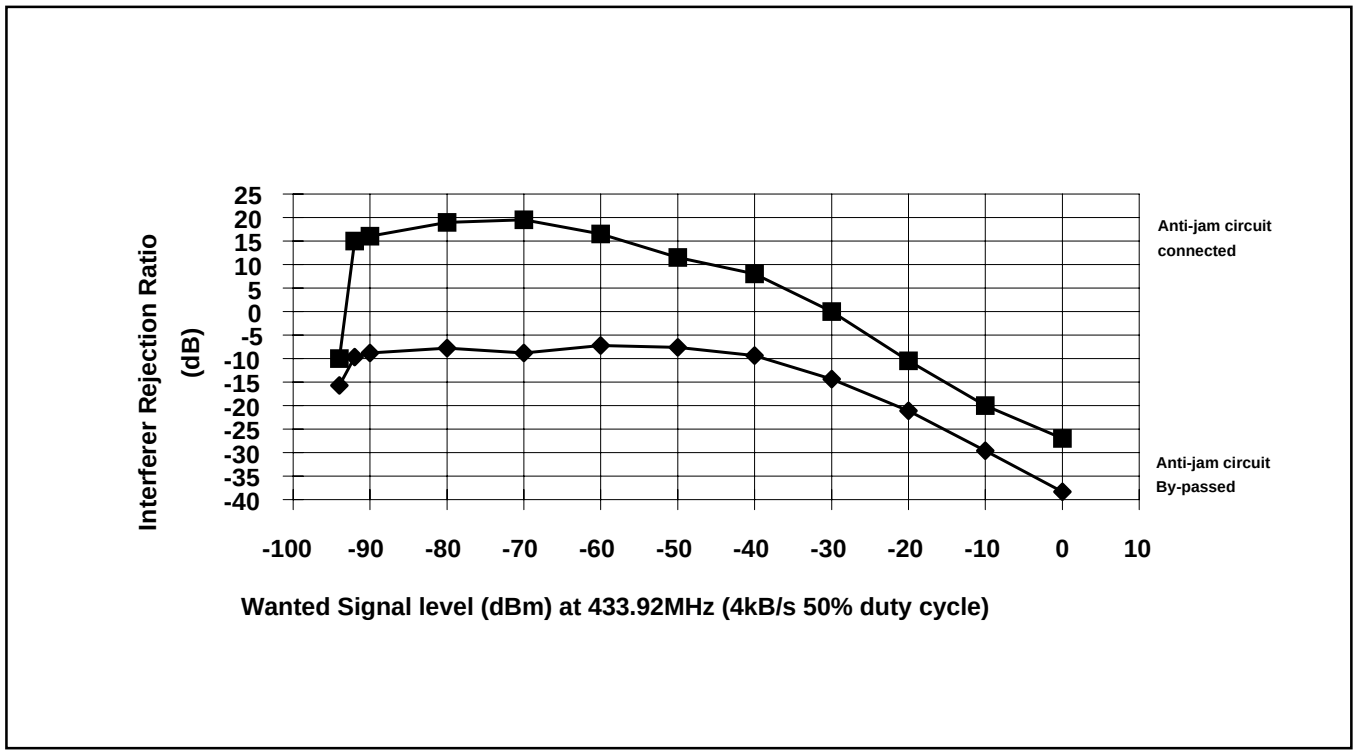


Figure 5a In-band interference rejection of the receiver

Note: Unmodulated interfering signal is 100kHz low side from wanted signal. Both signals are within the passband of the receiver (ceramic filter)

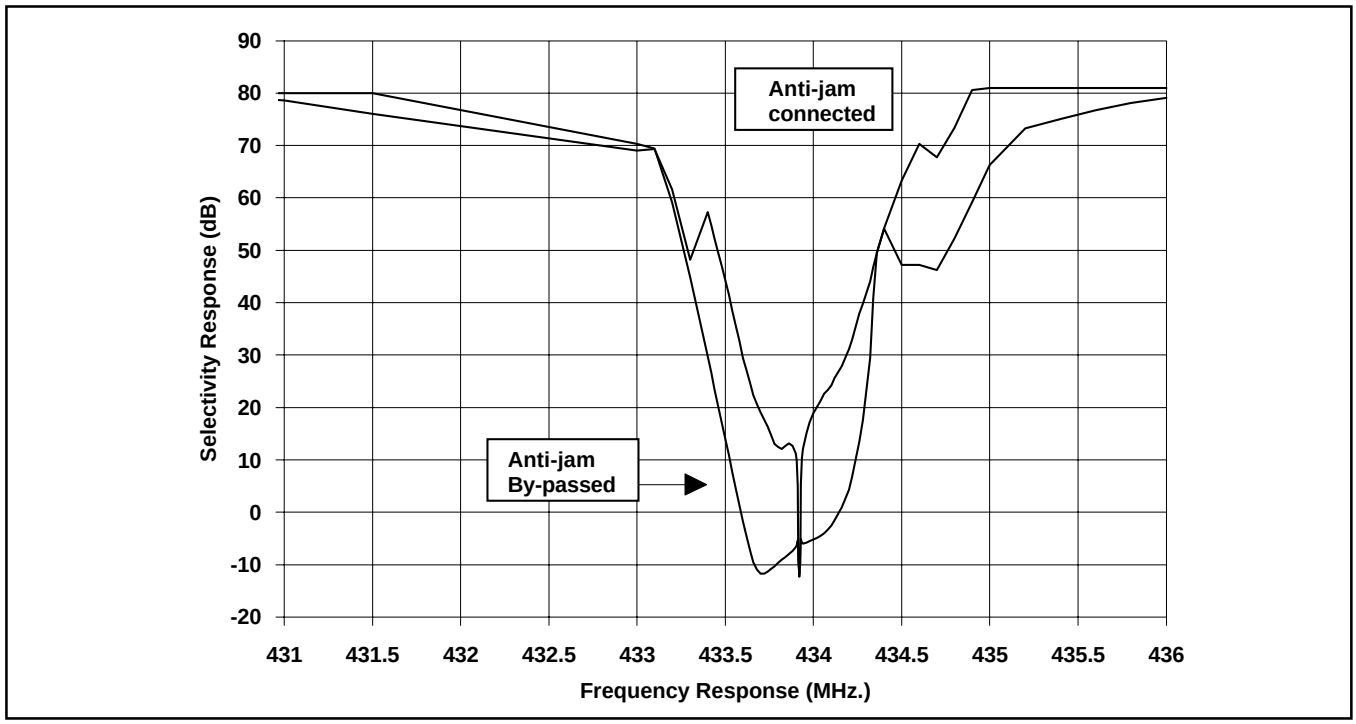


Figure 5b KESRX04 selectivity response

Note: The action of the anti-jam circuit to centre the bandwidth of the receiver around the wanted modulated signal at 433.92MHz

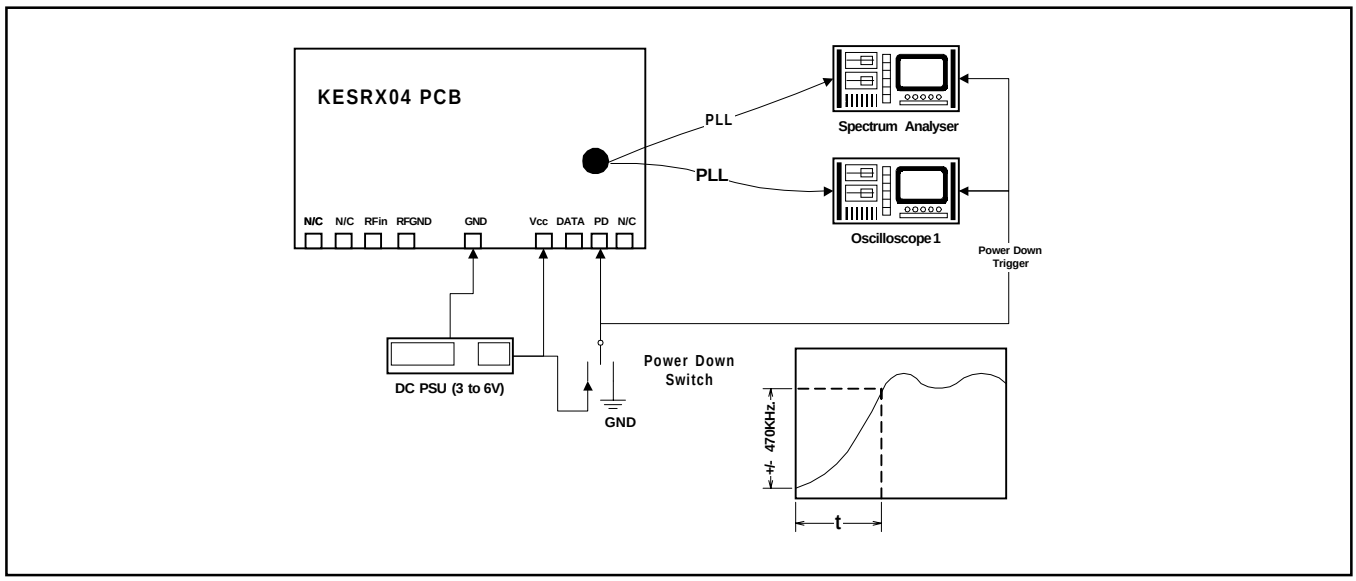


Figure 6 Characterising the PLL aquisition time from power-up

Note :

1 High impedance (*10 probe) oscilloscope probe recommended
2 Loosely coupled antenna or high impedance FET probe recommended for the spectrum analyser measurement.
3 Time taken for PLL to achieve 90% of final voltage and the VCO within +/- 470kHz. of final frequency (423.33MHz.)
4 Power down switch operation.

- PD0 = PD pin connected to GND, receiver fully powered down.
- PD1 = PD pin open circuit or connected to Vcc/2, crystal oscillator running.
- PD2 = PD pin connected to Vcc, receiver fully operational.

5. Spectrum analyser set to PLL lock frequency (423.33MHz), zero span 470kHz IF bandwidth, t sweep 20mS.

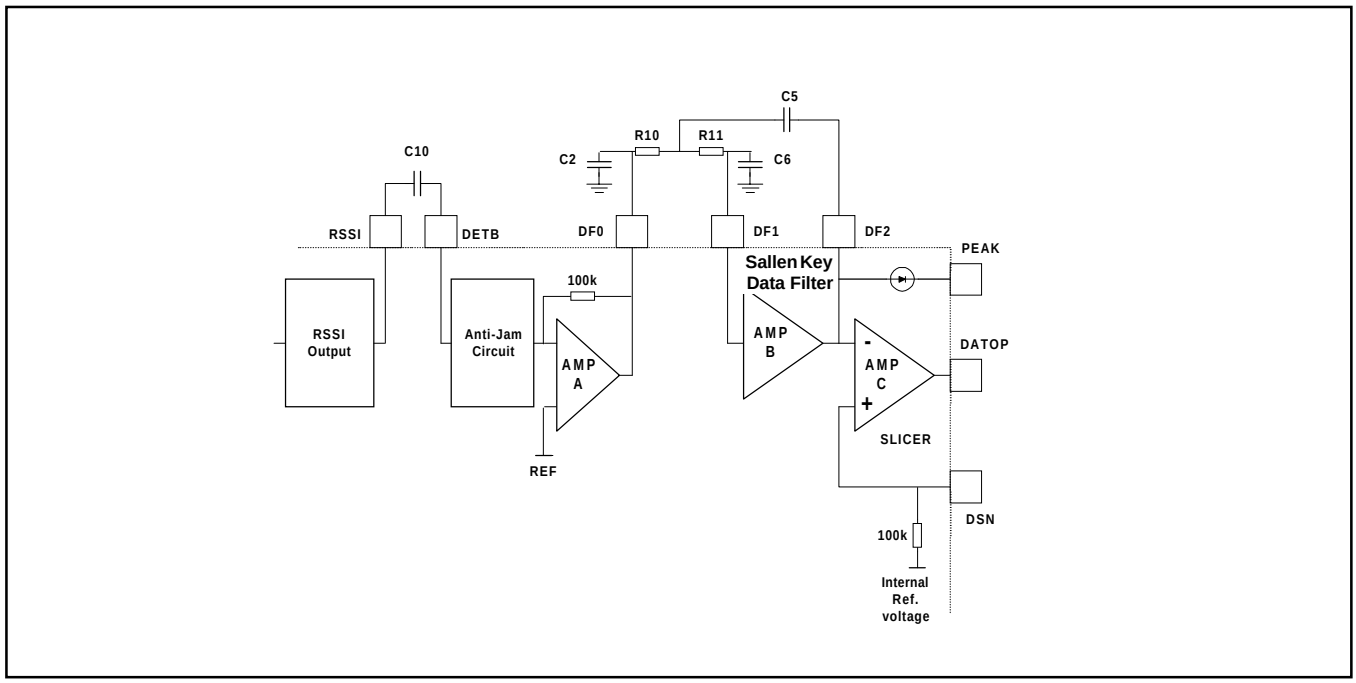


Figure 7 Anti - jamming circuit and data filter

Sallen-Key Data filter components

$\omega c = 2\pi f c Y$: $f c$: cut off frequency (Hz)

$$C5 = \frac{2.Q}{R.\omega c} \qquad C6 = \frac{1}{2.Q.R.\omega c}$$

Bessel	Butterworth
Q=0.577	Q=0.71
Y=1.732	Y=1.0

Example

To implement a Bessel response filter with a 10kHz 3dB cut-off frequency, R = 100kohm

Bessel Filter	C5 = 106pF	C6 = 80pF
Butterworth Filter	C5 = 150pF	C6 = 150pF

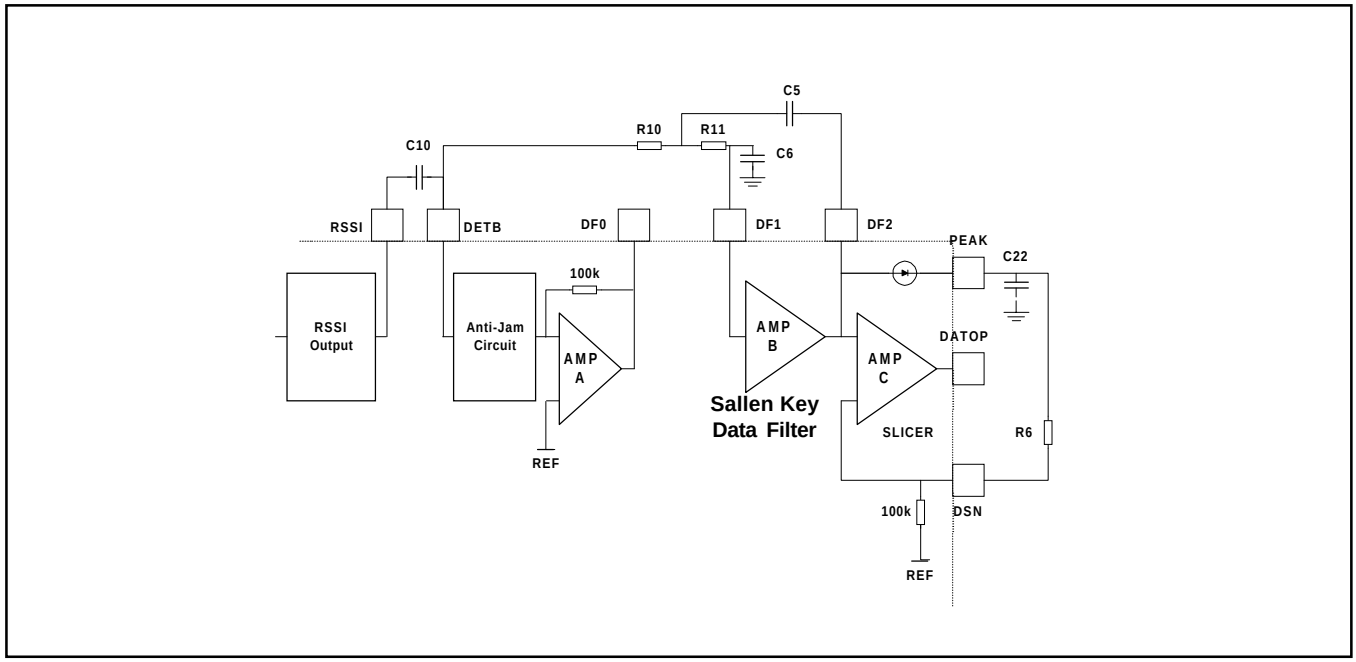


Figure 8 By-passing the anti - jamming circuit

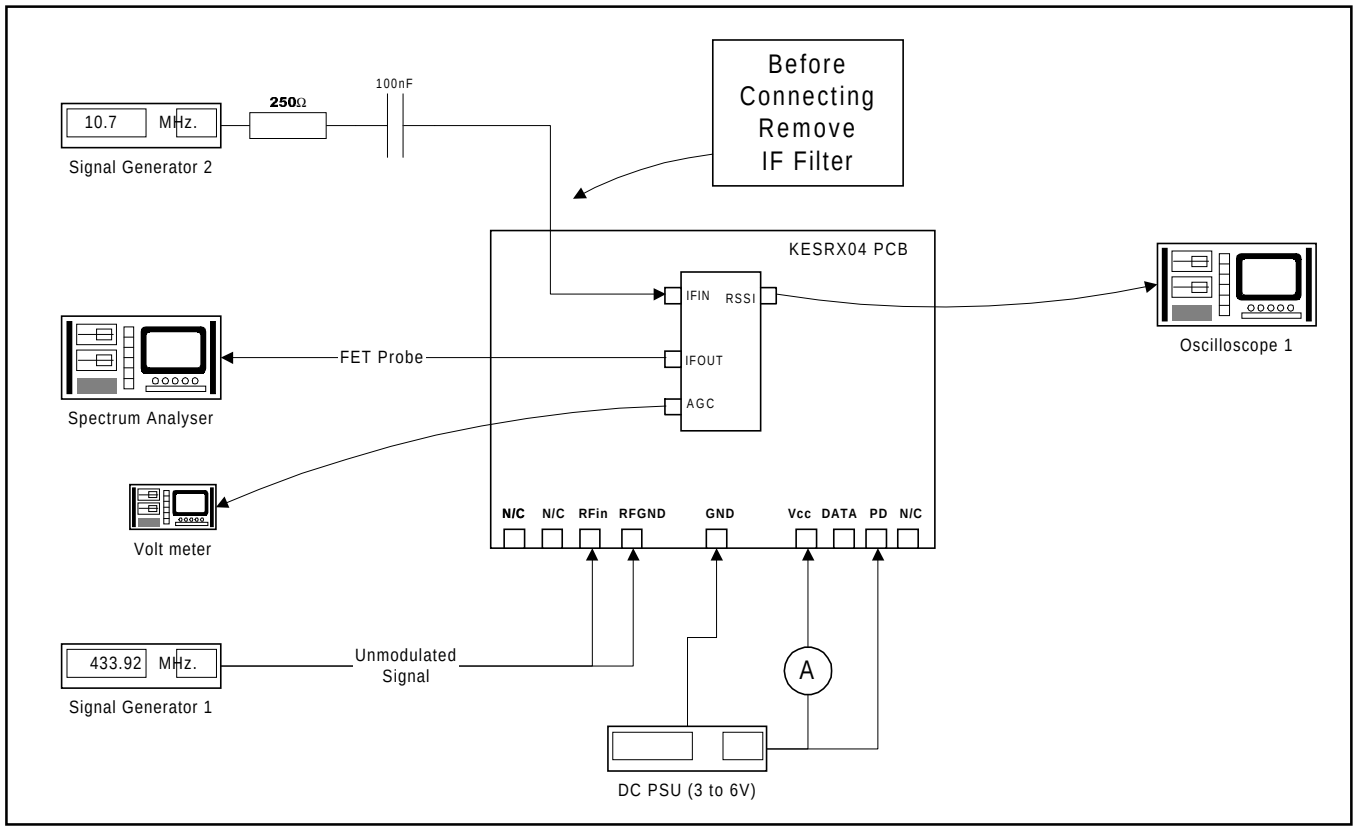


Figure 9 Characterising the receiver performance (Figure 9A to 9D)

Note: 1. 250 Ohms added to signal generator 2 to modifiy its characteristic impedance to mimic the output impedance of the ceramic filter.
2. 100nF capacitor to prevent de-biasing of IFIN.

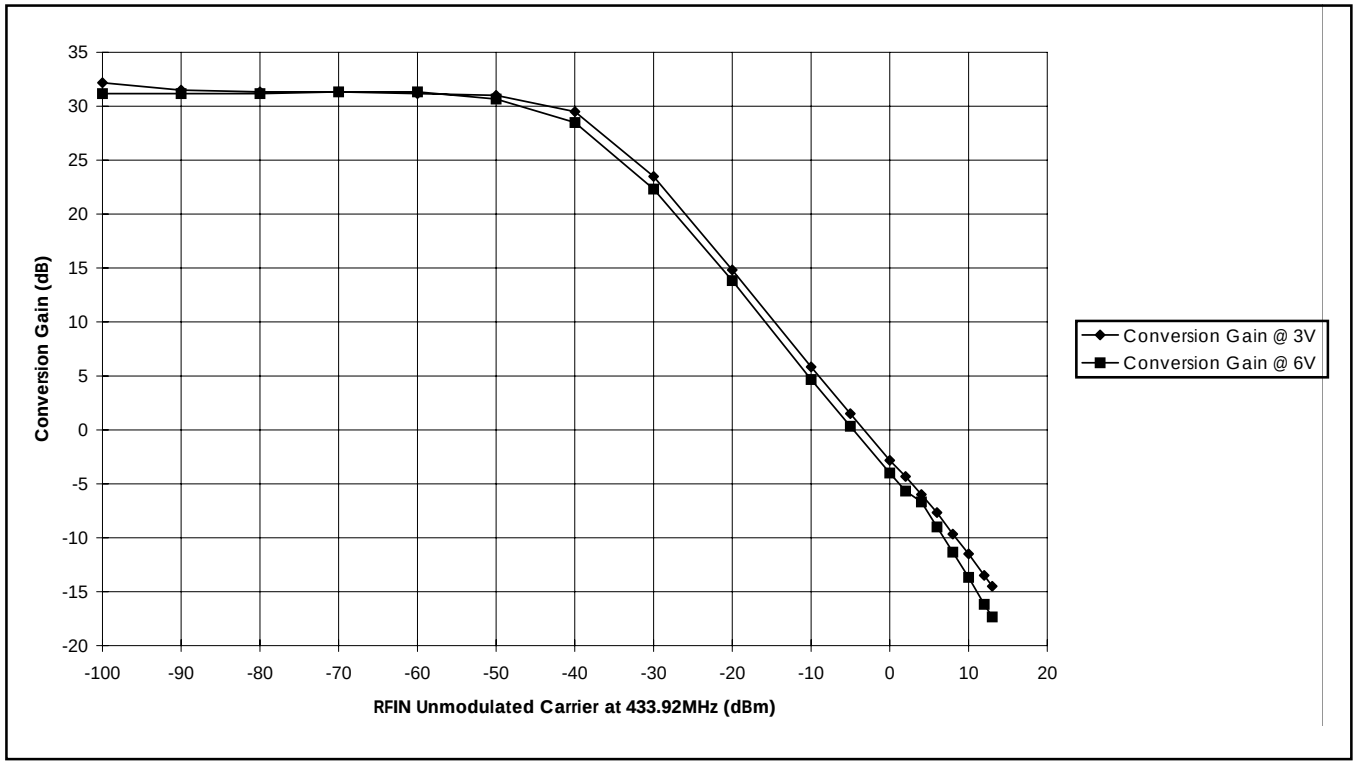


Figure 9a RFIN to IFOUT conversion gain

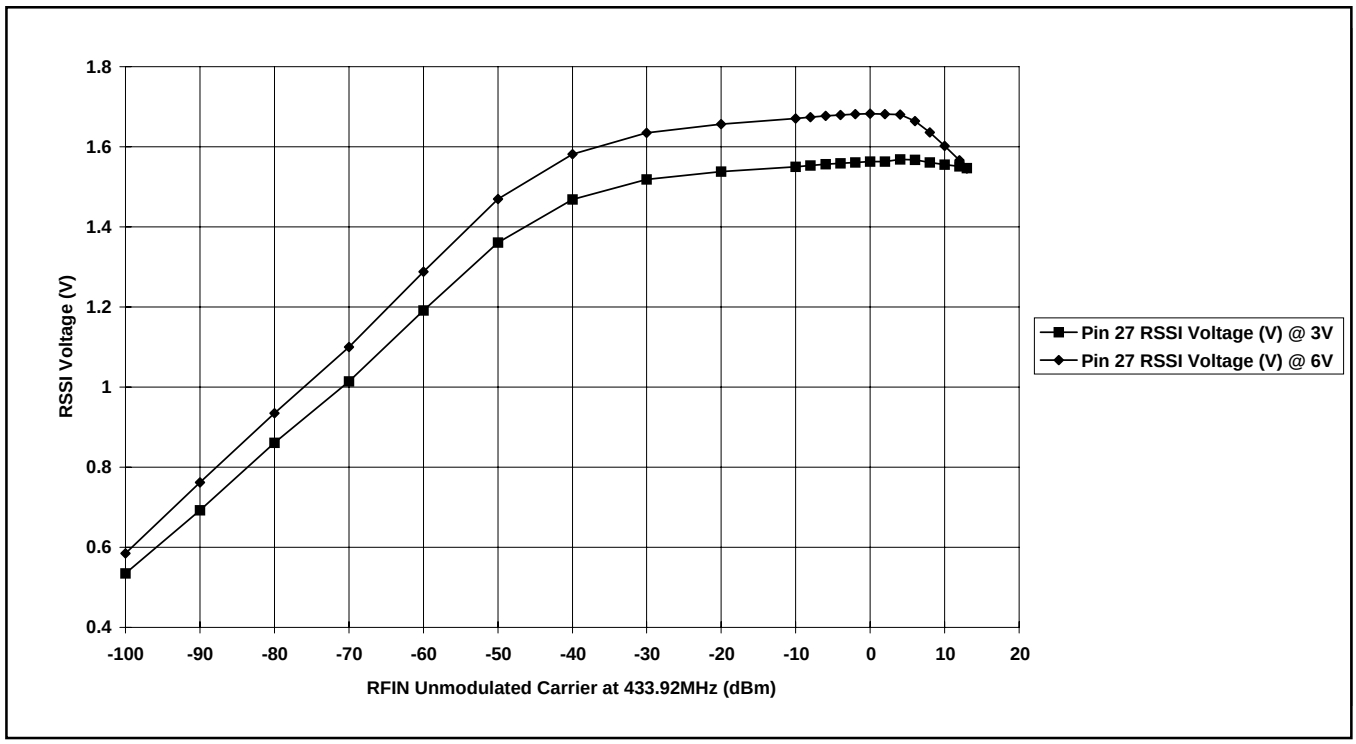


Figure 9b RFIN to RSSI output transfer characteristic

See Notes on page 15

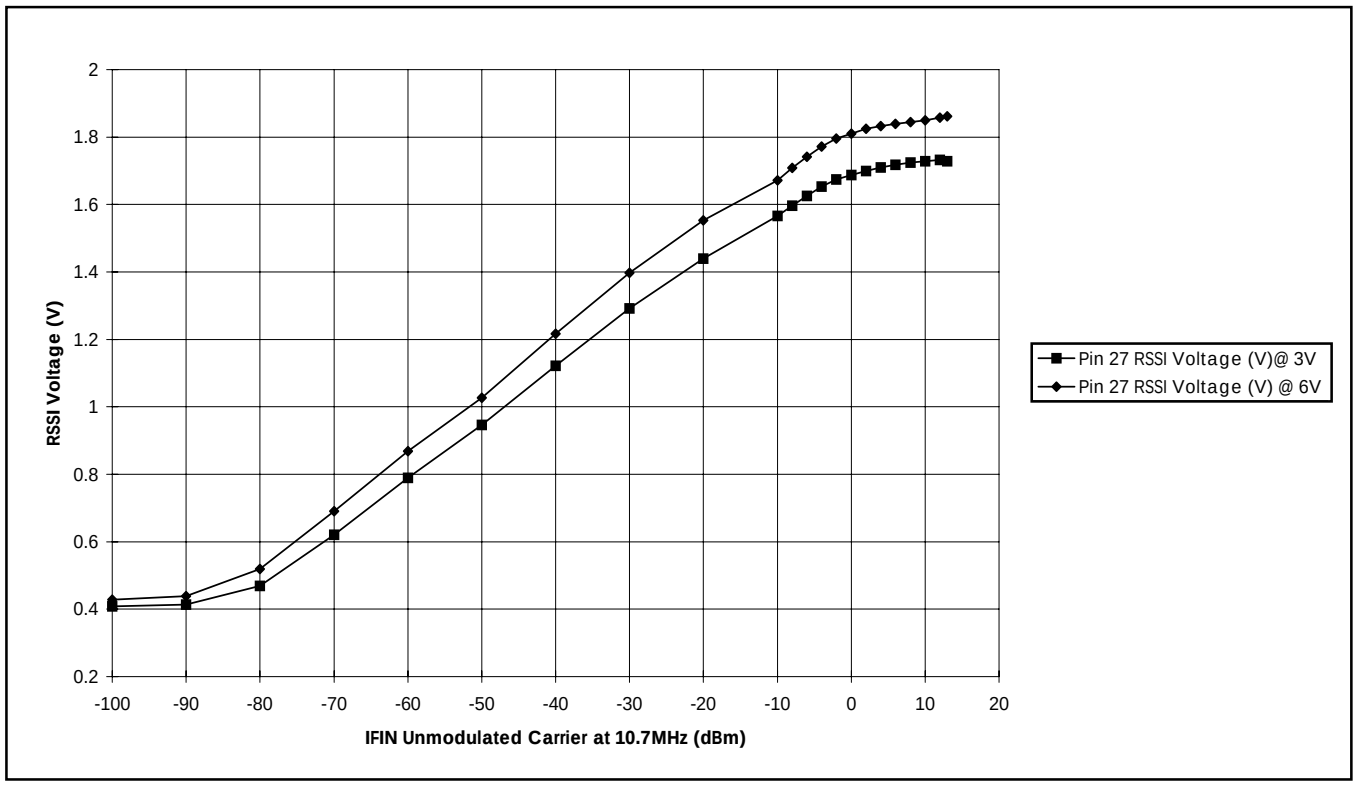


Figure 9c IFIN to RSSI output transfer characteristic

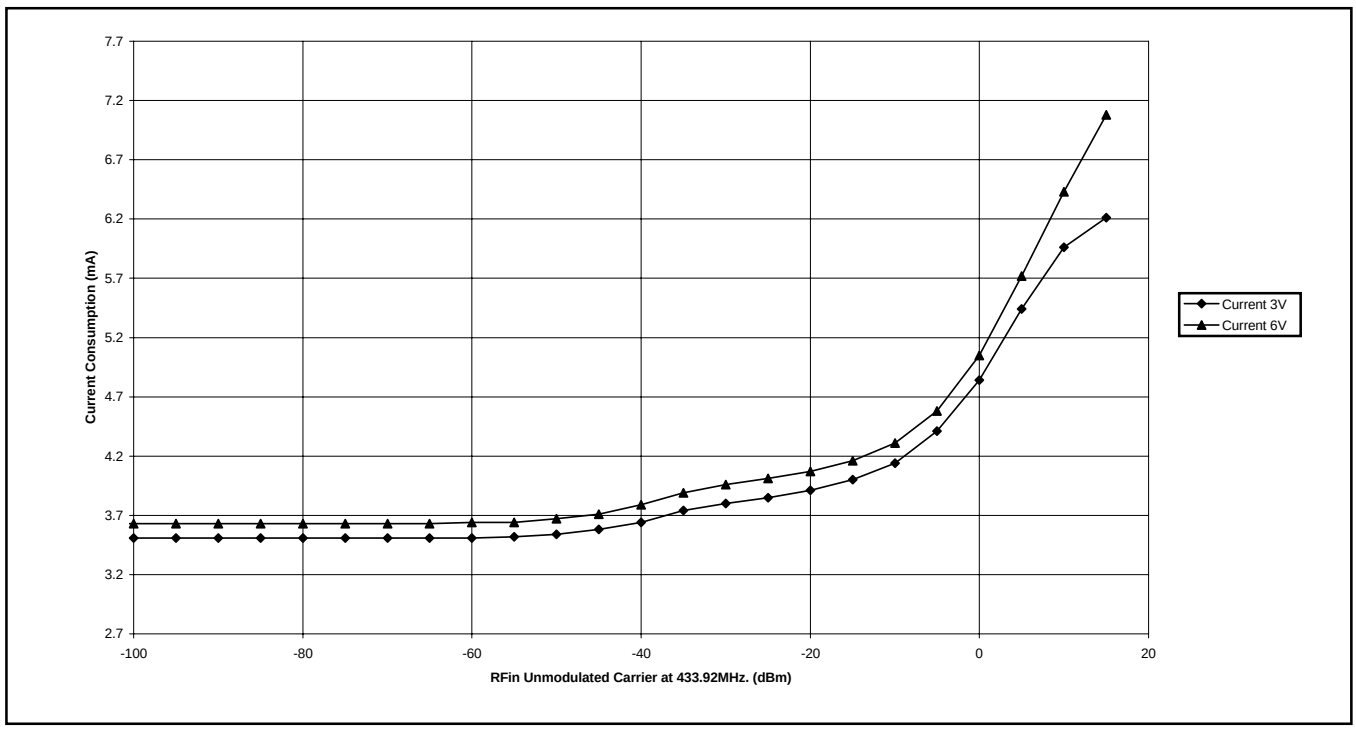


Figure 9d Receiver current consumption V s received signal strength RFIN

Note:

1. Conversion gain of the receiver is limited by the insertion loss of the front end SAW filter.
2. Dynamic range of RSSI output transfer characteristic (Figure 9B) is governed by the noise figure of the receiver, which is limited by the insertion loss of the front end SAW filter, and the bandwidth of the 10.7MHz ceramic filter.
3. Reduction in conversion gain and increase in receiver current consumption coincides with lift-off of the AGC control line (Pin 12). Action of the AGC applies additional mixer booster current to improve the linearity of the mixer at high signal levels.

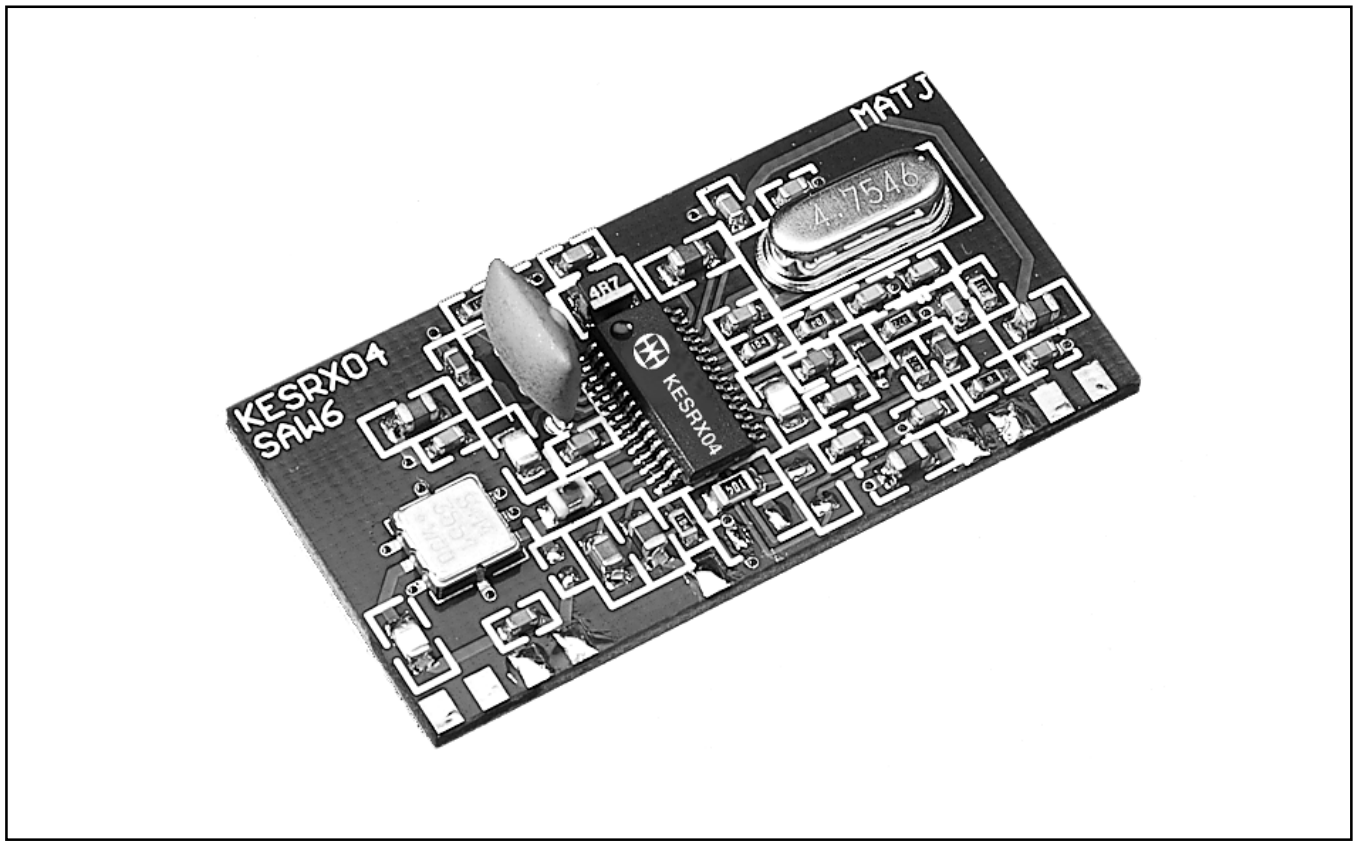


Figure 10 Applications KESRX04 PCB with 10.7MHz IF Ceramic filter
(PCB size = 22mm x 40mm)

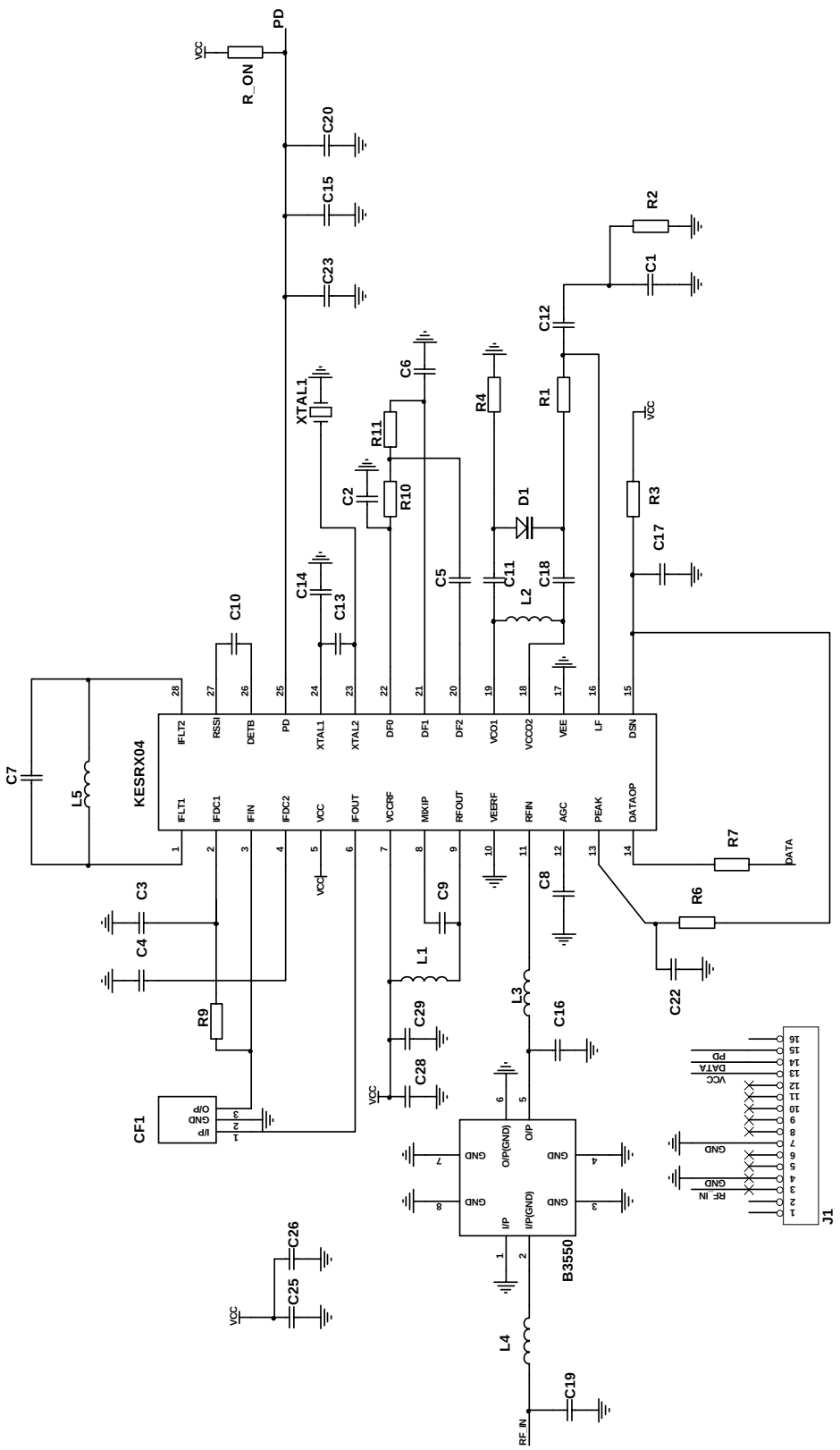


Figure 11 Applications circuits diagram for KESRX04 with 10.7MHz IF

KESRX04

Component list for applications circuit for KESRX04 with 10.7MHz IF (Figure 11)

(Not to be used for Test Fixture Circuit Figure 12) Test fixture component values can be supplied on request.

Identity	433.92 MHz. + SAW	Part No Tolerance	Supplier	Size
C1	150pF	GRM39C0G151J	Murata	0603
C2	270pF	GRM39C0G271J	Murata	0603
C3	10nF	GRM39X7R103K	Murata	0603
C4	10nF	GRM39X7R103K	Murata	0603
C5	270pF	GRM39SL271J	Murata	0603
C6	270pF	GRM39SL271J	Murata	0603
C7**	47pF	GRM39COG470G	Murata	0603
C8	10nF	GRM39Y5V103K	Murata	0603
C9	56pF	GRM39COG560J	Murata	0603
C10	470nF	GRM40Y5V474Z	Murata	0805
C11**	12pF	GRM39COG120J	Murata	0603
C12	1.5nF	GRM39X7R152K	Murata	0603
C13	18pF	GRM39COG180J	Murata	0603
C14	18pF	GRM39COG180J	Murata	0603
C15	82pF	GRM39COG820J	Murata	0603
C16*	N/A	N/A	N/A	N/A
C17	N/A	N/A	N/A	N/A
C18**	12pF	GRM39COG120J	Murata	0603
C19*	6.8pF	GRM39COG6R8C	Murata	0603
C20	N/A	N/A	N/A	N/A
C22	1uF	GRM40Y5V105Z	Murata	0805
C23	82pF	GRM39COG820J	Murata	0603
C25	82pF	GRM39COG820J	Murata	0603
C26	1uF	GRM40Y5V105Z	Murata	0805
C28	1uF	GRM40Y5V105Z	Murata	0805
C29	82pF	GRM39COG820J	Murata	0603
R1	4.7K	N/A	Rohm	0603
R2	10K	N/A	Rohm	0603
R3	N/A	N/A	N/A	N/A
R4	4.7K	N/A	Rohm	0603
R6	100K	N/A	Rohm	0805
R7	100K	N/A	Rohm	0603
R9**	360	N/A	Rohm	0603
R10	100K	N/A	Rohm	0603
R11	100K	N/A	Rohm	0603
R_ON	N/A	N/A	N/A	N/A
D1	BB833	4 to 10pF	Siemens	SOD323
CF1**	SFE10.7MA26	3dB BW = 470KHz.	Murata	Radial
B355*	B3550	3dB BW = 750KHz.	Siemens	$5mm^2$
L1*	39nH	LL2012-F39NJ	TOKO	2012
L2*	27nH	LL2012-F27NJ	TOKO	2012
L3*	100nH	LL1608-FHR10J	TOKO	1608
L4*	33nH	LL2012-F33NJ	TOKO	2012
L5**	4.7uH	FLU25204R7J	TOKO	2520
XTAL1*	6.61281MHz.	+/-100 PPM	Kinseki / Quartz Tek	HC49/4H
KESRX04	KESRX04	KESRX04	Zarlink Semiconductor	QP28

*Adjust for alternative centre frequency.

**Adjust for alternative IF frequency / ceramic filter.

AGC time constant (C8) optimised for minimum settling time (time to good) data

N/A. Not Applicable

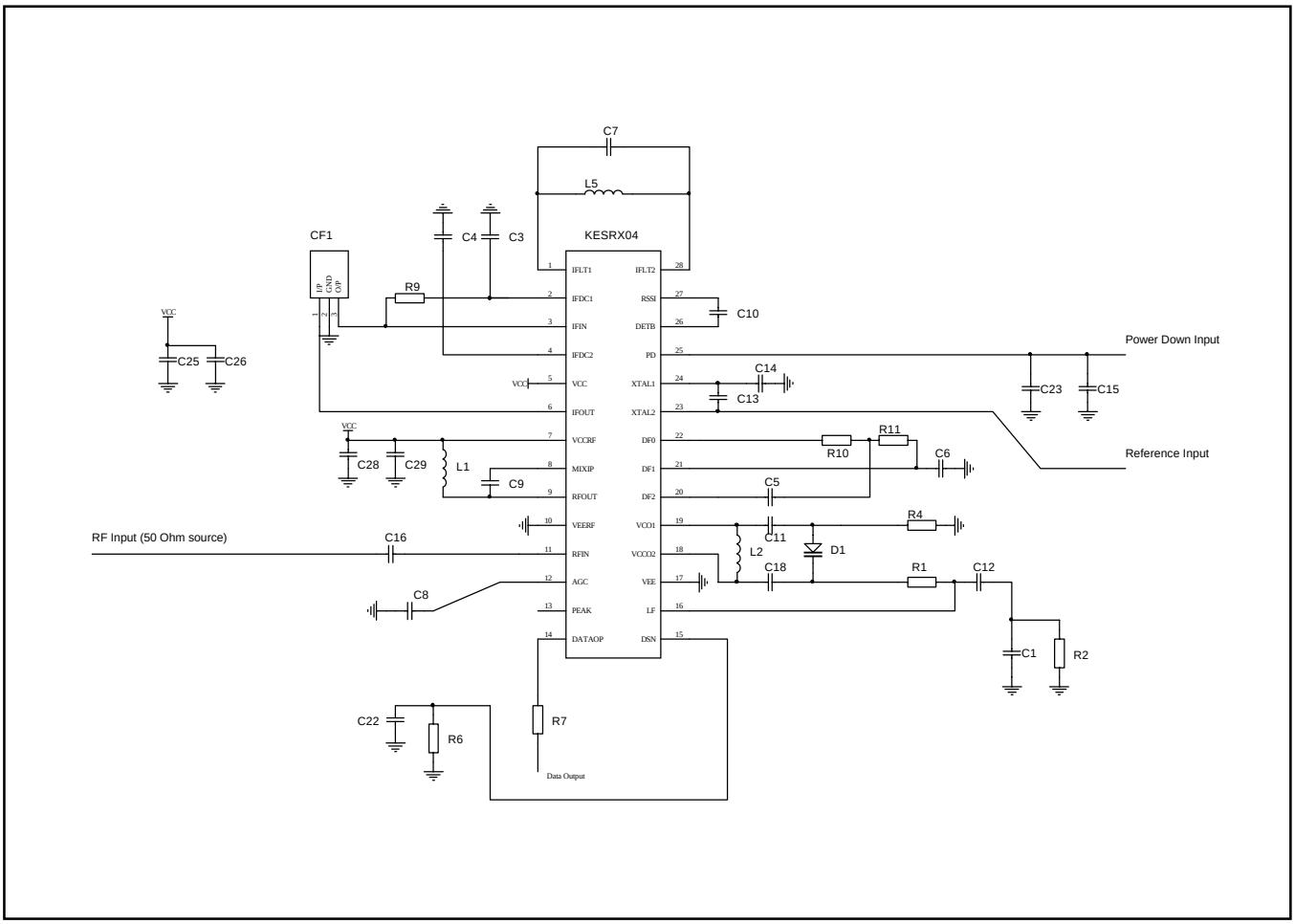
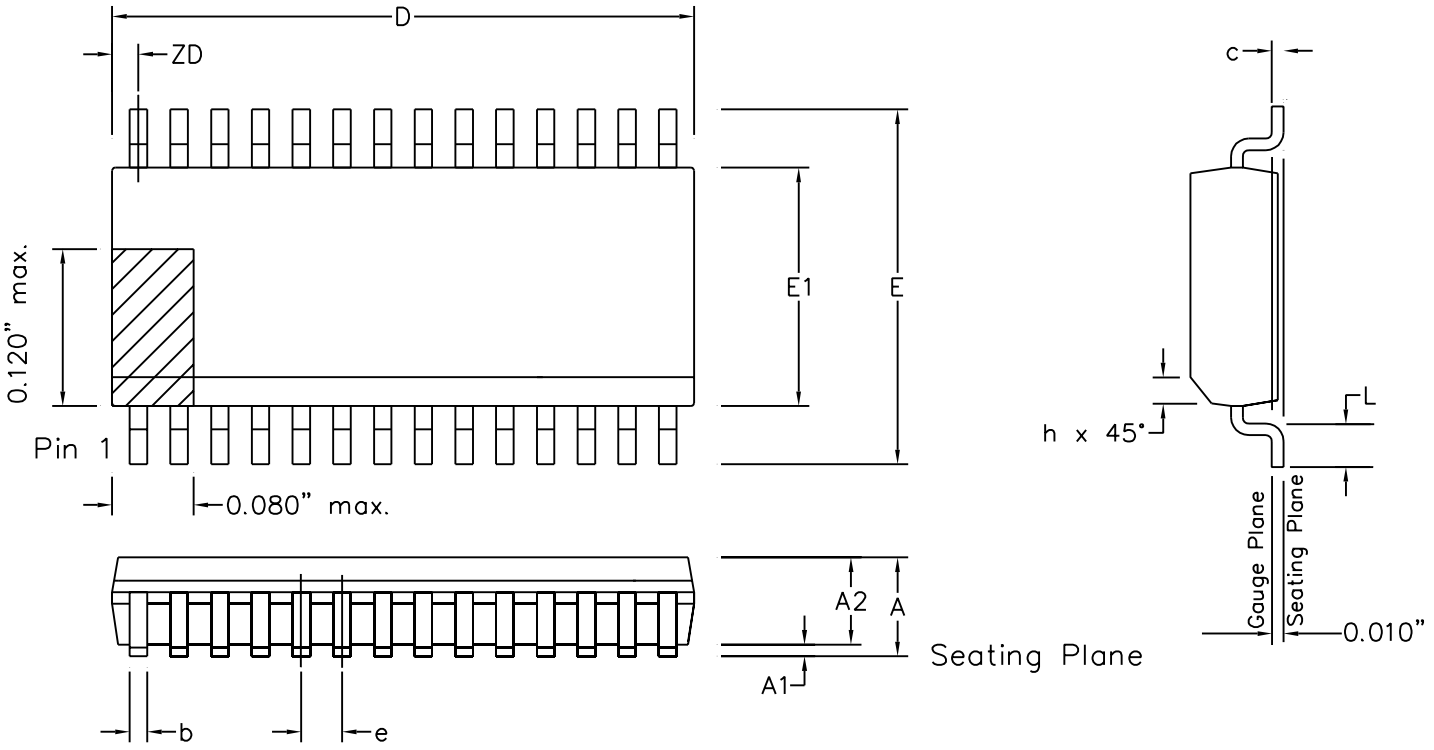


Figure 12 Production test circuit for KESRX04 with 10.7MHz IF



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.386	0.394	9.80	10.01
ZD	0.033 REF.		0.84 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	28			
Conforms to JEDEC MO-137AF Iss. A				

This drawing supersedes
418/ED/51617/004 (Swindon/Plymouth)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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ZARLINK SEMICONDUCTOR

Previous package codes
QP / Q

Package Code DG

Package Outline for 28 lead QSOP (0.150" Body Width)

GPD00292



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