6AM13

Silicon N Channel/P Channel Complementary Power MOS FET Array

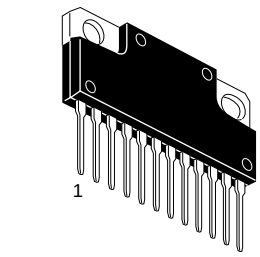
Application

High speed power switching

Features

- Low on-resistance
  N-channel: R_{DS} (on) ≤ 0.075 Ω, V_{GS} = 10 V
  I_D = 5 A
  P-channel: R_{DS} (on) ≤ 0.12 Ω, V_{GS} = –10 V
  I_D = –5 A
- Capable of 4 V gate drive
- Low drive current
- Hight speed switching
- High density mounting
- Suitable for H-bridged motor driver
- Discrete packaged devices of same die
  N-channel: 2SK971 (TO-220AB),
  2SK1094 (TO-220FM)
  P-channel: 2SJ173 (TO-220AB),
  2SJ176 (TO-220FM)

SP-12TA



1 : Nch Source
2, 8, 9 : Nch Gate
3, 7,10 : Nch Drain
: Pch Drain
4, 6,11 : Pch Gate
5, 12 : Pch Source

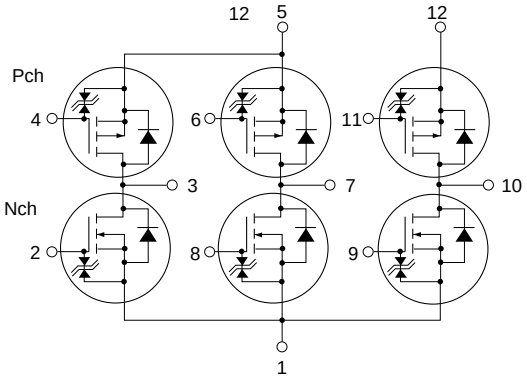


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	10	–10	A
Drain peak current	$I_{D(pulse)}$*	40	–40	A
Body–drain diode reverse drain current	I_{DR}	10	–10	A
Channel dissipation	Pch (Tc =25°C)**	42		W
Channel dissipation	Pch**	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 6 devices operation

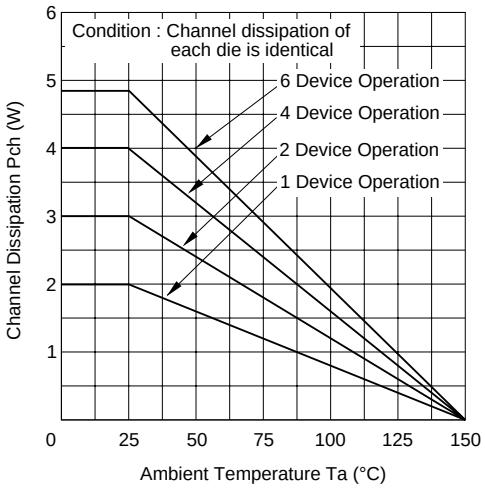
Table 2 Electrical Characteristics (Ta = 25°C) (1 Unit)

Item	Symbol	N channel			P channel			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.075	—	0.09	0.12	Ω	I_D = 5 A, V_{GS} = 10 V *
		—	0.08	0.11	—	0.12	0.18	Ω	I_D = 5 A, V_{GS} = 4 V *
Forward transfer admittance	|yfs|	6	9.5	—	5	8	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	—	1400	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	450	—	—	720	—	pF	
Reverse transfer capacitance	Crss	—	140	—	—	220	—	pF	
Turn–on delay time	$td_{(on)}$	—	10	—	—	15	—	ns	I_D = 5 A, V_{GS} = 10 V, R_L = 6 Ω
Rise time	tr	—	50	—	—	100	—	ns	
Turn–off delay time	$td_{(off)}$	—	180	—	—	250	—	ns	
Fall time	tf	—	110	—	—	160	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	—	–1.0	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	120	—	—	200	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

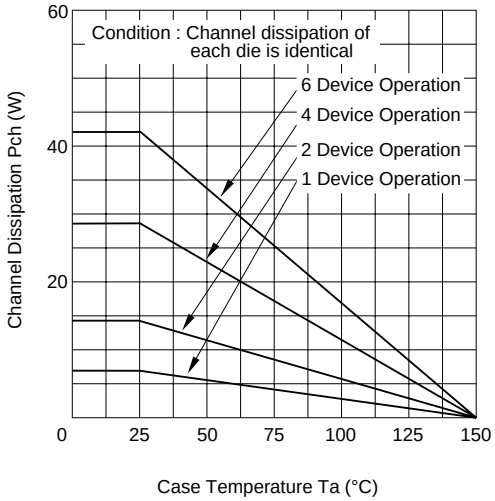
* Pulse Test
Note: Polarity of test conditions for P channel device is reversed.

■ Nch : See characteristic curves of 2SK971
■ Pch : See characteristic curves of 2SJ173

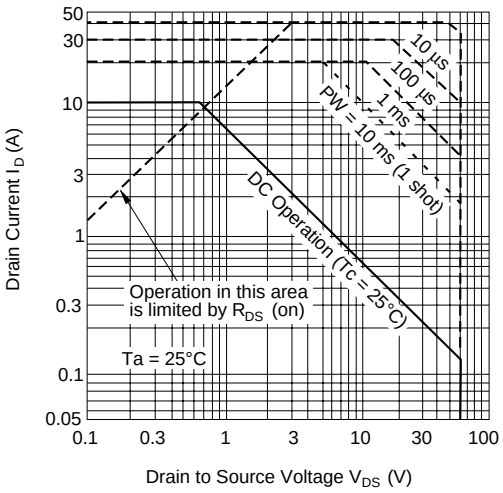
Maximum Channel Dissipation Curve



Maximum Channel Dissipation Curve



Maximum Safe Operation Area (N-channel)



Maximum Safe Operation Area (P-channel)