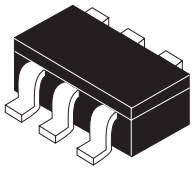
KBMFxxSC6

A.S.D.™

EMI FILTER AND LINE TERMINATION FOR PS/2 MOUSE OR KEYBOARD PORTS

MAIN APPLICATION

EMI Filter and line termination for mouse and keyboard ports on:
- Desktop computers
- Notebooks
- Workstations
- Servers



SOT23-6L

DESCRIPTION

On the implementation of computer systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of EMC compatibility, the computing devices are required to tolerate ESD events and remain operational without user intervention.

The KBMF implements a low pass filter to limit EMI levels and provide ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device also implements the pull up resistors needed to bias the data and clock lines. The package is the SOT23-6L which is ideal for situations where board space is at a premium.

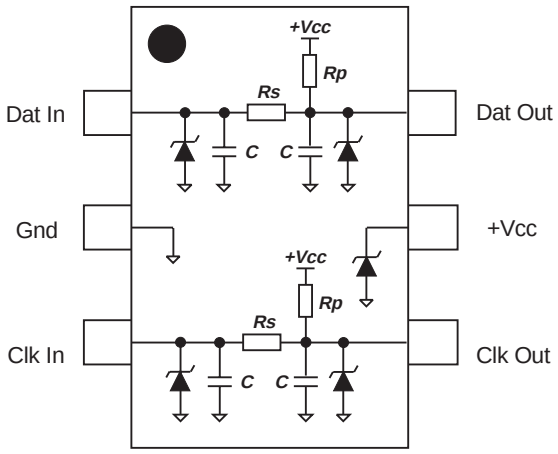
FEATURES

- Integrated low pass filters for Data and Clock lines
- Integrated ESD protection
- Integrated pull-up resistors
- Small package size
- Breakdown voltage: V_{BR} = 6V min

BENEFITS

- EMI / RFI noise suppression
- ESD protection exceeding IEC61000-4-2 level 4
- High flexibility in the design of high density boards

FUNCTIONAL DIAGRAM



	Rs	Rp	C
code 01	39Ω	4.7kΩ	120pF
Tolerance	±10%	±10%	±20%

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COMPLIES WITH THE FOLLOWING ESD STANDARDS:

IEC 61000-4-2 (R = 330Ω C = 150pF), level 4
±15 kV (air discharge)
±8 kV (contact discharge)

MIL STD 883C, Method 3015-6
Class 3 C = 100 pF R = 1500 Ω
3 positive strikes and 3 negative strikes (F = 1 Hz)

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge R = 330Ω C = 150pF contact discharge ESD discharge - MIL STD 883 - Method 3015-6	±12 ±25	kV kV
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	- 55 to +150	°C
T_L	Lead solder temperature (10 second duration)	260	°C
T_{op}	Operating temperature Range	0 to 70	°C
P_r	Power rating per resistor	100	mW

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
I_R	Diode leakage current	V_{RM} = 5.0V			10	µA
V_{BR}	Diode breakdown voltage	I_R = 1mA	6			V
V_F	Diode forward voltage drop	I_F = 50mA		0.9		V

TECHNICAL INFORMATION

EMI FILTERING

The KBMFxxSC6 ensure a filtering protection against ElectroMagnetic and RadioFrequency Interferences thanks to its low-pass filter structure. This filter is characterized by the following parameters :

- cut-off frequency
- Insertion loss
- high frequency rejection

Fig. A1: Measurements configuration

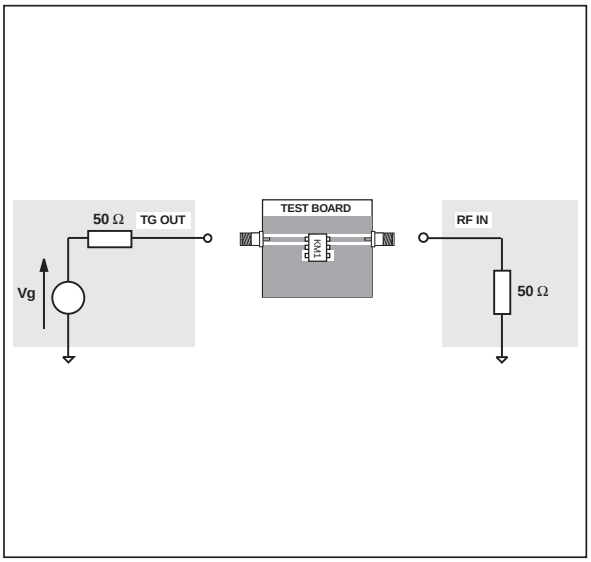
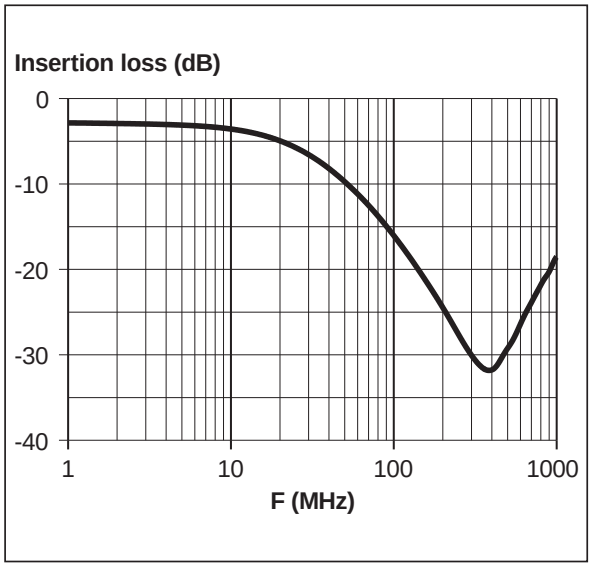


Fig. A2: KBMFxxSC6 attenuation curve



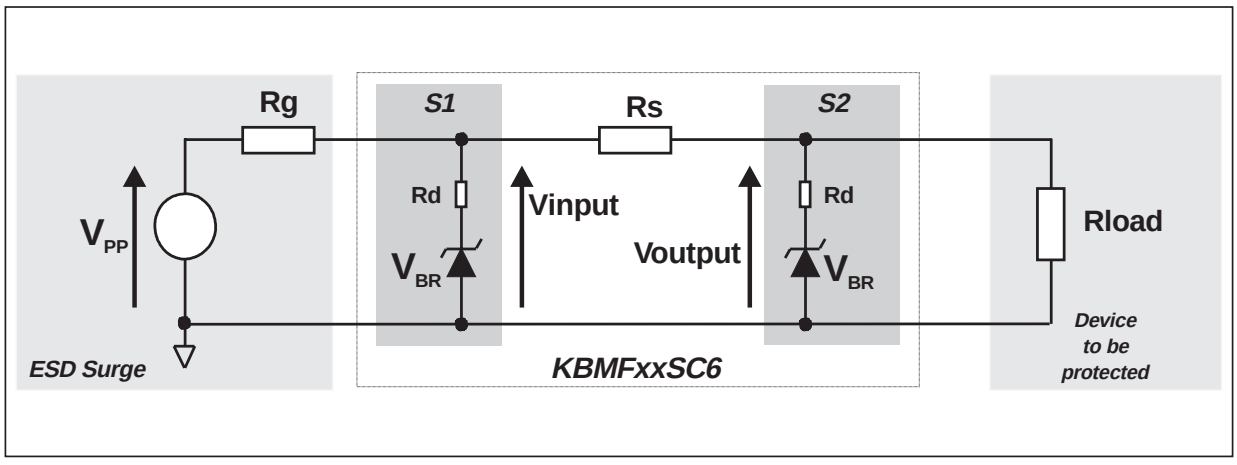
ESD PROTECTION

The KBMFxxSC6 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at :

$$Vouput = V_{BR} + R_d.I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure A3, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the Voutput level.

Fig. A3: ESD clamping behavior



To have a good approximation of the remaining voltages at both Vinput and Voutput stages, we give the typical dynamical resistance value Rd. By taking into account these following hypothesis : Rt>Rd, Rg>Rd and Rload>Rd, it gives these formulas:

$$Vinput = \frac{R_g.V_{BR} + R_d.V_g}{R_g}$$

$$Voutput = \frac{R_S.V_{BR} + R_d.Vinput}{R_t}$$

The results of the calculation done for V_{PP}=8kV, Rg=330Ω (IEC 61000-4-2 standard), Vbr=7V (typ.) and Rd = 1ohm (typ.) give:

Vinput = 31.2 V

Voutput = 7.8 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the input side. This parasitic effect is not present at the output side due the low current involved after the resistance R_S.

The measurements done here after show very clearly (Fig. A5) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on output stage
- Voutput clamping voltage very close to Vbr (positive strike) and -Vf (negative strike)

Fig. A4: Measurement conditions

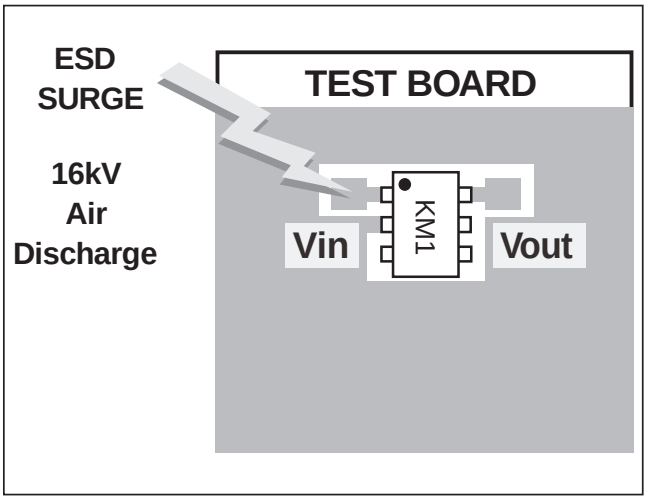
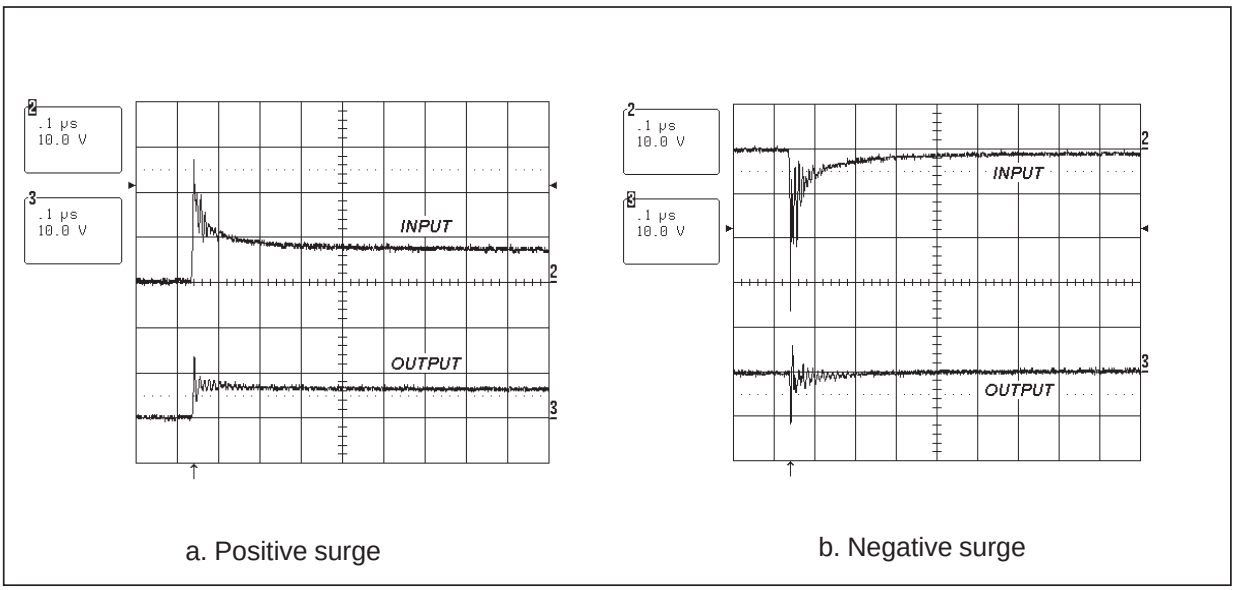


Fig. A5: Remaining voltage at both stages S1 (Vinput) and S2 (Voutput) during ESD surge.



a. Positive surge

b. Negative surge

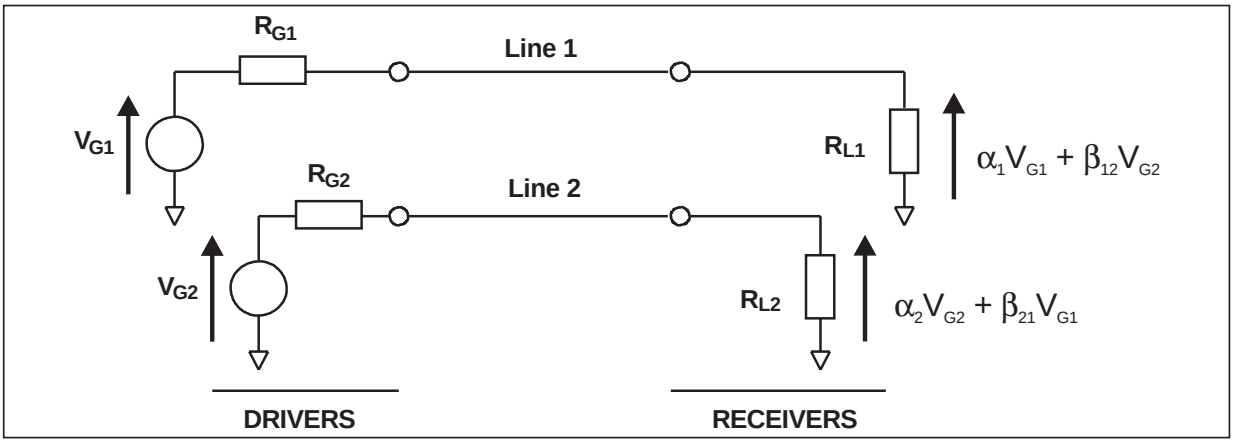
Please note that the KBMFxxSC6 is not only acting for positive ESD surges but also for negative ones. For these kind of disturbances it clamps close to ground voltage as shown in Fig. A5b.

LATCH-UP PHENOMENA

The early ageing and destruction of IC's is often due to latch-up phenomena which is mainly induced by dV/dt. Thanks to its structure, the KBMFxxSC6 provides a high immunity to latch-up phenomena by smoothing very fast edges.

CROSSTALK BEHAVIOR

Fig. A6: Crosstalk phenomena



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, this is the reason why we provide crosstalk measurements for monolithic device to guarantee negligeable crosstalk between the lines. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Fig. A7: Analog Crosstalk measurements configuration

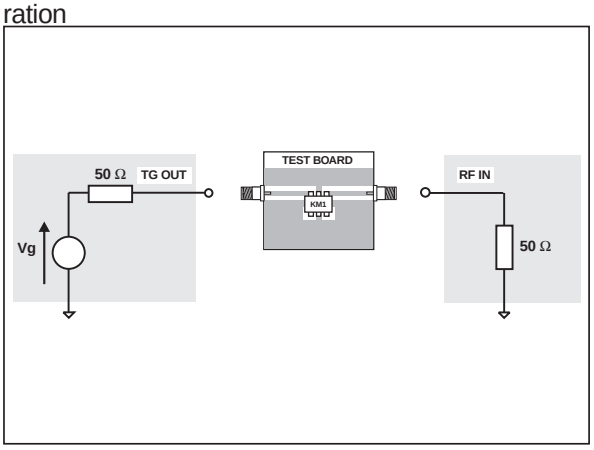


Fig. A8: Typical Analog Crosstalk measurement

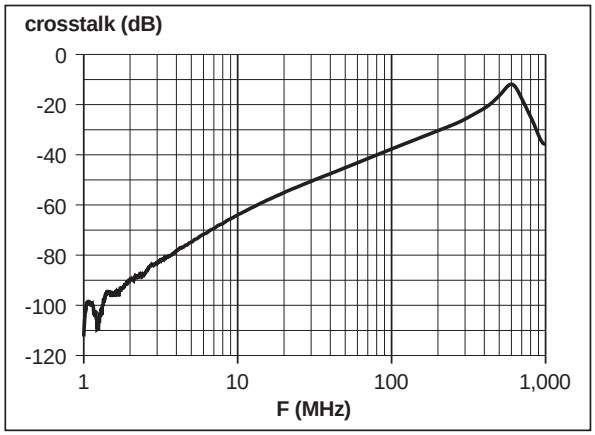


Figure A7 gives the measurement circuit for the analog crosstalk application. In figure A8, the curve shows the effect of the Data line on the CLK line. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -37dB.

Fig. A9: Digital crosstalk measurements configuration

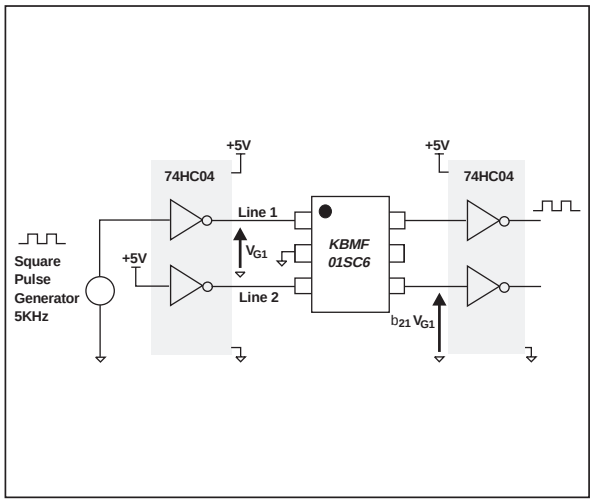


Fig. A10: Digital crosstalk measurements

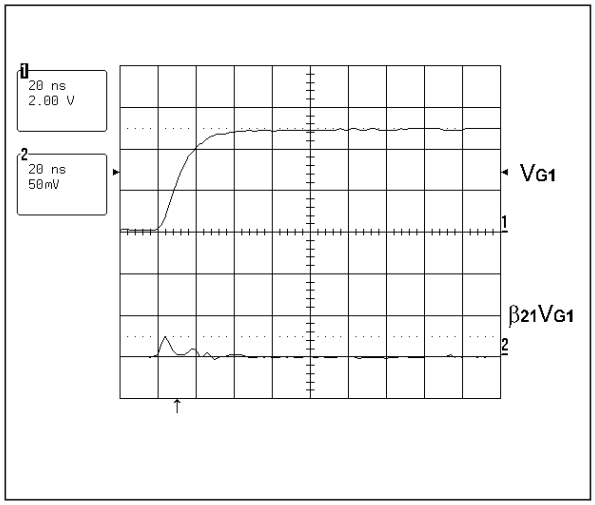
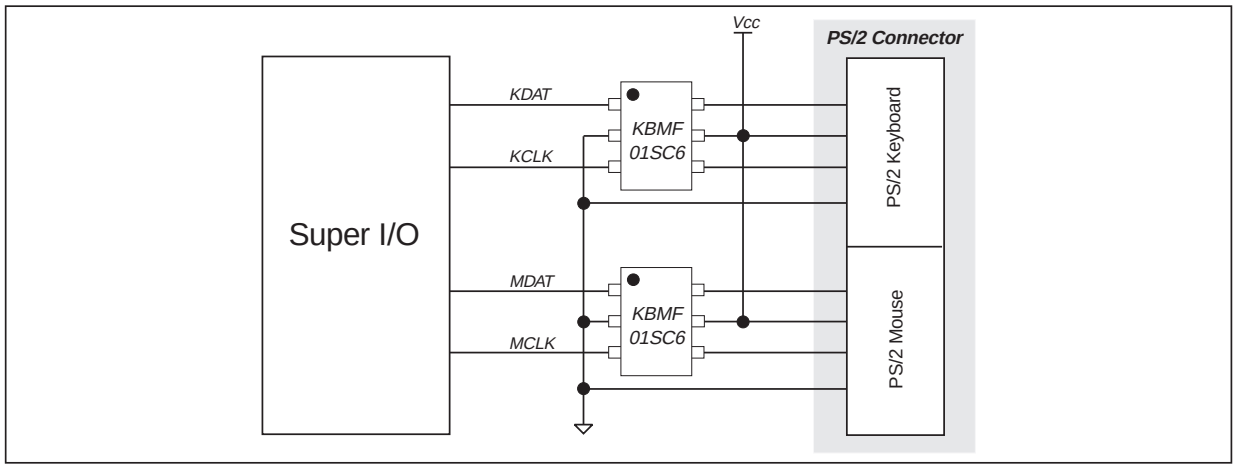


Figure A9 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A10 shows that in such a condition signal from 0 to 5V and rise time of few ns, the impact on the other line is less than 50mV peak to peak. (Below the logic high threshold voltage).The measurements performed with falling edges gives the results within the same range.

APPLICATION EXAMPLE

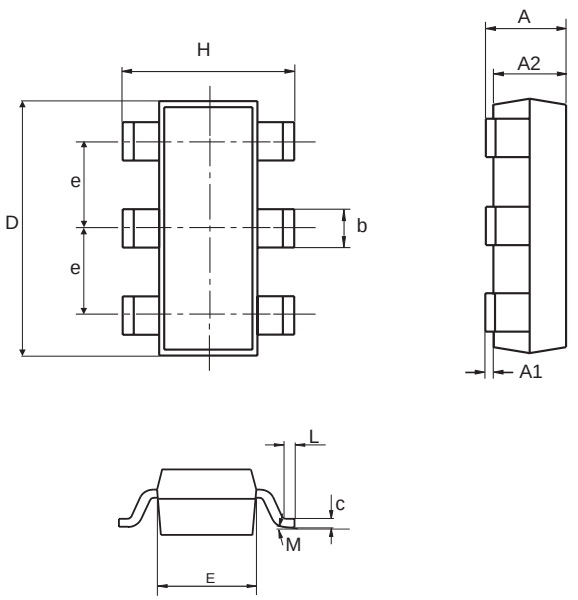
Fig. A11: Implementation of KBMFxxSC6 in a typical application



The KBMFxxSC6 device could be used on PS/2 mouse or keyboard as indicated by figure A11.

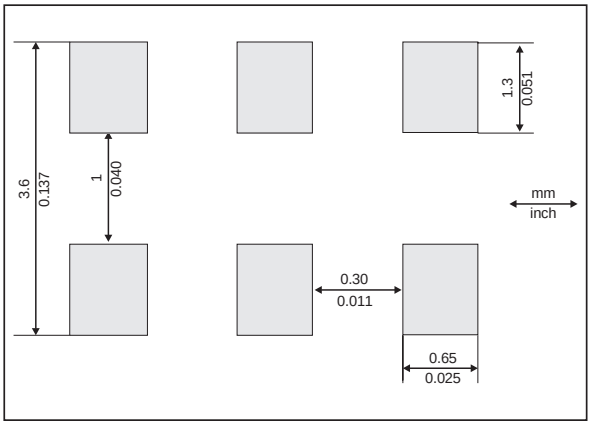
PACKAGE MECHANICAL DATA.

SOT23-6L



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.45	0.035	0.057
A1	0	0.15	0	0.006
A2	0.90	1.30	0.035	0.0512
b	0.35	0.50	0.0137	0.02
C	0.09	0.20	0.004	0.008
D	2.80	3.00	0.11	0.118
E	1.50	1.75	0.059	0.0689
e	0.95 Typ.		0.0374 Typ.	
H	2.60	3.00	0.102	0.118
L	0.10	0.60	0.004	0.024
M		10°		10°

RECOMMENDED FOOTPRINT (mm)



MECHANICAL SPECIFICATIONS

Lead plating	Tin-lead
Lead plating thickness	5µm min 25µm max
Lead material	Sn / Pb (70% to 90%Sn)
Lead coplanarity	10µm max
Body material	Molded epoxy
Flammability	UL94V-0

MARKING

Type	Order Code	Weight	Marking	Package	Base Qty
KBMF01SC6	KBMF01SC6	16.7mg	KM1	SOT23-6L	3000