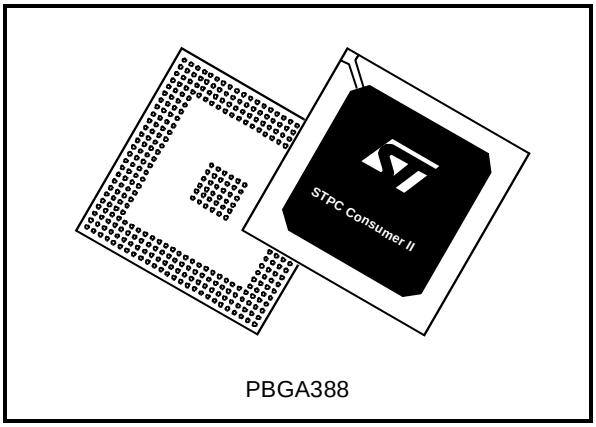
STPC® CONSUMER-II

X86 Core PC Compatible Information Appliance System-on-Chip

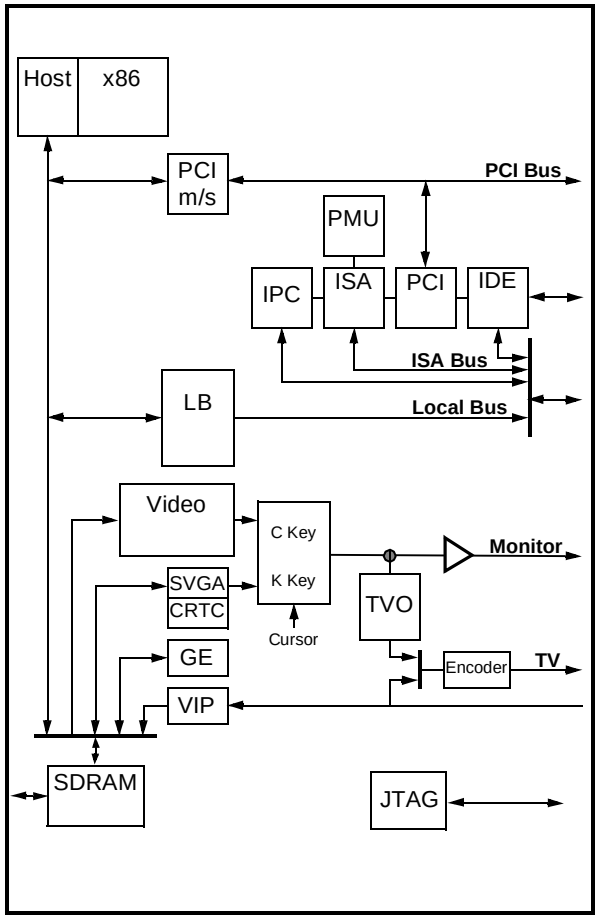
ADVANCED DATA

- POWERFUL x86 PROCESSOR
- 64-BIT SDRAM UMA CONTROLLER
- VGA & SVGA CRT CONTROLLER
- 135MHz RAMDAC
- 2D GRAPHICS ENGINE
- VIDEO INPUT PORT
- VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- TV OUTPUT
  - 3-LINE FLICKER FILTER
  - CCIR 601/656 SCAN CONVERTER
  - NTSC / PAL COMPOSITE, RGB, S-VIDEO
- PCI MASTER / SLAVE / ARBITER
- ISA MASTER / SLAVE
- OPTIONAL 16-BIT LOCAL BUS INTERFACE
- EIDE CONTROLLER
- I²C INTERFACE
- IPC
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- JTAG IEEE1149.1



PBGA388

Figure 0-1. Logic Diagram



DESCRIPTION

The STPC Consumer-II integrates a standard 5th generation x86 core, a Synchronous DRAM controller, a graphics subsystem, a video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single consumer orientated PC compatible subsystem on a single device.
The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing memory between the CPU, the graphics and the video.

The STPC Consumer-II is packaged in a 388 Plastic Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Runs up to 100MHz (x1) or 133 MHz (x2).
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5V operation.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 100MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 2MB up to 128 MB system memory.
- Supports 16-, 64-, and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non buffered, and registered DIMMs
- 4-line write buffers for CPU to SDRAM and PCI to SDRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.

- **2D Graphics Controller**
- 64-bit windows accelerator.
- Backward compatibility to SVGA standards.
- Hardware acceleration for text, bitblts, transparent blts and fills.
- Up to 64 x 64 bit graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8-, 16-, 24- and 32-bit pixels.
- Drivers availables for various OSes.

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- Requires external frequency synthesizer and reference sources.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.
- Requires no external frequency synthesizer.
- Requires only external reference source.

- **Video Input port**
- Accepts video inputs in CCIR 601 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- Video pass through to the TV output for full screen video images.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.

- **Video Output**
- NTSC-M; PAL-B, D, G, H, I, M, N encoding.
- 4 analog outputs in two configurations:
  - R,G,B + CVBS
  - C,YS,CVBS1 + CVBS2
- Flicker-free interlaced output.
- Programmable two tap filter with gamma correction or three tap flicker filter.
- Interlaced or non-interlaced operation mode.
- Progressive to interlaced scan converter.
- Cross color reduction by specific trap filtering on luma within CVBS flow.
- Power down mode available on each DAC.

- **PCI Controller**
- Fully compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 cpu bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 22-bit address bus.
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 2 Programmable Flash Chip Select.
- 4 Programmable I/O Chip Select.
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 16MB flash devices with boot block shadowed to 0x000F0000.

- **IDE Interface**
- Supports PIO
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
- Support for PIO mode 3 & 4.
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).
- Drivers for Windows and other Operating Systems

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.