DATA SHEET

74ABT845

8-bit bus interface latch with set and reset (3-State)

Product data
Supersedes data of 1995 Sep 06

2002 Dec 17

Philips
Semiconductors

PHILIPS

8-bit bus interface latch with set and reset (3-State)

74ABT845

FEATURES

- High speed parallel latches
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Broadside pinout
- Output capability: +64 mA / –32 mA
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT845 consists of eight D-type latches with 3-State outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 74ABT845 has two additional $\overline{OE}$ pins, making a total of three Output Enable ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) pins. The multiple Output enables allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

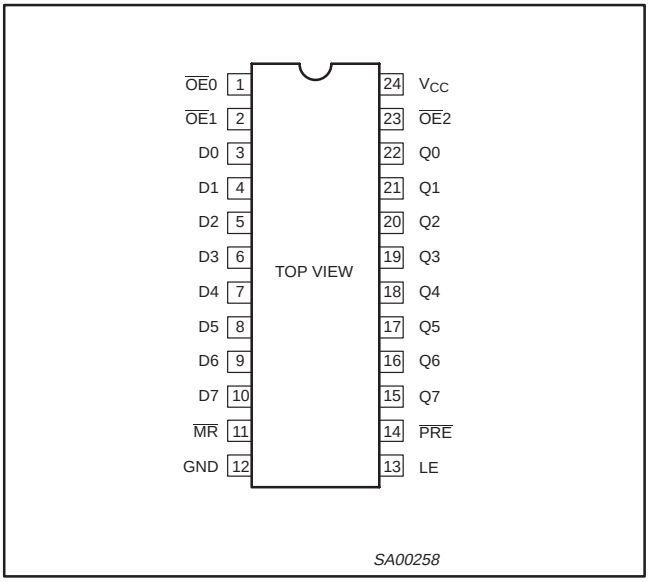
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50 pF; V_{CC} = 5 V	5.4	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
24-Pin Plastic DIP	–40 °C to +85 °C	74ABT845N	SOT222-1
24-Pin Plastic SSOP Type II	–40 °C to +85 °C	74ABT845DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74ABT845PW	SOT355-1

PIN CONFIGURATION



SA00258

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 23	$\overline{OE}0$ – $\overline{OE}2$	Output enable inputs (active-LOW)
3, 4, 5, 6, 7, 8, 9, 10	D0 – D7	Data inputs
22, 21, 20, 19,18, 17, 16, 15	Q0 – Q7	Data outputs
11	$\overline{MR}$	Master reset input (active-LOW)
13	LE	Latch enable input (active-HIGH)
14	$\overline{PRE}$	Preset input (active-LOW)
12	GND	Ground (0 V)
24	V_{CC}	Positive supply voltage

8-bit bus interface latch with set and reset (3-State)

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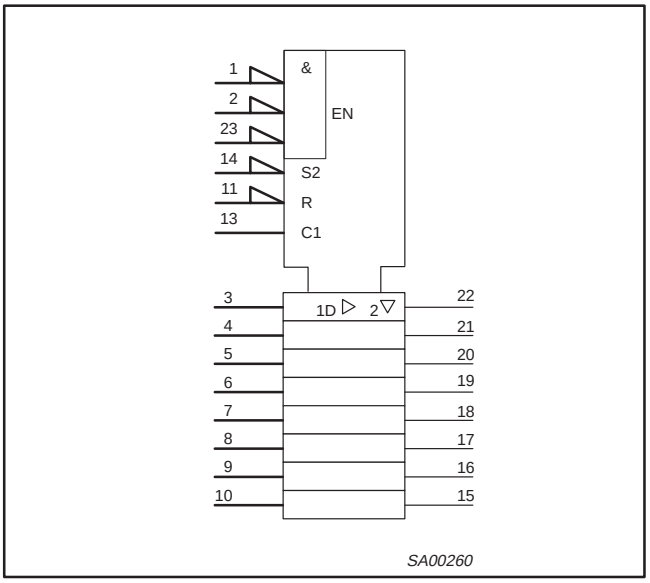
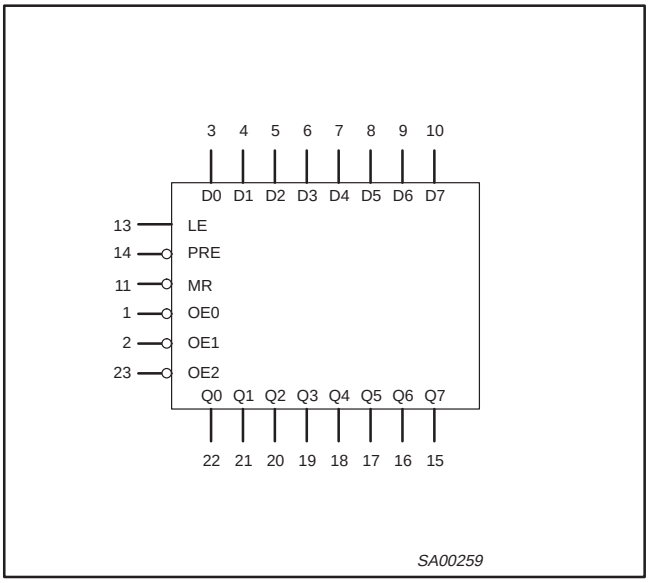
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

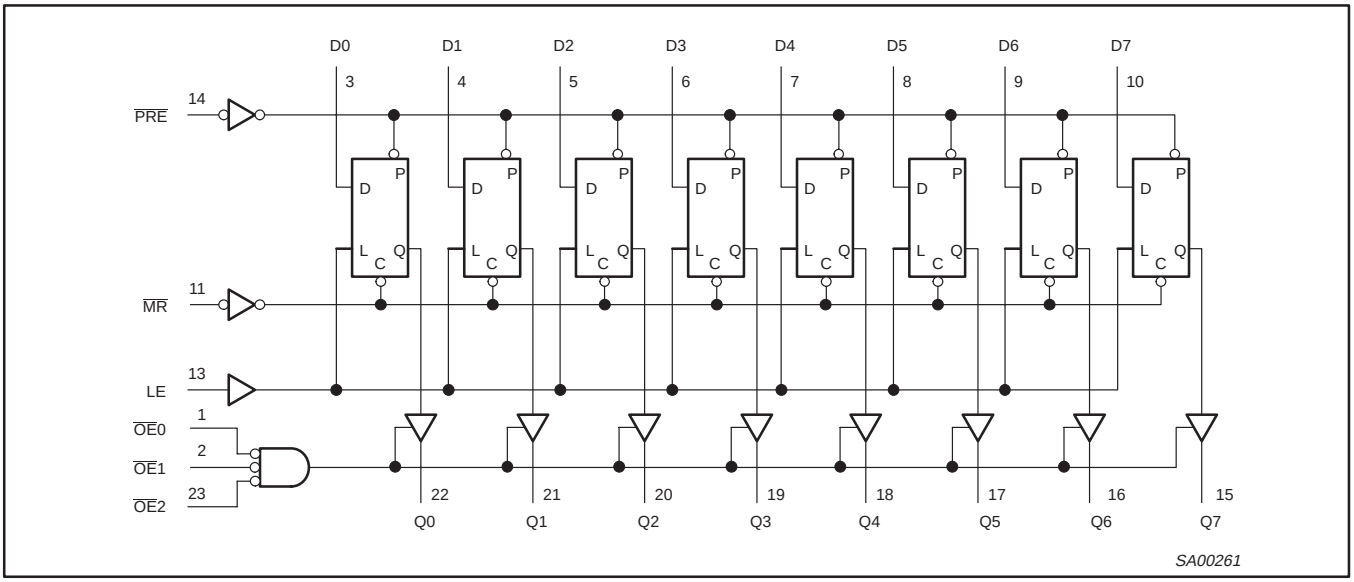


FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}n$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the HIGH-to-LOW LE transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = HIGH-to-LOW transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		–0.9	–1.2		–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O or $V_I \leq$ 4.5 V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-state output current[4]	V_{CC} = 2.1 V; V_O = 0.5 V; $V_{\overline{OE}}$ = V_{CC}; V_I = GND or V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs HIGH, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5 V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. For V_{CC} = 2.1 V to V_{CC} = 5 V ± 10%, a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	1	1.0 2.2	3.9 5.4	5.4 6.8	1.0 2.2	6.2 7.8	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	2	2.0 2.8	5.1 6.4	6.6 7.9	2.0 2.8	7.5 8.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PRE}$ to Qn	1	2.2 3.0	4.9 5.3	6.6 6.8	2.2 3.0	7.8 7.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Qn	1	2.4 3.1	4.9 5.9	6.4 7.3	2.4 3.1	7.3 8.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Qn	4 5	1.0 2.0	3.8 4.7	5.4 6.1	1.0 2.0	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Qn	4 5	1.9 2.2	4.6 4.7	6.2 6.4	1.9 2.2	7.2 7.0	ns

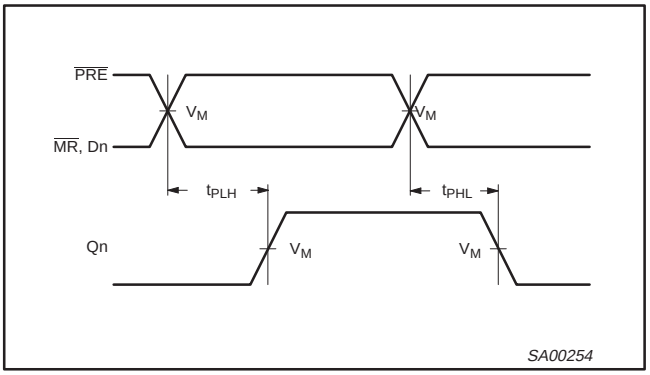
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

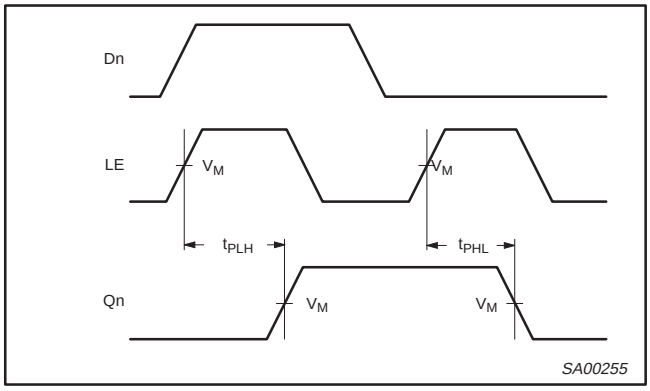
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V		T_{amb} = –40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V	
			Min	Typ	Min	
t_s(H) t_s(L)	Set-up time, HIGH or LOW Dn to LE	3	2.8 3.5	1.0 1.4	2.8 3.5	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW Dn to LE	3	1.0 1.0	–1.2 –0.6	1.0 1.0	ns
t_w(H)	LE pulse width, HIGH	3	3.0	1.5	3.0	ns
t_w(L)	$\overline{PRE}$ pulse width, LOW	6	3.5	2.0	3.5	ns
t_w(L)	$\overline{MR}$ pulse width, LOW	6	2.8	1.3	2.8	ns
t_{rec}	$\overline{PRE}$ recovery time	6	3.0	1.4	3.0	ns
t_{rec}	$\overline{MR}$ recovery time	6	3.4	1.6	3.4	ns

AC WAVEFORMS

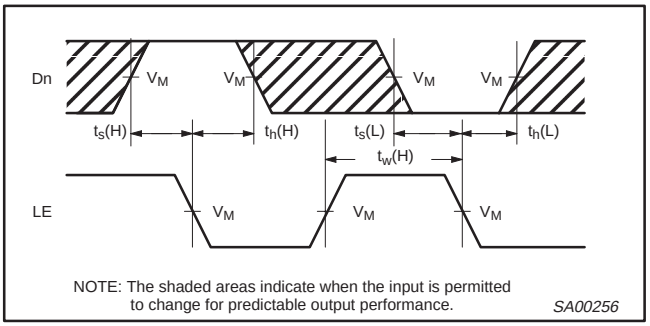
For all waveforms, V_M = 1.5 V.



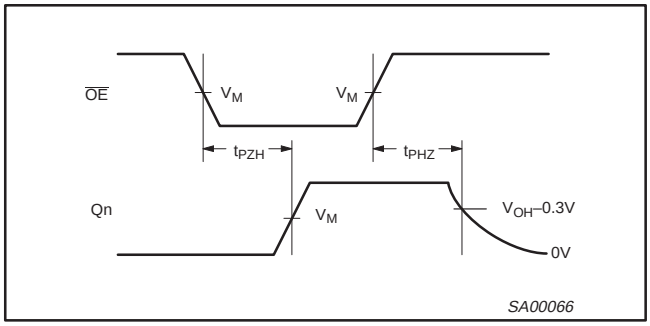
Waveform 1. Propagation Delay, Data to Output, Preset to Output, and Master Reset to Output



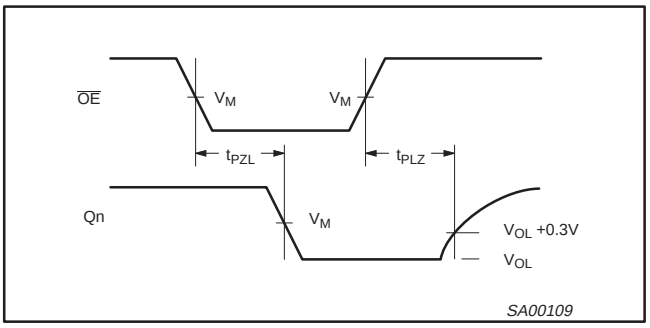
Waveform 2. Propagation Delay, Latch Enable to Output



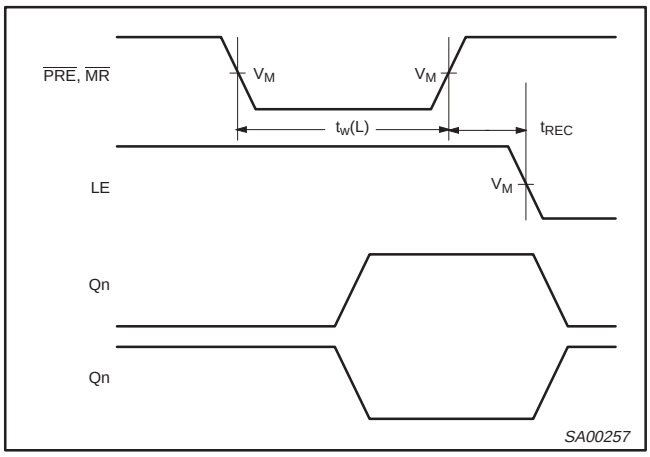
Waveform 3. Data Set-up and Hold Times and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

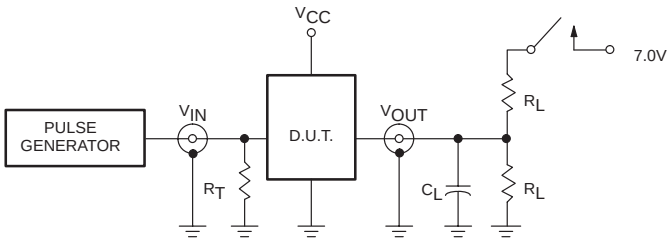


Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

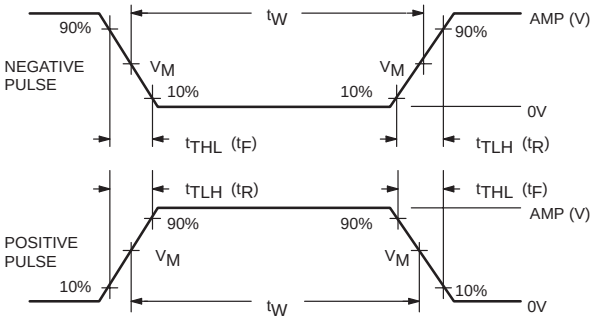


Waveform 6. Master Reset and Preset Pulse Width and Master Reset and Preset to Latch Enable Recovery Time

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

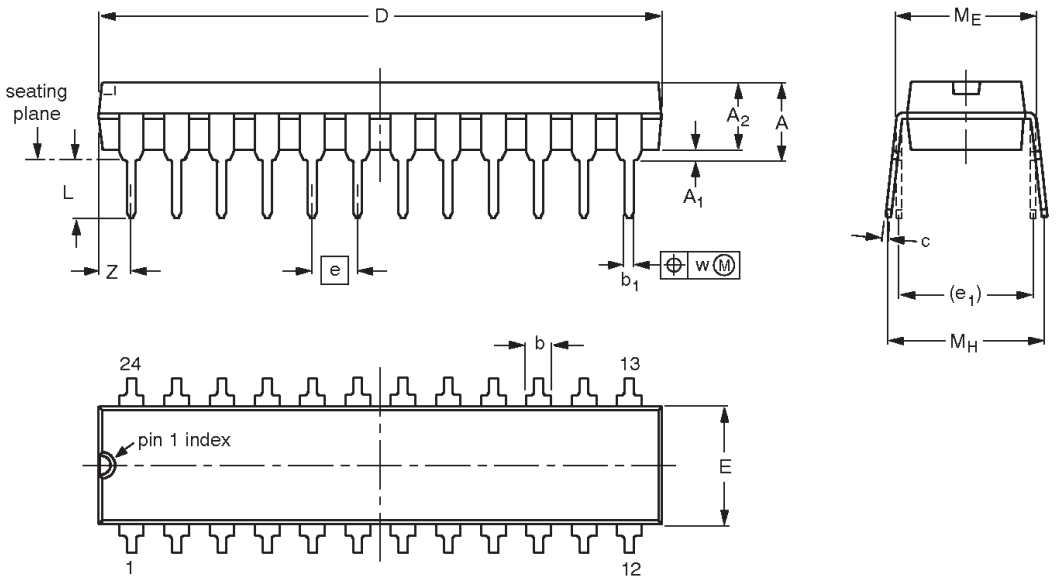
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

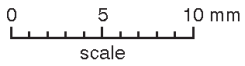
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

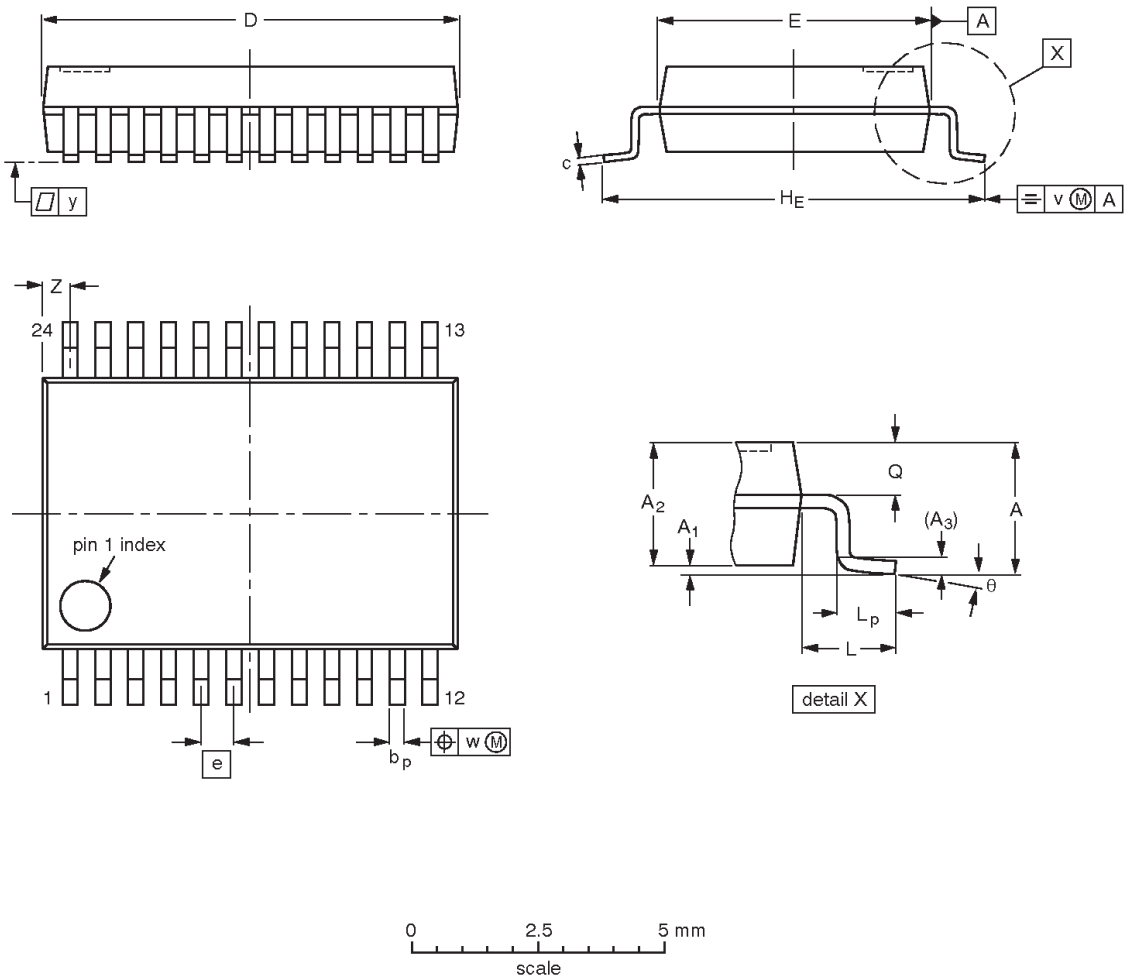
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001				~~99-04-28~~ 99-12-27

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

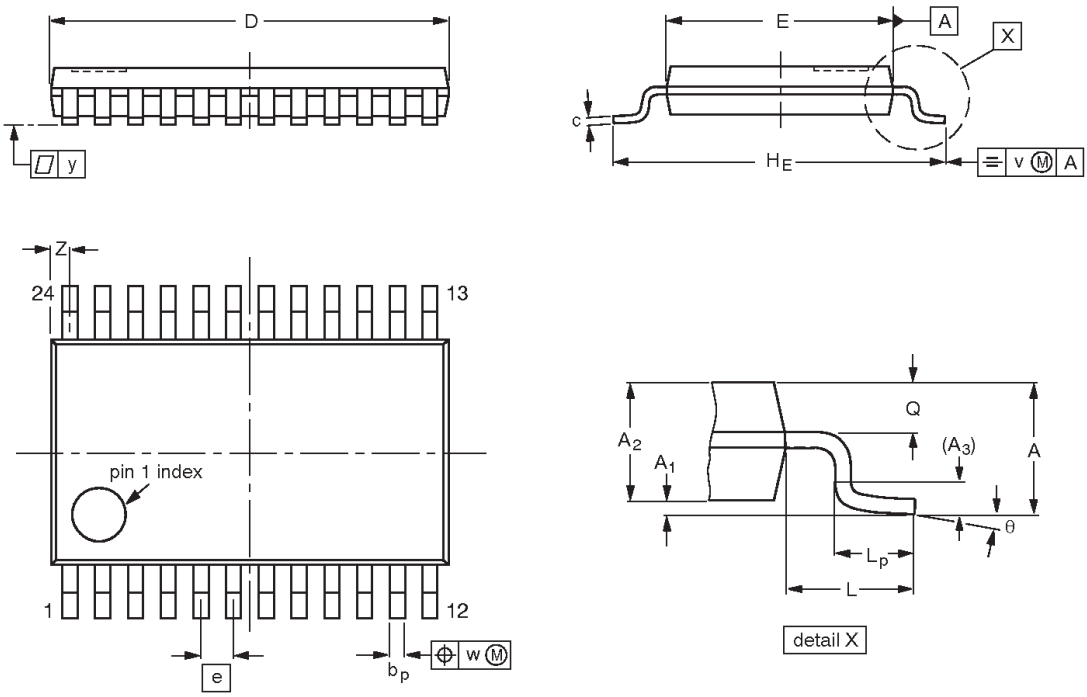
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

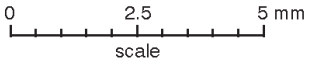
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_2	20021217	**Product data (9397 750 10852); ECN 853-1703 29288 of 12 December 2002. Supersedes data of 06 September 1995.** Modifications: ● Ordering information table: remove “North America” column; remove 74ABT845D package offering.
_1	19950906	**Product specification. ECN 853-1703 15702 of 06 September 1995.**

8-bit bus interface latch with set and reset (3-State)

74ABT845

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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