



3.3V CMOS 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16836

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

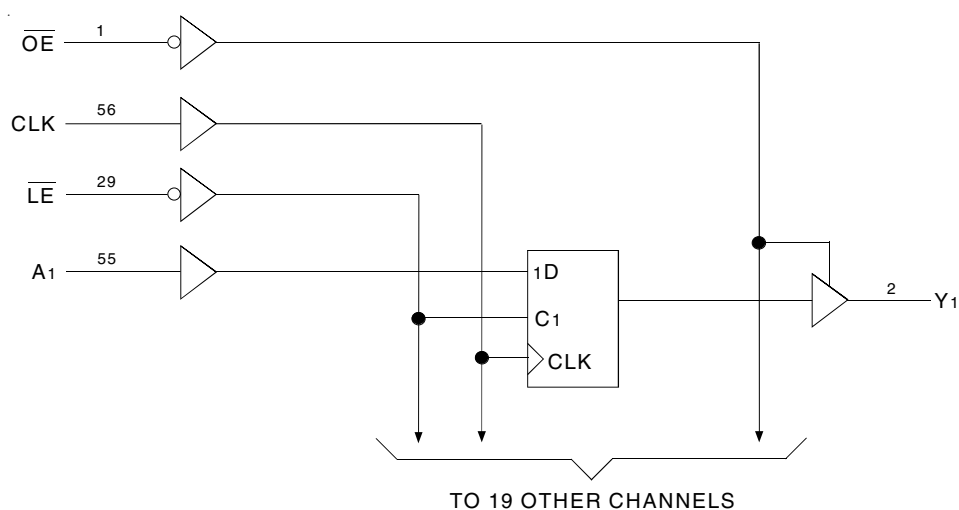
DESCRIPTION:

This 20-bit universal bus driver is built using advanced dual metal CMOS technology. Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low. When $\overline{LE}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

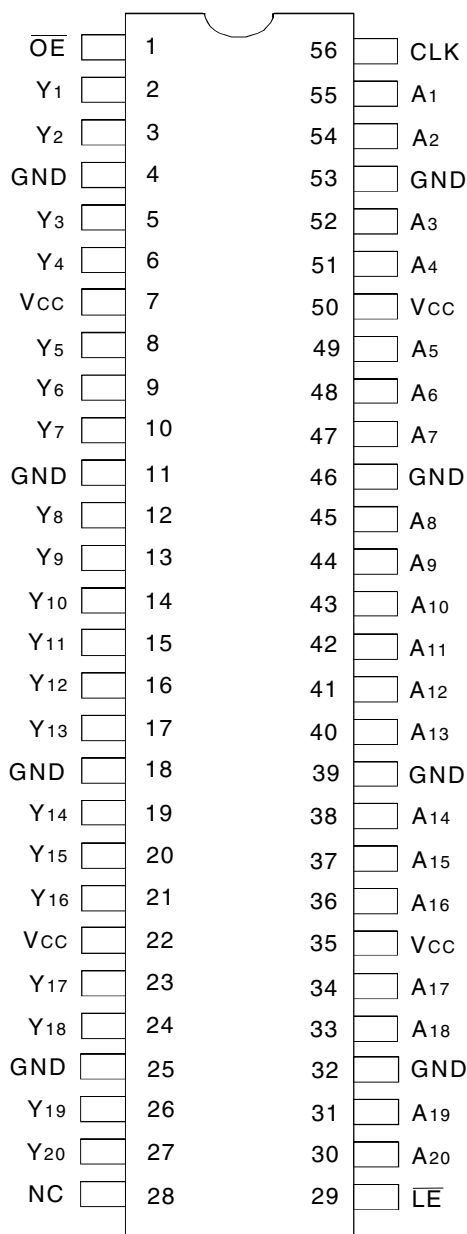
The ALVCH16836 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16836 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high-impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
$\overline{LE}$	Latch Enable (Active LOW)
Ax	Data Inputs ⁽¹⁾
Yx	3-State Outputs
NC	No Internal Connection

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, $V_i < 0$ or $V_i > V_{CC}$	±50	mA
IOK	Continuous Clamp Current, $V_o < 0$	-50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COU	Output Capacitance	VOU = 0V	7	9	pF
COU	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

- As applicable to the device type.

FUNCTION TABLE⁽¹⁾

Inputs				Output
$\overline{OE}$	$\overline{LE}$	CLK	Ax	Yx
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y ⁽²⁾
L	H	L	X	Y ⁽³⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
Z = High-Impedance
- Output level before the indicated steady-state input conditions were established, provided that CLK is HIGH before $\overline{LE}$ goes LOW.
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	μA
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = – 0.1mA	V _{CC} – 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = – 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = – 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V	I _{OH} = – 24mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz			pF
CPD	Power Dissipation Capacitance Outputs disabled				

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	ns
t _{PLH} t _{PHL}	Propagation Delay A _x to Y _x	1	4.2	—	4.2	1	3.6	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{LE}}$ to Y _x	1.3	5	—	4.9	1.3	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to Y _x	1.4	5.5	—	5.2	1.4	4.5	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OE}}$ to Y _x	1.4	5.5	—	5.6	1.1	4.6	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OE}}$ to Y _x	1	4.5	—	4.3	1.3	3.9	ns
t _{SU}	Set-up Time, data before CLK↑	1.4	—	1.7	—	1.5	—	ns
t _{SU}	Set-up Time, data before $\overline{\text{LE}}$ ↑, CLK HIGH	1.2	—	1.6	—	1.3	—	ns
t _{SU}	Set-up Time, data before $\overline{\text{LE}}$ ↑, CLK LOW	1.4	—	1.5	—	1.2	—	ns
t _H	Hold Time, data after CLK↑	0.9	—	0.9	—	0.9	—	ns
t _H	Hold Time, data after $\overline{\text{LE}}$ ↑, CLK HIGH or LOW	1.1	—	1.1	—	1.1	—	ns
t _W	Pulse Duration, $\overline{\text{LE}}$ LOW	3.3	—	3.3	—	3.3	—	ns
t _W	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{SK(O)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

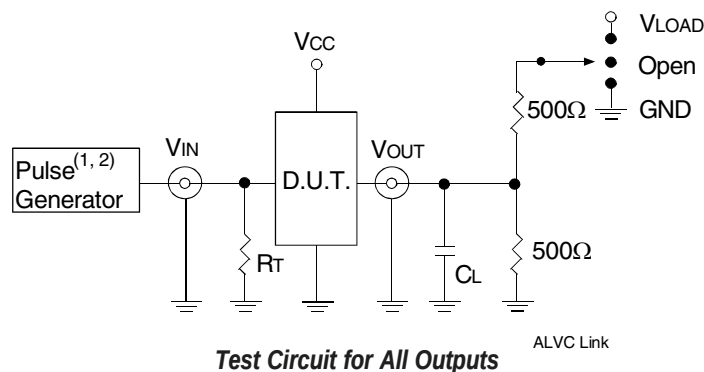
NOTES:

- See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

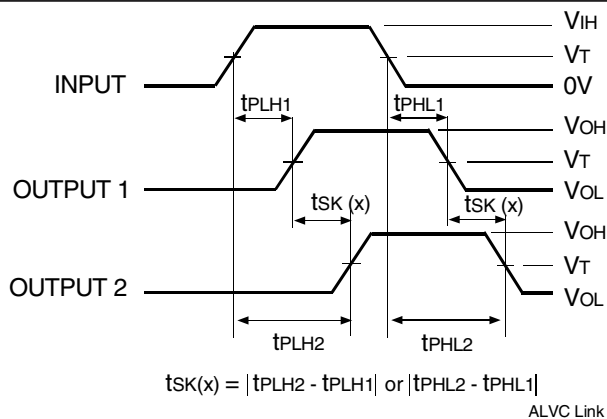
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_f ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_f ≤ 2ns.

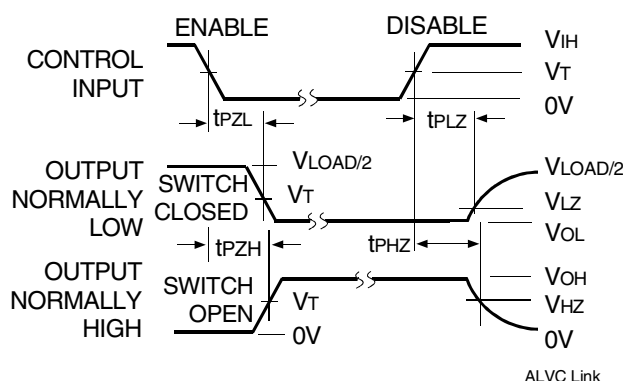
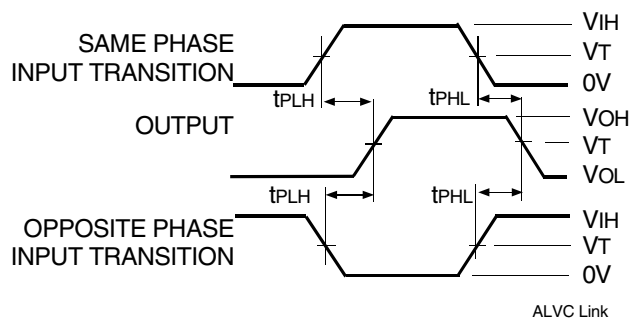
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



NOTES:

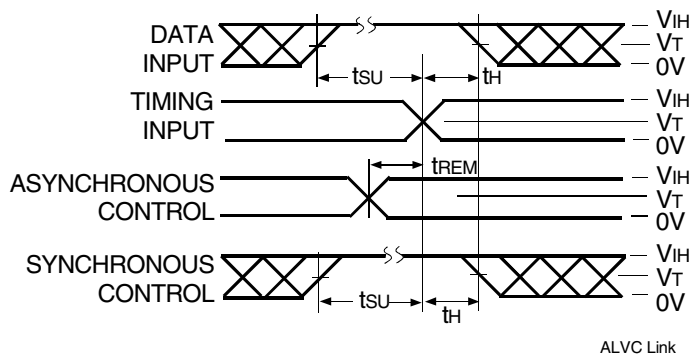
1. For tsK(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsK(b) OUTPUT1 and OUTPUT2 are in the same bank.



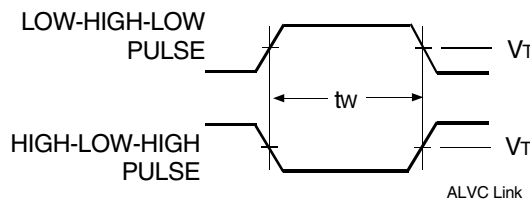
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package
						PA	Thin Shrink Small Outline Package
						PF	Thin Very Small Outline Package
					836		20-Bit Universal Bus Driver with 3-State Outputs
				16			Double-Density with Resistors, $\pm 24\text{mA}$
			H				Bus-Hold
				74			-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459