FAIRCHILD

SEMICONDUCTOR™

74F64
4-2-3-2-Input AND-OR-Invert Gate

General Description

This device contains gates configured to perform a 4-2-3-2 input AND-OR-INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
74F64SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F64SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F64PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
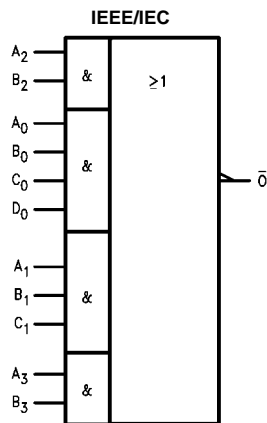
Connection Diagram
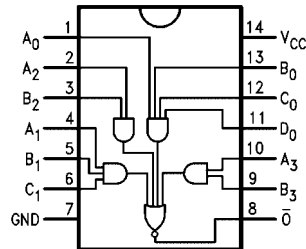
Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_n, B_n, C_n, D_n	Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{O}$	Output	50/33.3	−1 mA/20 mA

74F64

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

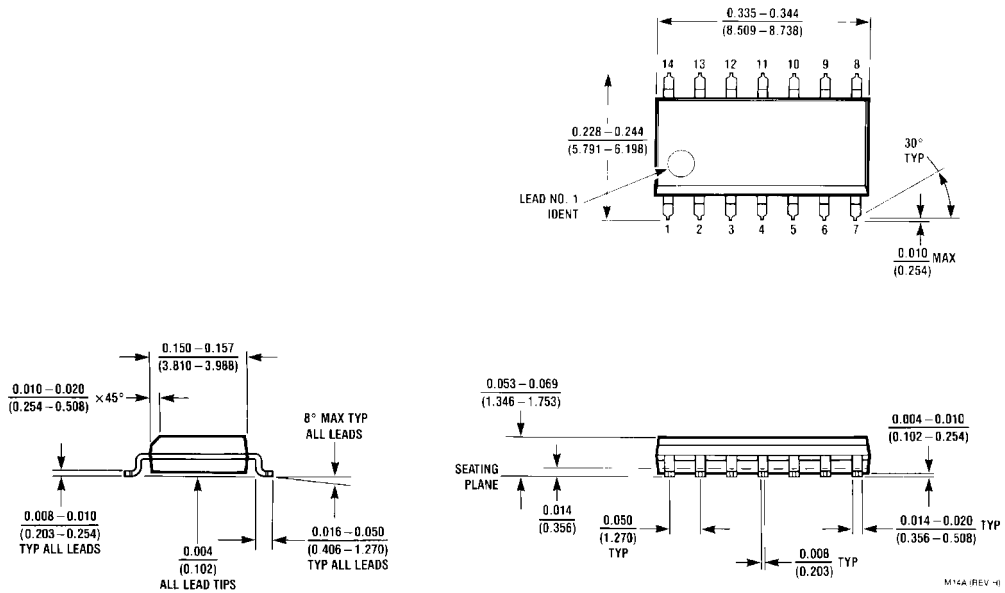**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage		V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage		V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	V	Min	I_{OH} = −1 mA
	Voltage	5% V_{CC}			I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current		µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test		µA	Max	V_{IN} = 7.0V
I_{CEX}	Output High Leakage Current		µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current		µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current		mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current		mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		mA	Max	V_O = LOW

AC Electrical Characteristics

Symbol	Parameter	T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			T_A = 0° to +70°C C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	4.6	6.5	2.5	7.5	ns
t_{PHL}	A_n, B_n, C_n, D_n to $\overline{O}$	1.5	3.2	4.5	1.5	5.5	

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) ×45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1

-A-

1.1 TYP

14   8

7.8

3.9

5.3±0.1

-B-

⌒ | 0.2 | C | B | A
ALL LEAD TIPS

PIN #1 IDENT.

1   7

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   6   7

1.27 TYP   0.6 TYP

ALL LEAD TIPS

2.1 MAX.

⌒ | 0.1 | C

-C-

1.8±0.1

0.15±0.05

1.27 TYP

0.35-0.51

⊕ | 0.12 Ⓜ | C | A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A
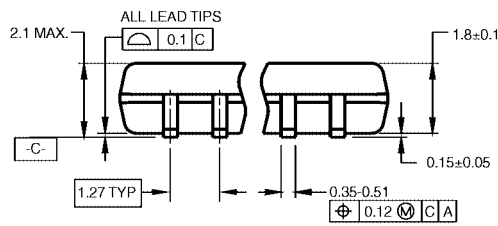
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1
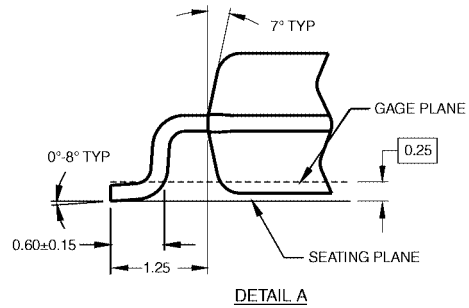
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com