GTLP/TTL 1:2/1:6 CLOCK DRIVER

IDT74GTLP816
PRELIMINARY

FEATURES:

- **Interface between GTLP and TTL logic levels**
- **GTLP to TTL 1:6 fanout**
- **TTL to GTLP 1:2 fanout**
- **Edge Rate Control Circuit reduces output noise on GTLP port**
- **V_{REF} pin provides reference voltage for receiver threshold**
- **CMOS technology for low power dissipation**
- **Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage, and temperature**
- **5V tolerant inputs and outputs on TTL ports**
- **TTL-compatible Driver and Control inputs**
- **High Output source/sink ±24mA on TTL ports**
- **High Output sink +34mA on GTLP ports**
- **Open drain on GTLP to support wired-or connection**
- **Available in TSSOP package**

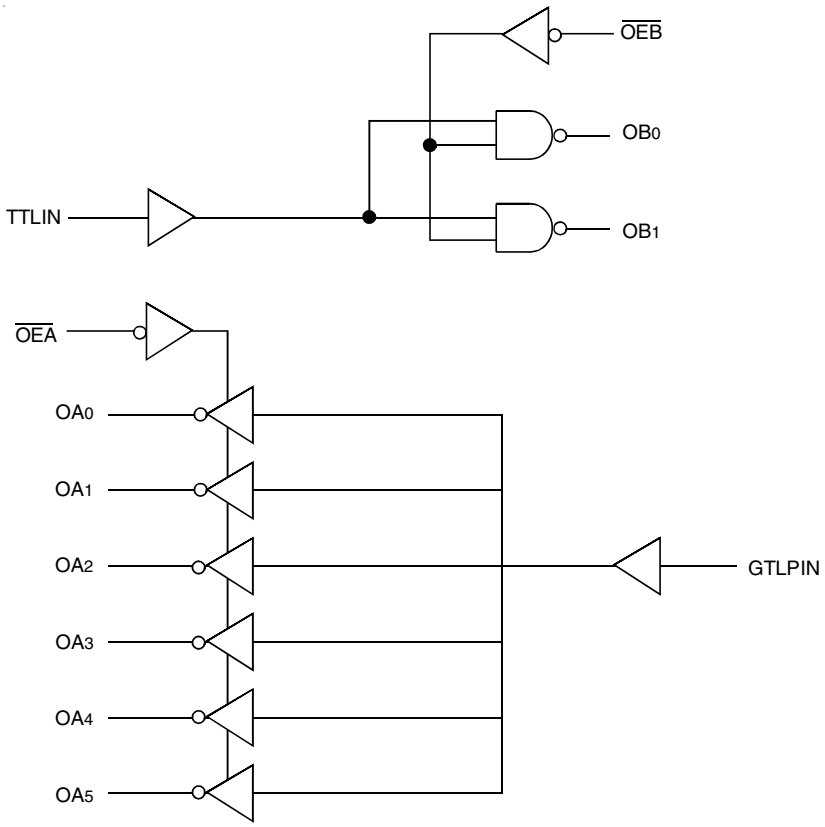
DESCRIPTION:

The GTLP816 is a GTLP to TTL (1:6) and TTL to GTLP (1:2) clock driver with inverting outputs. The clock driver provides a high-speed interface between cards operating at TTL logic levels and back-planes operating at GTLP logic levels. GTLP provides reduced output swing (<1V), reduced input threshold levels, and output edge-rate control to minimize signal setting times. The GTLP816 is a derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD8-3 and incorporates internal edge-rate control, which is process, voltage, and temperature (PVT) compensated.

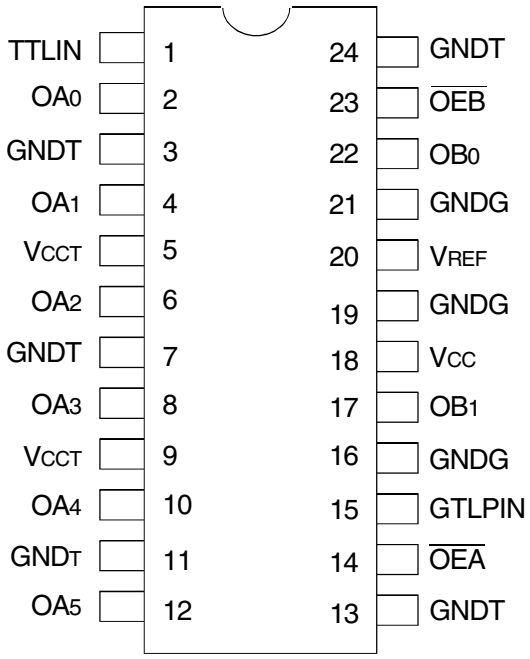
GTLP output low voltage is typically less than 0.5V. The output high is 1.5V, and the receiver threshold is 1V.

The GTLP816 is available in Industrial Temperature Range (-40°C to +85°C). See Ordering Information for details.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1,2)

Symbol	Rating		Max.	Unit
V_{CC}	Supply Voltage		–0.5 to +7	V
V_{CCT}				
V_I	DC Input Voltage		–0.5 to +7	V
V_O	DC Output Voltage	3-State	–0.5 to +7	V
		Active	–0.5 to V_{CC} + 0.5	
I_{OL}	DC Output Sink Current into OA		64	mA
I_{OH}	DC Output Source Current from OA		–64	mA
I_{OL}	DC Output Sink Current into OB (in the LOW state)		80	mA
I_{IK}	DC Input Diode Current	V_I < 0V	–50	mA
I_{OK}	DC Output Diode Current	V_O < 0V	–50	mA
		V_O > V_{CC}	+50	
T_{STG}	Storage Temperature		–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Unused inputs must be held HIGH or LOW.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.(2)	Max.	Unit
C_{IN}	Control Pins/GTLPIN/TTLIN	V_I = V_{CC} or 0	3.7	—	pF
C_{OUT}	OAx	V_I = V_{CC} or 0	7	—	pF
	OBx	V_I = V_{CC} or 0	7	—	pF

NOTES:
1. As applicable to the device type.
2. All typical values are at V_{CC}, V_{CCT} = 5V, T_A = 25°C

FUNCTION TABLE(1)

Inputs				Outputs(2)	
$\overline{OEB}$	$\overline{OEA}$	GTLPIN	TTLIN	OAx	OBx
L	L	H	H	L	L
L	L	L	L	H	H
H	H	X	X	Z	Z

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output polarity is inverting.

PIN DESCRIPTION

Pin Names	Description
TTLIN, GTLPIN	Clock Inputs (TTL and GTLP)
$\overline{OEB}$	Clock Enable for GTLP Outputs. Set LOW for normal operation.
$\overline{OEA}$	Clock Enable for TTL Outputs. Set LOW for normal operation.
V_{CCT}	Power Supply for TTL Clock Outputs
GNDT	Ground for TTL Clock Outputs
V_{CC}	Power Supply for Internal Circuitry
GNDG	Ground for GTLP Clock Outputs
V_{REF}	Voltage Reference Input
OA[5:0]	TTL Clock Outputs (Inverted)
OB[1:0]	GTLP Clock Outputs (Inverted)

RECOMMENDED OPERATING CONDITIONS(1)

Symbol	Rating		Min.	Typ.	Max.	Unit
V_{CC}, V_{CCT}	Supply Voltage		4.75	5	5.25	V
V_{TT}	Bus Termination Voltage	GTLP	1.47		1.53	V
		V_{REF}	0.98		1.02	
V_I	Input Voltage on TTLIN and Control Pins		0	—	5.5	V
I_{OH}	HIGH Level Output Current (OAx)		—	—	-24	mA
I_{OL}	LOW Level Output Current (OAx)		—	—	+24	mA
I_{OL}	LOW Level Output Current (OBx)		—	—	+34	mA
T_A	Operating Temperature		–40	+25	+85	°C

NOTE:

1. Unused inputs must be held HIGH or LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C; V_{REF} = 1V; V_{CC}, V_{CCT} = 5V ± 5%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	GTLPIN			V_{REF}+ 0.05	—	V_{TT}	V
	All Others			2	—	—	
V_{IL}	GTLPIN			0	—	V_{REF}– 0.05	V
	All Others			—	—	0.8	
V_{REF}	GTLP			—	1	—	V
	GTL			—	0.8	—	
V_{TT}	GTLP			—	1.5	—	V
	GTL			—	1.2	—	
V_{IK}		V_{CC} = Min, I_I = –18mA		—	—	–1.2	V
V_{OH}	OAx	V_{CC} = Min	I_{OH} = –100µA	V_{CC}–0.2	—	—	V
			I_{OH} = –18mA	2.4	—	—	
			I_{OH} = –24mA	2.2	—	—	
V_{OL}	OAx	V_{CC} = Min	I_{OL} = 100µA	—	—	0.2	V
			I_{OL} = 18mA	—	—	0.4	
			I_{OL} = 24mA	—	—	0.5	
V_{OL}	OBx	V_{CC} = Min	I_{OL} = 100µA	—	—	0.2	V
			I_{OL} = 34mA	—	—	0.65	
I_I	TTLIN/Control Pins	V_{CC} = Max	V_I = 5.25V or 0V	—	—	±5	µA
	GTLPIN		V_I = V_{TT} or 0V	—	—	±5	
I_{OFF}	TTLIN	V_{CC} = 0	V_I or V_O = 0 to 5.25V	—	—	100	µA
I_{OZH}	OAx	V_{CC} = Max	V_O = 5.25 V	—	—	5	µA
	OBx		V_O = 1.5V	—	—	5	
I_{OZL}	OAx	V_{CC} = Max	V_O = 0	—	—	–5	µA
I_{CC}	OAx or OBx	V_{CC} = Max	Outputs HIGH	—	7	18	mA
			Outputs LOW	—	7	20	
		V_I = V_{CC} or GND	Outputs Disabled	—	7	20	
ΔI_{CC}(2)	TTLIN	V_{CC} = Max	V_I = V_{CC} - 2.1	—	—	6	mA

NOTES:

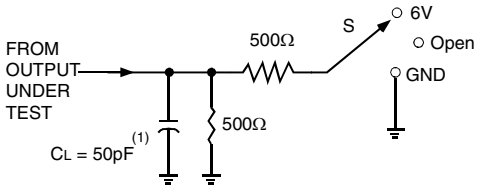
1. All typical values are at V_{CC}, V_{CCT} = 5V, and T_A = 25°C.
2. ΔI_{CC} is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC ELECTRICAL CHARACTERISTICS(1,2)

Symbol	Parameter	Min.	Typ.(3)	Max.	Unit
t_{PLH}	TTLIN to OBx	1.5	3.8	6	ns
t_{PHL}		1.5	2.8	5	
t_{PLH}	$\overline{OEB}$ to OBx	1.5	6.4	10.5	ns
t_{PHL}		1.5	3.2	6	
t_{PLH}	GTLPIN to OAx	1.5	4.4	6.5	ns
t_{PHL}		1.5	4	6	
t_R	OBx Output Rise Time (20% to 80%)	—	2.3	—	ns
t_F	OBx Output Fall Time (20% to 80%)	—	2.3	—	
t_R	OAx Output Rise Time (10% to 90%)	—	2	—	ns
t_F	OAx Output Fall Time (10% to 90%)	—	2	—	
$t_{SK(o)}$	Output Skew(4)	—	0.2	1	ns
t_{PZH}	$\overline{OEA}$ to OAx	0.5	3.6	6.5	ns
t_{PZL}					
t_{PHZ}		0.5	3.8	6.5	ns
t_{PLZ}					

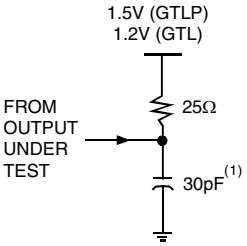
NOTES:
1. See Test Circuits and Waveforms.
2. Unless otherwise noted, V_{REF} = 1V, C_L = 30pF for OBx, and C_L = 50pF for OAx.
3. Typical values are at V_{CC}, V_{CCT} = 5V, and T_A = 25°C.
4. Skew specs are given for specific, worst case V_{CC} temp. Skew values between the OBx outputs could vary on the backplane due to loading and impedance seen by the device.

TEST CIRCUITS AND WAVEFORMS



NOTE:
1. CL includes probes and jig capacitance.

Test Circuit for OA Outputs

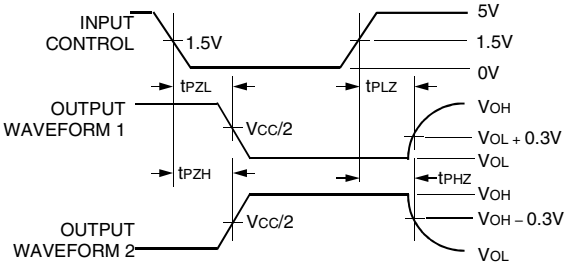


NOTE:
1. CL includes probes and jig capacitance. CL = 30pF is used for worst case.

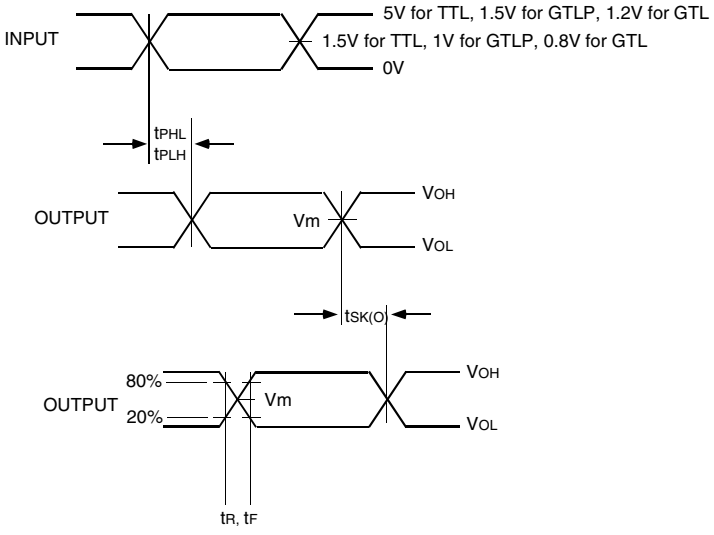
Test Circuit for OB Outputs

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open



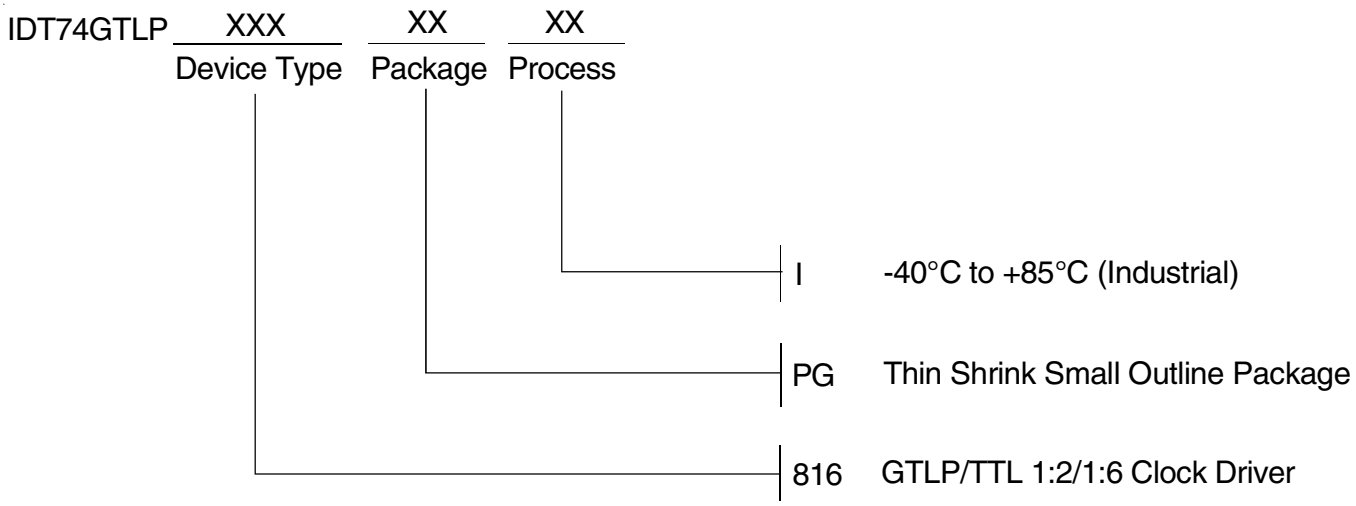
Voltage Waveforms Enable and Disable Times (OAx)



Voltage Waveforms Pulse Duration
(Vm = Vcc/2 for OAx and 1V for OBx)

NOTES:
Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
All input pulses have the following characteristics: frequency = 10 MHz, tR = tF = 2 ns, ZO = 50Ω. The outputs are measured one at a time with one transition per measurement.

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459