

# DATA SHEET

**74HC3G07; 74HCT3G07**  
**Buffers with open-drain outputs**

Product specification  
File under Integrated Circuits, IC06

2003 Aug 21

**Buffers with open-drain outputs****74HC3G07; 74HCT3G07****FEATURES**

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- ESD protection:  
2000 V Human Body Model (A 114-A)  
200 V Machine Model (A 115-A).
- Balanced propagation delays
- Very small 8 pins package.

**DESCRIPTION**

The 74HC3G/HCT3G07 is a high-speed Si-gate CMOS device. Specified in compliance with JEDEC standard no. 7A.

The 74HC3G/HCT3G07 provides three non-inverting buffers.

The outputs of the 74HC3G/HCT3G07 devices are open drains and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

**QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 6.0 \text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC3G	HCT3G	
$t_{PZL}$	propagation delay nA to nY	$C_L = 50 \text{ pF}$ ; $V_{CC} = 4.5 \text{ V}$	9	11	ns
$t_{PLZ}$	propagation delay nA to nY	$C_L = 50 \text{ pF}$ ; $V_{CC} = 4.5 \text{ V}$	11	10	ns
$C_I$	input capacitance		1.5	1.5	pF
$C_{PD}$	power dissipation capacitance	notes 1 and 2	4	4	pF

**Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;  $V_{CC}$  = supply voltage in Volts;

$N$  = total switching outputs;  $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. For HC3G the condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

For HCT3G the condition is  $V_I = \text{GND}$  to  $V_{CC} - 1.5 \text{ V}$ .

**FUNCTION TABLE**

See note 1.

INPUTS	OUTPUTS
nA	nY
L	L
H	Z

**Note**

1. H = HIGH voltage level;  
L = LOW voltage level;  
Z = high-impedance OFF-state.

## Buffers with open-drain outputs

## 74HC3G07; 74HCT3G07

## ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC3G07DP	-40 to +125 °C	8	TSSOP-8	plastic	SOT505-2	H07
74HCT3G07DP	-40 to +125 °C	8	TSSOP-8	plastic	SOT505-2	T07

## PINNING

PIN	SYMBOL	DESCRIPTION
1, 3, 6	1A, 2A, 3A	data inputs
2, 5, 7	3Y, 2Y, 1Y	data outputs
4	GND	ground (0 V)
8	V <sub>CC</sub>	DC supply voltage

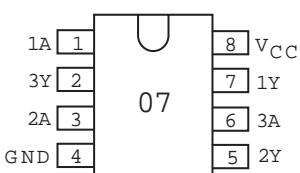


Fig.1 Pin configuration.

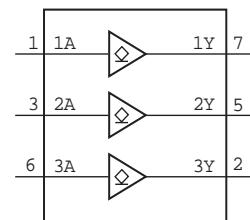


Fig.2 Logic symbol.

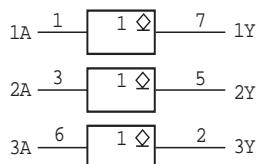


Fig.3 IEC logic symbol.

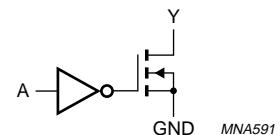


Fig.4 Logic diagram (one driver).

## Buffers with open-drain outputs

## 74HC3G07; 74HCT3G07

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC3G07			74HCT3G07			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	–	6.0	0	–	5.5	V
V <sub>O</sub>	output voltage		0	–	V <sub>CC</sub>	0	–	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t <sub>r,t<sub>f</sub></sub>	input rise and fall times	V <sub>CC</sub> = 2.0 V	–	–	1000	–	–	–	ns
		V <sub>CC</sub> = 4.5 V	–	6.0	500	–	6.0	500	ns
		V <sub>CC</sub> = 6.0 V	–	–	400	–	–	–	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		–0.5	+7.0	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < –0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V; note 1	–	±20	mA
I <sub>OK</sub>	output diode current	V <sub>O</sub> < –0.5 V; note 1	–	–20	mA
V <sub>O</sub>	output voltage	active mode; note 1	–0.5	V <sub>CC</sub> + 0.5	V
		high-impedance mode; note 1	–0.5	7.0	V
I <sub>O</sub>	output sink current	–0.5 V < V <sub>O</sub> < 7.0 V; note 1	–	–25	mA
I <sub>CC</sub>	V <sub>CC</sub> or GND current	note 1	–	50	mA
T <sub>stg</sub>	storage temperature		–65	+150	°C
P <sub>D</sub>	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	300	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P<sub>D</sub> derates linearly with 8 mW/K.

## Buffers with open-drain outputs

## 74HC3G07; 74HCT3G07

## DC CHARACTERISTICS

## Type 74HC3G07

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	2.0	–	0	0.1	V
			4.5	–	0	0.1	V
			6.0	–	0	0.1	V
			4.5	–	0.15	0.33	V
			6.0	–	0.16	0.33	V
			6.0	–	–	–	–
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	6.0	–	–	±5.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	10	µA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	2.0	–	–	0.1	V
			4.5	–	–	0.1	V
			6.0	–	–	0.1	V
			4.5	–	–	0.4	V
			6.0	–	–	0.4	V
			6.0	–	–	–	–
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	6.0	–	–	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	20	µA

## Note

- All typical values are measured at T<sub>amb</sub> = 25 °C.

## Buffers with open-drain outputs

## 74HC3G07; 74HCT3G07

**Type 74HCT3G07**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>cc</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	—	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	—	1.2	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA I <sub>O</sub> = 4.0 mA	4.5 4.5	— —	0 0.15	0.1 0.33	V V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	—	—	±1.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	—	±5.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	—	—	10	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	—	—	375	µA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	—	—	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	—	—	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA I <sub>O</sub> = 4.0 mA	4.5 4.5	— —	— —	0.1 0.4	V V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	—	—	±1.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	—	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	—	—	20	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	—	—	410	µA

**Note**

- All typical values are measured at T<sub>amb</sub> = 25 °C.

## Buffers with open-drain outputs

## 74HC3G07; 74HCT3G07

## AC CHARACTERISTICS

## Type 74HC3G07

GND = 0 V;  $t_r = t_f \leq 6.0$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)				UNIT	
		WAVEFORMS	$V_{cc}$ (V)	-40 to +85		-40 to +125			
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.		
$t_{PZL}$	propagation delay nA to nY	see Figs 5 and 6	2.0	—	25	95	—	125 ns	
			4.5	—	9	19	—	25 ns	
			6.0	—	7	16	—	20 ns	
$t_{PLZ}$	propagation delay nA to nY	see Figs 5 and 6	2.0	—	25	95	—	125 ns	
			4.5	—	11	23	—	30 ns	
			6.0	—	10	23	—	26 ns	
$t_{THL}$	output transition time	see Figs 5 and 6	2.0	—	18	95	—	125 ns	
			4.5	—	6	19	—	25 ns	
			6.0	—	5	16	—	20 ns	

## Note

- All typical values are measured at  $T_{amb} = 25$  °C.

## Type 74HCT3G07

GND = 0 V;  $t_r = t_f \leq 6.0$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)				UNIT	
		WAVEFORMS	$V_{cc}$ (V)	-40 to +85		-40 to +125			
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.		
$t_{PZL}$	propagation delay nA to nY	see Figs 5 and 6	4.5	—	11	27	—	32 ns	
$t_{PLZ}$	propagation delay nA to nY	see Figs 5 and 6	4.5	—	10	26	—	31 ns	
$t_{THL}$	output transition time	see Figs 5 and 6	4.5	—	6	19	—	22 ns	

## Note

- All typical values are measured at  $T_{amb} = 25$  °C.

## Buffers with open-drain outputs

74HC3G07; 74HCT3G07

## AC WAVEFORMS

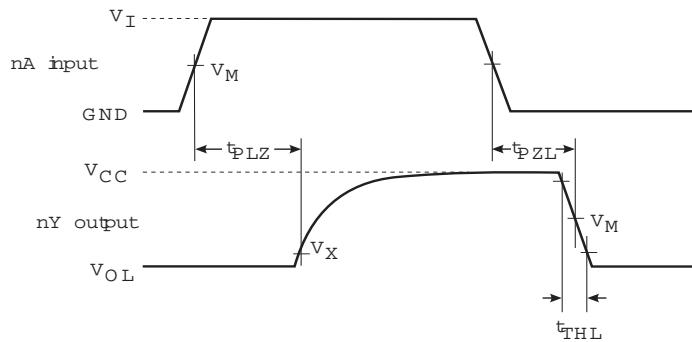
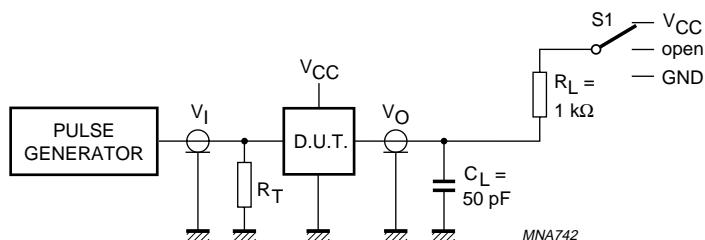
For HC3G:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .For HCT3G:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3.0 \text{ V}$ .For HC3G and HCT3G:  $V_X = 0.1 \times V_{CC}$ .

Fig.5 The input (nA) to output (nY) propagation delays and transition times.



TEST	S <sub>1</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	open
t <sub>PZL</sub> /t <sub>PZL</sub>	V <sub>CC</sub>
t <sub>PZH</sub> /t <sub>PZH</sub>	GND

Definitions for test circuit:

 $C_L$  = load capacitance including jig and probe capacitance (see "AC characteristics"). $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

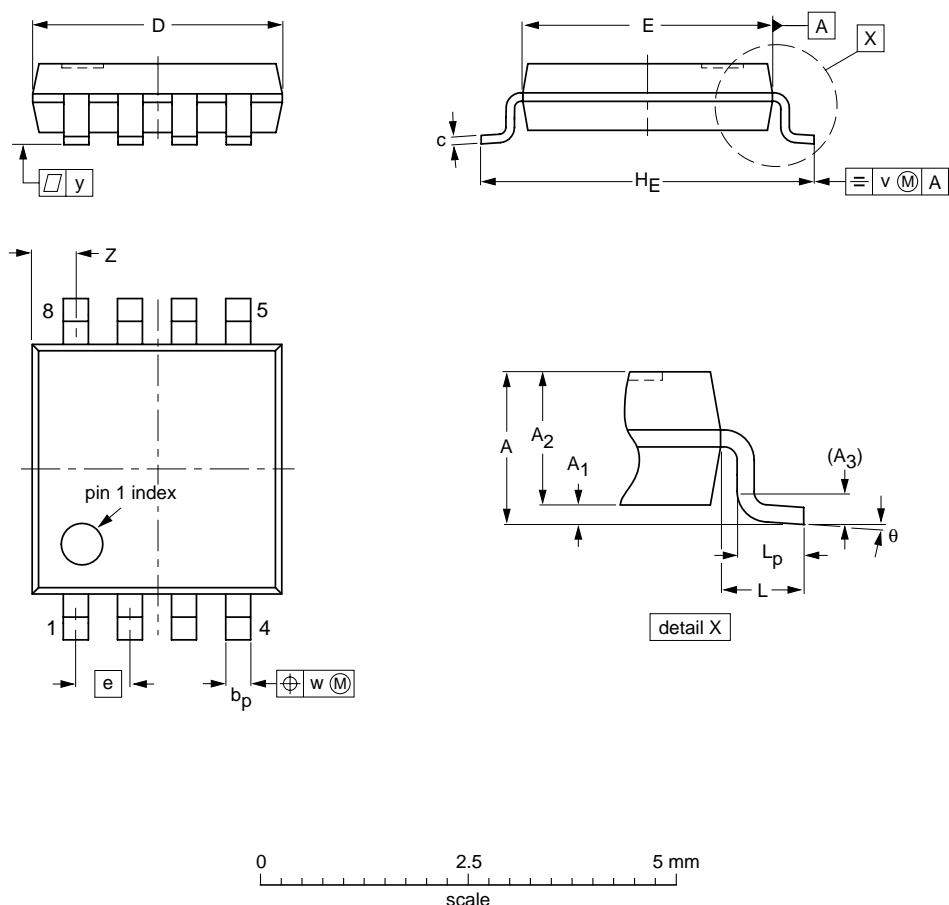
Fig.6 Load circuitry for switching times.

## Buffers with open-drain outputs

74HC3G07; 74HCT3G07

## PACKAGE OUTLINE

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



## DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

## Note

- Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

## Buffers with open-drain outputs

74HC3G07; 74HCT3G07

**DATA SHEET STATUS**

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS <sup>(1)</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

**Note**

1. Please consult the most recently issued data sheet before initiating or completing a design.

**DEFINITIONS**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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