

74VCX38

Low Voltage Quad 2-Input NAND Gate with Open Drain Outputs and 3.6V Tolerant Inputs and Outputs

General Description

The VCX38 contains four 2-input NAND gates with open drain outputs. This product is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The VCX38 is fabricated with advanced CMOS technology to achieve high-speed operation while maintaining CMOS low power dissipation.

Features

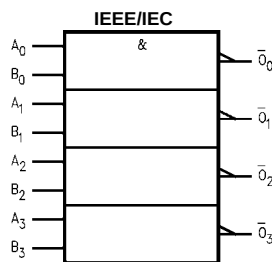
- 1.4V-3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
2.8 ns max for 3.0V to 3.6V V_{CC}
- Power-Off high impedance inputs and outputs
- Static Drive (I_{OL})
+24 mA @ 3.0V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 250V

Ordering Code:

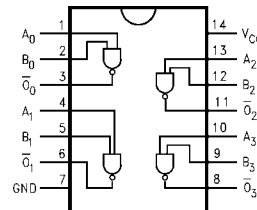
Order Number	Package Number	Package Description
74VCX38M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VCX38MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\bar{O}_n$	Outputs

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O) (Note 2)	−0.5V to +4.6V
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
DC Output Source/Sink Current (I_{OL})	+50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{stg})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	0V to 3.6V
Output Current in I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	+24 mA
$V_{CC} = 2.3V$ to 2.7V	+18 mA
$V_{CC} = 1.65V$ to 2.3V	+6 mA
$V_{CC} = 1.4V$ to 1.6V	+2 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{in} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Floating or unused inputs must be held HIGH or LOW

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6	2.0 1.6 $0.65 \times V_{CC}$ $0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6		0.8 0.7 $0.35 \times V_{CC}$ $0.35 \times V_{CC}$	V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 18 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	2.7 - 3.6 2.7 3.0 3.0		0.2 0.4 0.4 0.55	V
		$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 18 \text{ mA}$	2.3 - 2.7 2.3 2.3		0.2 0.4 0.6	
		$I_{OL} = 100 \mu A$ $I_{OL} = 6 \text{ mA}$	1.65 - 2.3 1.65		0.2 0.3	
		$I_{OL} = 100 \mu A$ $I_{OL} = 2 \text{ mA}$	1.4 - 1.6 1.4		0.2 0.35	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.4 - 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \leq (V_I) \leq 3.6V$	1.4 - 3.6 1.4 - 3.6		20 ±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	μA
I_{OHZ}	Off State Current	$V_O = 3.6$	1.4 - 3.6		10	μA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PZL} , t _{PLZ}	Propagation Delay	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	2.8	ns	Figures 1, 2
			2.5 ± 0.2	0.8	3.7		
			1.8 ± 0.15	1.0	6.7		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	13.4		Figures 3, 4
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 5)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1		1.5		

Note 4: For C_L = 50pF, add approximately 300 ps to the 30 pF AC maximum specification.

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _I = 0V OR V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	6	pF
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} $3.3V \pm 0.3V$ to $1.8V \pm 0.15V$)

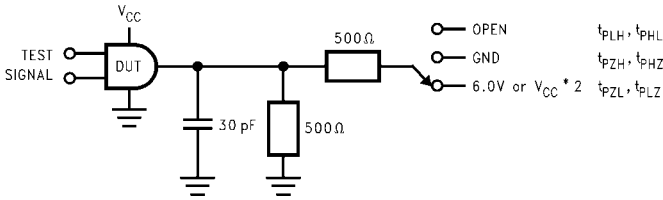


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V$; 1.8V

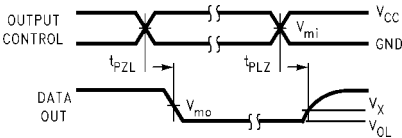


FIGURE 2. Waveform for Open Drain, Inverting and Non-inverting Functions

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5 \pm 0.1V$)

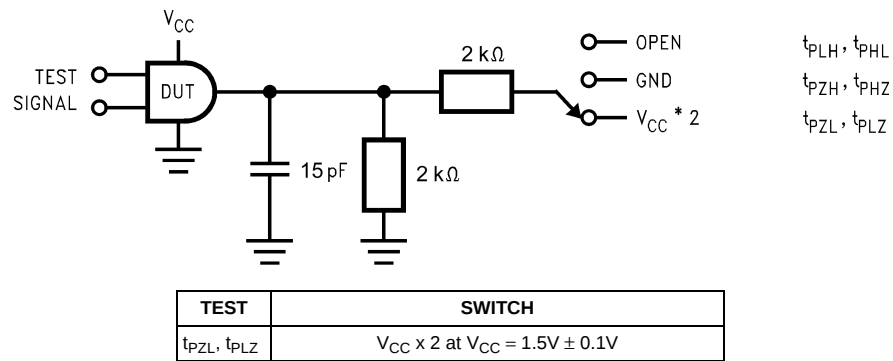


FIGURE 3. AC Test Circuit

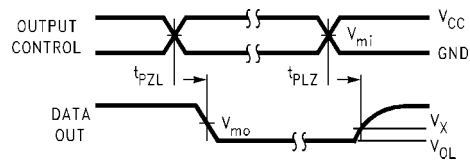
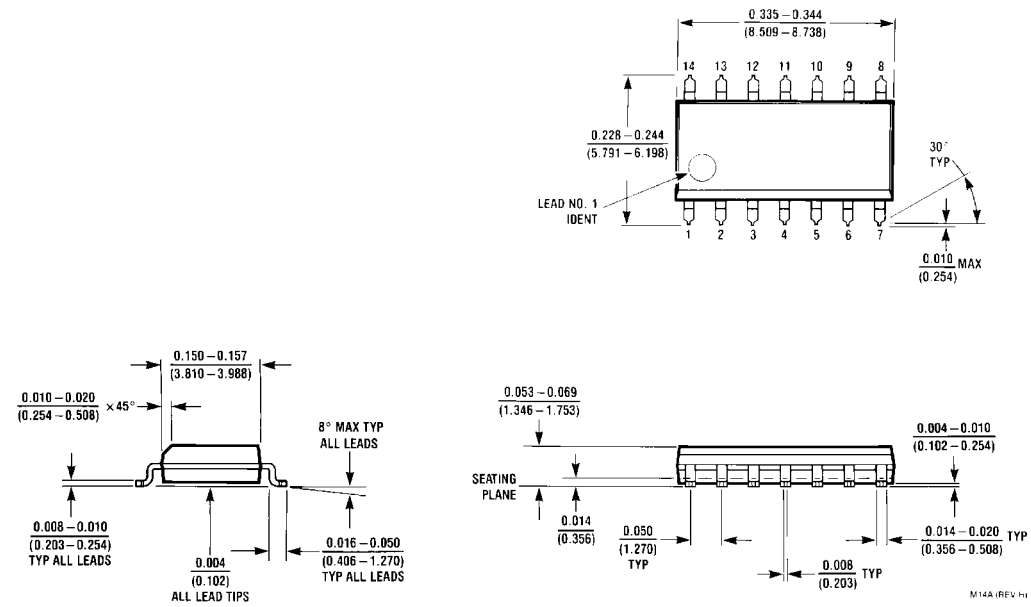


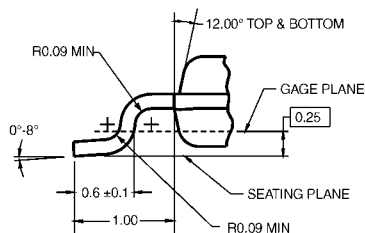
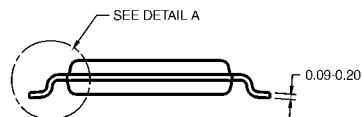
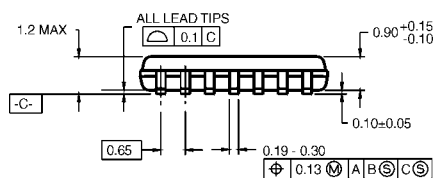
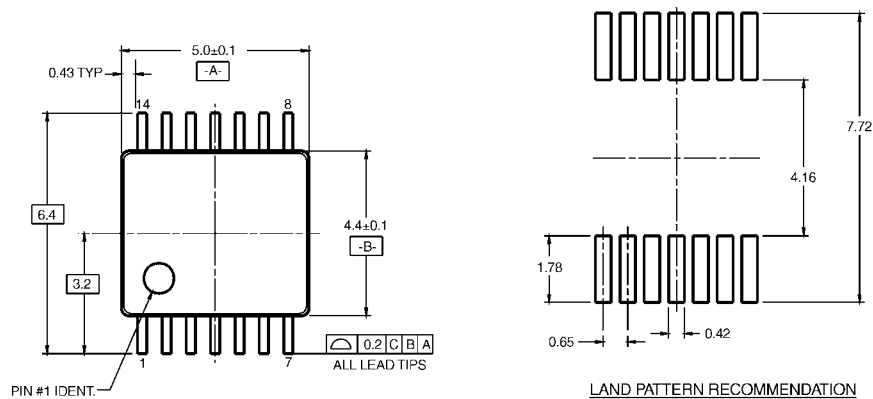
FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_x	$V_{OL} + 0.1V$
V_y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

DETAIL A

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

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