



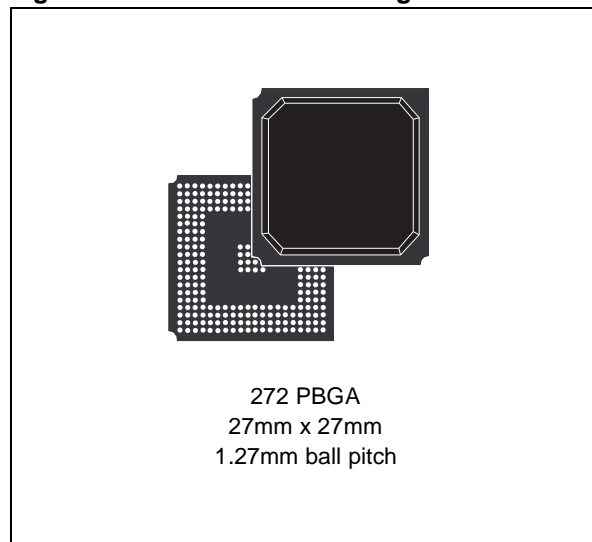
16K x 68-bit Entry NETWORK SEARCH ENGINE

DATA BRIEFING

FEATURES SUMMARY

- 16K ENTRIES IN 68-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO FOUR (4) QUADRANTS
(Data entry width in each quadrant is configurable as 34, 68, 136, or 272 bits.)
- UP TO 83 MILLION SUSTAINED SEARCHES PER SECOND IN 68-BIT and 136-BIT CONFIGURATIONS
- UP TO 41.5 MILLION SEARCHES PER SECOND IN 34-BIT and 272-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 124K to 992K DEPENDING ON THE SIZE OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE:
 V_{DD} (Operating Supply Voltage) = 1.8V
 V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 272 BALL, 27mm x 27mm, CAVITY-UP BGA

Figure 1. 272-ball PBGA Package



DESCRIPTION

Overview

The M7010 is a feature-rich hardware search engine optimized for networking and communications applications. It incorporates leading-edge Associative Processing Technology (APT, trademark of Cypress Semiconductor, Inc.) and Advanced Power Management. The data table may be partitioned into up to four (4) quadrants, allowing the user to configure each quadrant with different table entry widths (x34, x68, x136, or x272-bit). It is also programmable to accelerate performance.

Performance

The M7010 outperforms competitive solutions using software sequential search algorithms in conjunction with SRAMs or ASICs, or hardware implementation with ASICs and CAMs. The latter solution, while faster than a software-based solution, still suffers from performance degradation

when depth-cascaded and is unable to scale to next-generation requirements. The M7010-based solutions overcome all of these drawbacks.

Applications

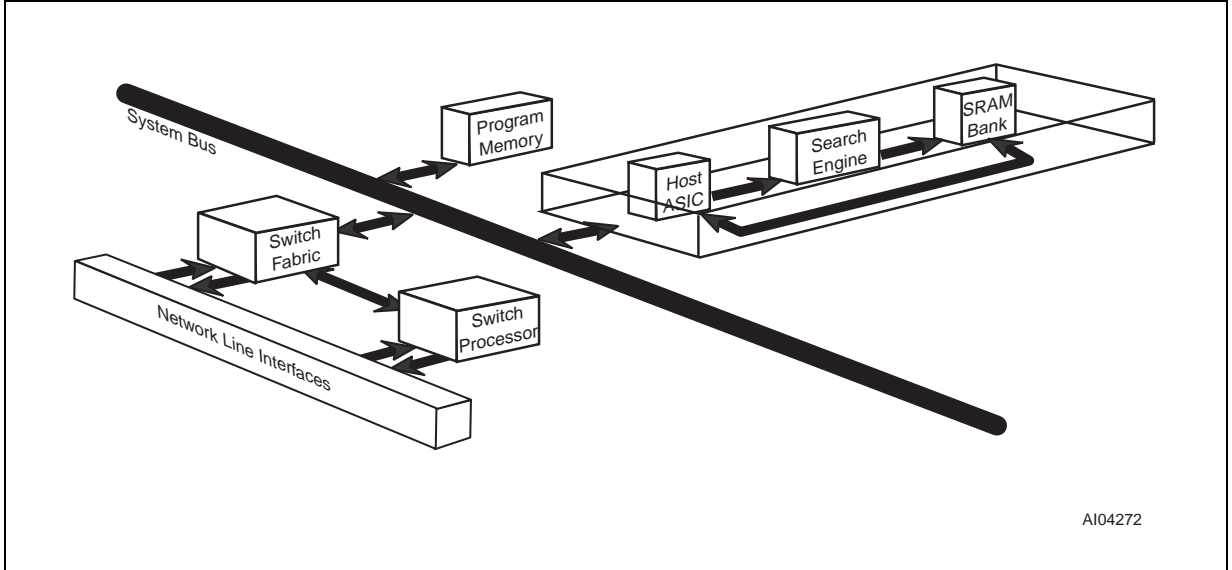
The performance and features of the M7010 makes it ideal in applications such as enterprise LAN switches, broadband switching and routing equipment, supporting multiple data rates from OC-48 and beyond.

Figure 2 illustrates how a search engine subsystem can be optimized using a host bridge ASIC (or a dedicated co-processor, such as the Cypress Semiconductor LNI8010), the M7010, and synchronous or non-synchronous SRAMs. It also illustrates how this system fits into a switch-router implementation.

Table 1. Product Range

| Part Number | Operating Supply Voltage | Operating I/O Voltage | Speed |
|---------------|--------------------------|-----------------------|-------|
| M7010R-083ZA1 | 1.8V | 2.5 or 3.3V | 83MHz |
| M7010R-066ZA1 | 1.8V | 2.5 or 3.3V | 66MHz |

Figure 2. Switch/Router Implementation Using the M7010



AI04272

Table 2. Signal Names

| Symbol | Type | Connection Name |
|---------------------------|------|------------------------------|
| Clocks and Reset | | |
| CLK2X | I | Master Clock |
| PHS_L | I | Phase |
| RST_L | I | Reset |
| Command and DQ Bus | | |
| CMD[8:0] | I | Command Bus |
| CMDV | I | Command Valid |
| DQ[67:0] | I/O | Address/Data Bus |
| ACK ⁽¹⁾ | T | READ Acknowledge |
| EOT ⁽¹⁾ | T | End of Transfer |
| SSF | T | SEARCH Successful Flag |
| SSV | T | SEARCH Successful Flag Valid |
| SADR[21:0] | T | SRAM Address |
| CE_L | T | SRAM Chip Enable |
| WE_L | T | SRAM WRITE Enable |
| OE_L | T | SRAM Output Enable |
| ALE_L | T | Address Latch Enable |

| | | |
|------------------------------|---|-------------------------------------|
| Cascade Interface | | |
| LHI[6:0] | I | Local Hit In |
| LHO[1:0] | O | Local Hit Out |
| BHI[2:0] | I | Block Hit In |
| BHO[2:0] | O | Block Hit Out |
| FULI[6:0] | I | Full In |
| FULO[1:0] | O | Full Out |
| FULL | O | Full Flag |
| Device Identification | | |
| ID[4:0] | I | Device Identification |
| Test Access Port | | |
| TDI | I | Test Access Port's Test Data In |
| TCK | I | Test Access Port's Test Clock |
| TDO | T | Test Access Port's Test Data Out |
| TMS | I | Test Access Port's Test Mode Select |
| TRST_L | I | Test Access Port's Reset |

Note: Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate

1. ACK and EOT Signals require a pull-down resistor of 47 ohms.

Figure 3. Connections

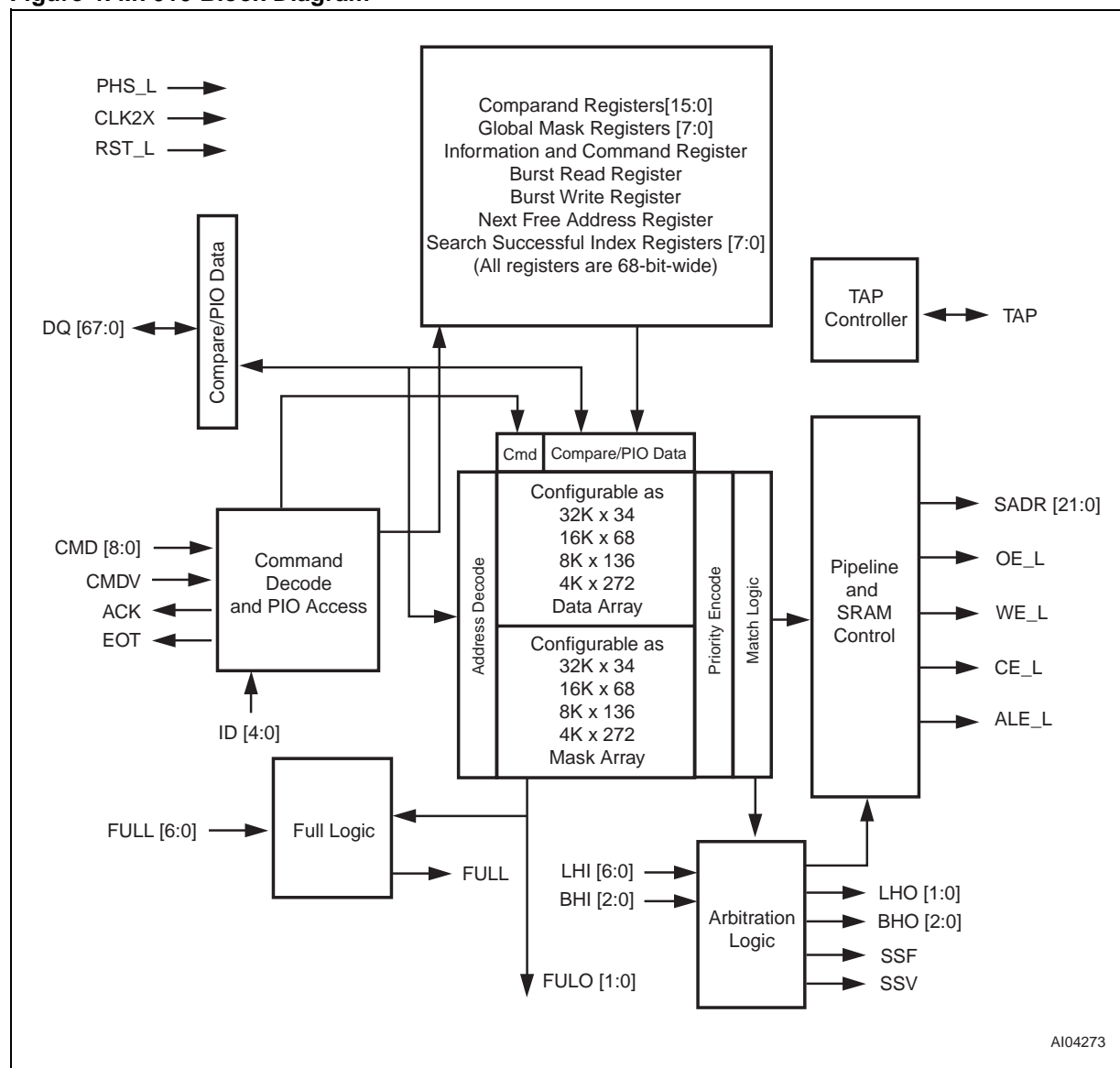
| | | | | | | | | | | | | | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|-------|------------------|------------------|------------------|-----------------|------------------|------------|------------------|-----------------|------------------|------------------|------------------|------------------|------------------|
| NC | GND | EOT | NC | NC | V _{DD} | FULI5 | FULI4 | FULI1 | BHO0 | V _{DD} | BHI0 | LHI6 | NC | V _{DD} | ID2 | ID0 | TDO | NC | NC |
| NC | NC | ACK | FULL | NC | FULO1 | NC | FULI6 | FULI2 | BHO1 | BHI2 | V _{DDQ} | LHI5 | LHI3 | LHI2 | ID3 | TMS | TDI | V _{DD} | NC |
| DQ64 | NC | NC | V _{DDQ} | V _{DD} | V _{DDQ} | NC | NC | V _{DDQ} | BHO2 | V _{DD} | LHO1 | LHI4 | V _{DDQ} | LHI0 | ID1 | TCK | NC | NC | DQ65 |
| DQ62 | NC | V _{DD} | GND | RSTL | NC | FULO0 | GND | FULI3 | FULI0 | BHI1 | LHO0 | GND | LHI1 | ID4 | T RST_L | GND | DQ63 | DQ61 | DQ57 |
| DQ60 | V _{DDQ} | NC | DQ66 | TOP | | | | | | | | | | | | DQ67 | DQ59 | NC | DQ53 |
| V _{DD} | NC | DQ56 | DQ58 | | | | | | | | | | | | | V _{DDQ} | DQ55 | DQ49 | V _{DD} |
| DQ50 | V _{DDQ} | DQ52 | DQ54 | | | | | | | | | | | | | DQ47 | V _{DDQ} | DQ51 | V _{DDQ} |
| NC | DQ46 | DQ48 | GND | | | | | | | | | | | | | GND | NC | DQ45 | DQ43 |
| DQ40 | DQ42 | V _{DDQ} | DQ44 | | | | | | | | | | | | | DQ41 | DQ39 | V _{DD} | DQ37 |
| V _{DD} | NC | DQ36 | DQ38 | | | | | | | | | | | | | V _{DDQ} | DQ35 | DQ33 | DQ31 |
| V _{DDQ} | DQ34 | DQ32 | DQ30 | | | | | | | | | | | | | V _{DDQ} | NC | DQ29 | V _{DD} |
| NC | DQ28 | V _{DDQ} | DQ26 | | | | | | | | | | | | | NC | DQ23 | DQ25 | DQ27 |
| DQ24 | V _{DD} | DQ20 | GND | | | | | | | | | | | | | GND | DQ19 | V _{DDQ} | DQ21 |
| DQ22 | DQ16 | DQ14 | V _{DDQ} | | | | | | | | | | | | | V _{DDQ} | NC | DQ15 | DQ17 |
| V _{DD} | DQ18 | V _{DDQ} | DQ6 | | | | | | | | | | | | | DQ9 | DQ11 | DQ13 | V _{DD} |
| NC | DQ12 | DQ8 | DQ0 | | | | | | | | | | | | | DQ1 | DQ5 | DQ7 | NC |
| DQ10 | NC | V _{DDQ} | GND | NC | CMD2 | CMD4 | GND | WE_L | CLK2X | V _{DD} | SADR 15 | GND | V _{DDQ} | SADR 5 | V _{DDQ} | GND | NC | NC | V _{DDQ} |
| DQ2 | DQ4 | V _{DD} | SSF | CMD6 | CMD3 | CMD0 | AE_L | OE_L | SADR 21 | SADR 18 | SADR 16 | SADR 12 | SADR 9 | SADR 7 | SADR 6 | NC | SADR 0 | V _{DD} | DQ3 |
| NC | NC | NC | SSV | CMD5 | CMD1 | CMDV | V _{DDQ} | PHS_L | V _{DDQ} | SADR 19 | V _{DDQ} | NC | SADR 10 | SADR 11 | NC | SADR 4 | SADR 3 | NC | NC |
| NC | NC | CMD8 | CMD7 | V _{DDQ} | V _{DD} | NC | CE_L | NC | V _{DD} | SADR 20 | SADR 17 | SADR 14 | SADR 13 | V _{DD} | SADR 8 | V _{DDQ} | SADR 2 | SADR 1 | NC |

LEFT RIGHT

BOTTOM

AI04270

Figure 4. M7010 Block Diagram



PART NUMBERING**Table 3. Ordering Information Scheme**

Example:

| | M70 | 10 | R | –083 | ZA | 1 | T |
|--|-----|----|---|------|----|---|---|
| Device Type | | | | | | | |
| M70 Search Engine | | | | | | | |
| Density | | | | | | | |
| 10 = 1Mb (16K x 68-bit Table Entries) | | | | | | | |
| Operating Supply Voltage | | | | | | | |
| R = $V_{DD} = 1.8V$ | | | | | | | |
| Speed | | | | | | | |
| –083 = 83 Million Searches per Second | | | | | | | |
| –066 = 66 Million Searches per Second | | | | | | | |
| Package | | | | | | | |
| ZA = PBGA, 272-count, 27mm x 27mm ⁽¹⁾ | | | | | | | |
| Temperature Range | | | | | | | |
| 1 = 0 to 70 °C | | | | | | | |
| Shipping Option | | | | | | | |
| Tape & Reel Packing = T | | | | | | | |

Note: 1. Where “Z” is the symbol for BGA packages and “A” denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.