



M28R400CT M28R400CB

Known Good Die

4 Mbit (256Kb x16, Boot Block) 1.8V Supply Flash Memory

FEATURES SUMMARY

■ SUPPLY VOLTAGE

- $V_{DD} = 1.65V$ to $2.2V$ Core Power Supply
- $V_{DDQ} = 1.65V$ to $2.2V$ for Input/Output
- $V_{PP} = 12V$ for fast Program (optional)

■ ACCESS TIME: 100ns

■ PROGRAMMING TIME

- $10\mu s$ typical
- Double Word Programming Option

■ COMMON FLASH INTERFACE

- 64 bit Security Code

■ MEMORY BLOCKS

- Parameter Blocks (Top or Bottom location)
- Main Blocks

■ BLOCK LOCKING

- All blocks locked at Power Up
- Any combination of blocks can be locked
- \overline{WP} for Block Lock-Down

■ SECURITY

- 64 bit user Programmable OTP cells
- 64 bit unique device identifier
- One Parameter Block Permanently Lockable

■ AUTOMATIC STAND-BY MODE

■ PROGRAM and ERASE SUSPEND

■ 100,000 PROGRAM/ERASE CYCLES per BLOCK

■ ELECTRONIC SIGNATURE

- Manufacturer Code: 20h
- Top Device Code, M28R400CT: 882Ah
- Bottom Device Code, M28R400CB: 882Bh

Figure 1. Delivery Form

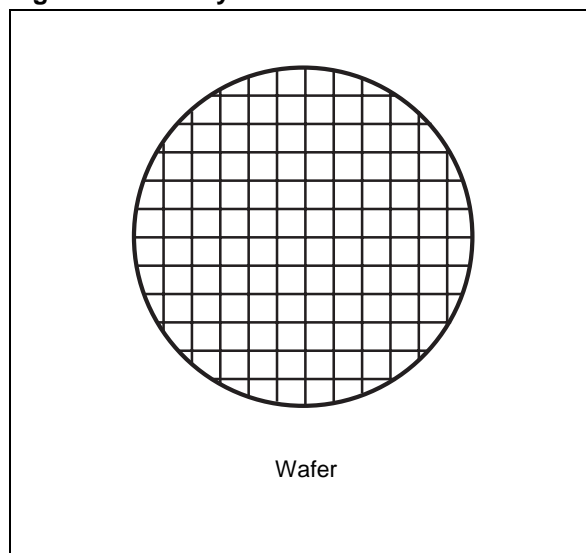


TABLE OF CONTENTS

SUMMARY DESCRIPTION	5
Figure 2. Logic Diagram	3
Table 1. Signal Names	3
FUNCTIONAL SPECIFICATION	4
Table 2. Product Specification	4
Table 3. Operating Conditions	4
Table 4. Read AC Characteristics	4
Table 5. Write AC Characteristics	4
Table 6. Physical Specification	4
Table 7. Manufacturing Information	4
DIE SPECIFICATIONS	5
Figure 3. Die Photograph and Pad Location	5
Figure 4. Wafer/Die Orientation	5
Table 8. Pad Extraction	6
PRODUCT TEST FLOW	7
Figure 5. Product Test Flow	7
HANDLING INSTRUCTIONS	
Processing	8
Storage	8
PART NUMBERING	9
Table 9. Ordering Information Scheme	9
REVISION HISTORY	10
Table 10. Document Revision History	10

SUMMARY DESCRIPTION

The M28R400C are available as Known Good Dice.

STMicroelectronics defines Known Good Dice as standard products offered as dice and tested for functionality and speed. ST's Known Good Die products are as reliable and of the same quality as products delivered in packages.

This datasheet should be read in conjunction with the full M28R400C datasheet.

The M28R400C is a 4 Mbit (256Kbit x 16) non-volatile Flash memory that can be erased electrically at the block level and programmed in-system on a Word-by-Word basis. These operations can be performed using a single low voltage (1.65 to 2.2V) supply. V_{DDQ} allows to drive the I/O pin down to 1.65V. An optional 12V V_{PP} power supply is provided to speed up customer programming.

The device features an asymmetrical blocked architecture. The M28R400C has an array of 15 blocks: 8 Parameter Blocks of 4 KWord and 7 Main Blocks of 32 KWord. M28R400CT has the Parameter Blocks at the top of the memory address space while the M28R400CB locates the Parameter Blocks starting from the bottom.

The M28R400C features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and block erase. When V_{PP} & V_{PPLK} all blocks are protected against program or block erase. All blocks are locked at power-up.

Each block can be erased separately. Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

The device includes a 128 bit Protection Register and a Security Block to increase the protection of a system design. The Protection Register is divided into two 64 bit segments, the first one contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. The Security Block, parameter block 0, can be permanently protected by the user.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller takes care of the tim-

ings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The M28R400C are supplied with all the bits erased (set to '1')

Figure 2. Logic Diagram

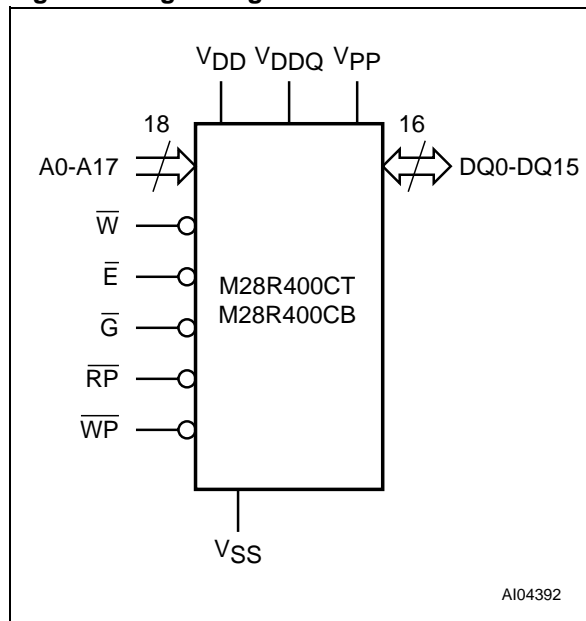


Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ15	Data Input/Output
\bar{E}	Chip Enable
\bar{G}	Output Enable
\bar{W}	Write Enable
\bar{RP}	Reset
\bar{WP}	Write Protect
V _{DD}	Core Power Supply
V _{DDQ}	Power Supply for Input/Output
V _{PP}	Optional Supply Voltage for Fast Program & Erase
V _{SS}	Ground

FUNCTIONAL SPECIFICATION

Refer to the M28R400C (document number 7653 on the ST Internet web site <http://www.st.com>) for full functional and electrical specifications of the product.

Tables 2 and 3 give the main product specification and operating conditions while Tables 4 and 5 summarize the Read and Write AC parameters which differ from those given in the M28R400C datasheet.

See Tables 6 and 7 for details of the die's physical specification and manufacturing.

Table 2. Product Specification

Product Root Part Number	M28R400CT M28R400CB
Speed Option	100ns
Delivery Form	Inked or mapped dice on whole unsawn wafer

Table 3. Operating Conditions

Supply Voltage	$V_{DD} = V_{DDQ} = 1.65V$ to $2.2V$
Junction Temperature Under Bias	T_J (max) = $125^{\circ}C$
Operating Temperature	$-40^{\circ}C$ to $+85^{\circ}C$

Table 4. Read AC Characteristics

Symbol	Description	Value	Unit
t_{AVAV}	Address Valid to Next Address Valid (min)	100	ns
t_{AVQV}	Address Valid to Output Valid (max)	100	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z (max)	25	ns
t_{ELQV}	Chip Enable Low to Output Valid (max)	100	ns
t_{GHQZ}	Output Enable High to Output Hi-Z (max)	25	ns
t_{GLQV}	Output Enable Low to Output Valid (max)	30	ns

Table 5. Write AC Characteristics

Symbol	Description	Value	Unit
t_{AVAV}	Address Valid to Next Address Valid (min)	100	ns
t_{ELQV}	Chip Enable Low to Output Valid (max)	100	ns

Table 6. Physical Specification

Die Dimensions, X by Y (with scribe line)	141.024 mils x 98.504 mils
	3.582mm x 2.502mm
Die Dimensions, X by Y (without scribe line)	137.008mils x 94.488mils
	3.480mm x 2.400mm
Die Thickness	9.84 mils
	725 μ m
Bond Pad Size	3.56 mils x 3.56 mils
	90.4 μ m x 90.4 μ m
Pad Area Free of Passivation	12.67 mils ²
	8172 μ m ²
Pad per Die	46
Bond Pad Metallization	AICU, TiN
Die Backside	No Metal
	May be grounded
Passivation	USG, Si ₃ N ₄

Table 7. Manufacturing Information

Manufacturing Location - Die Revision	Catania (M5 fab), Italy – V2
Manufacturing Location - Die Revision	Agrate (R2 fab), Italy – V1
Wafer Sort and Test Location	Agrate and Catania, Italy
Manufacturing ID	SA2B9AZ
Preparation for Shipment	Agrate and Catania, Italy
Fabrication Process	0.18 μ m technology

DIE SPECIFICATIONS

Figure 3. Die Photograph and Pad Location

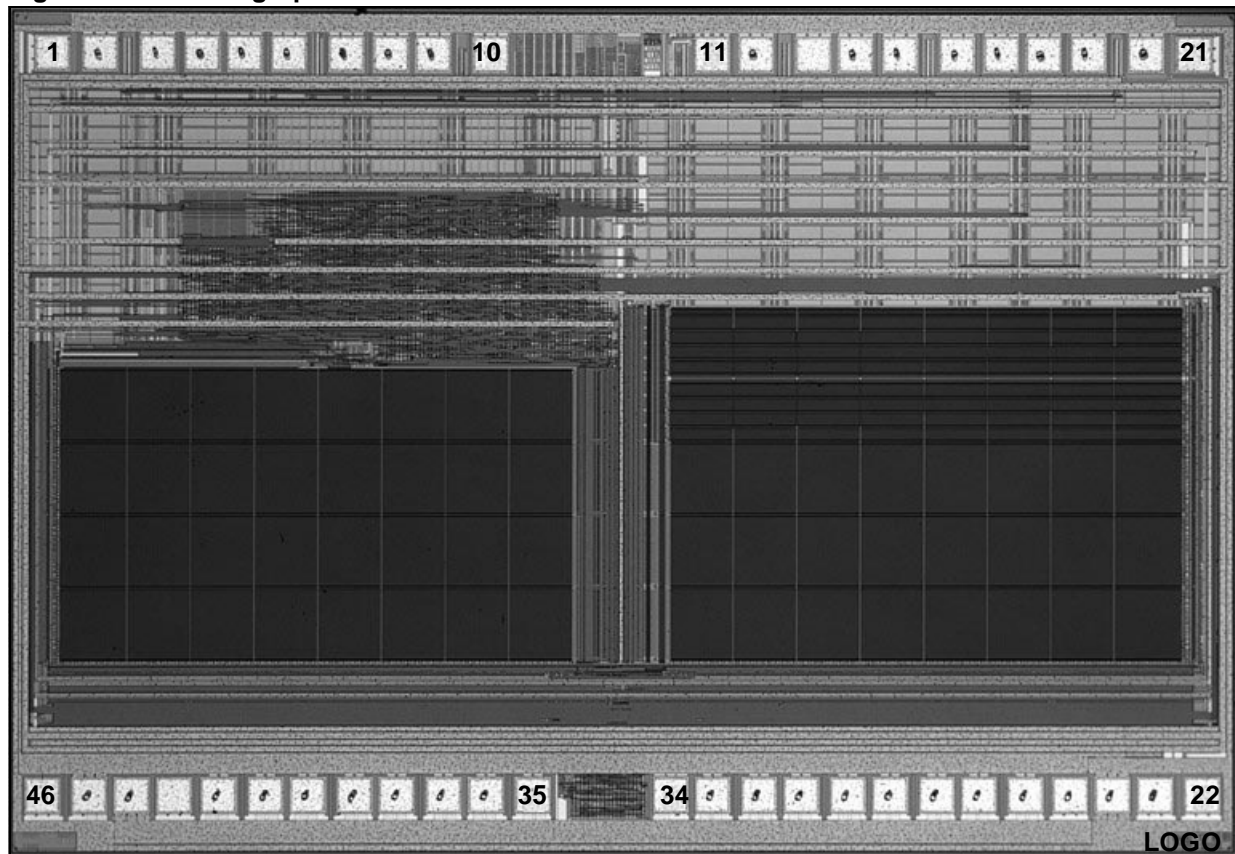
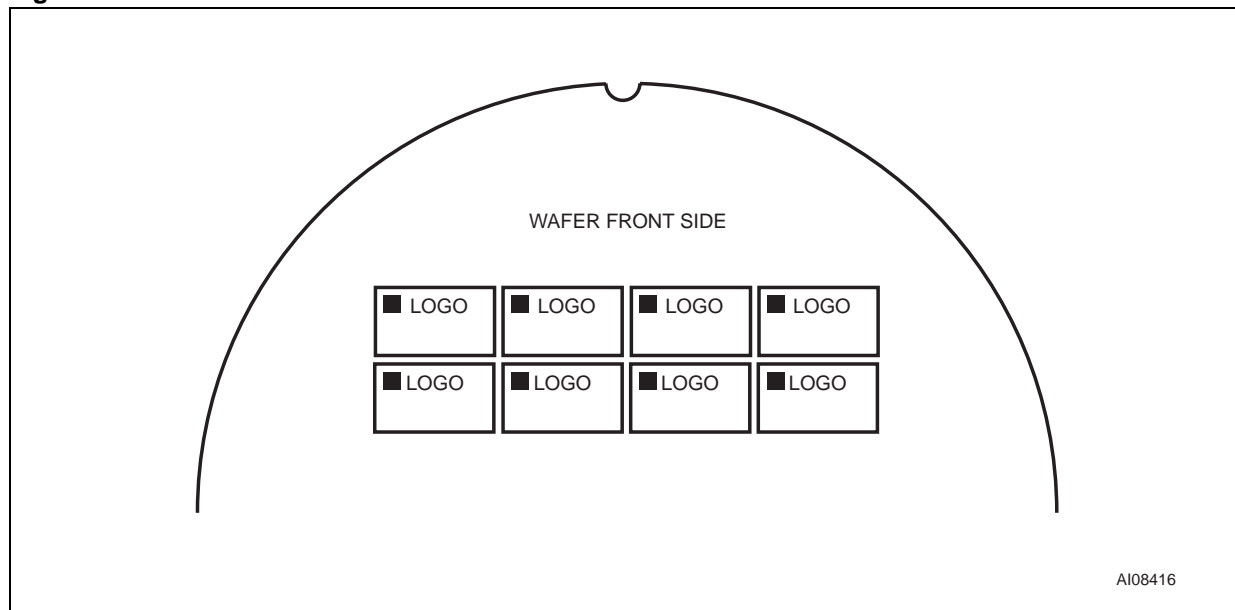


Figure 4. Wafer/Die Orientation



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Table 8. Pad Extraction

Pad Number	Pad Function	Pad Placement	
		X	Y
1	A15	-1612.24	1068.60
2	A14	-1477.72	1068.60
3	A13	-1315.88	1068.60
4	A12	-1190.28	1068.60
5	A11	-1071.16	1068.60
6	A10	-945.56	1068.60
7	A9	-783.72	1068.60
8	A8	-658.12	1068.60
9	\overline{W}	-539.00	1068.60
10	\overline{RP}	-377.16	1068.60
11	V _{PP}	249.16	1068.60
12	\overline{WP}	374.76	1068.60
13	NC	536.60	1068.60
14	A17	655.72	1068.60
15	A7	781.32	1068.60
16	A6	943.16	1068.60
17	A5	1068.76	1068.60
18	A4	1187.88	1068.60
19	A3	1313.48	1068.60
20	A2	1475.32	1068.60
21	A1	1609.84	1068.60
22	A0	1636.92	-1023.68
23	\overline{E}	1504.84	-1023.68

Pad Number	Pad Function	Pad Placement	
		X	Y
24	V _{SS}	1385.72	-1023.68
25	\overline{G}	1266.60	-1023.68
26	DQ0	1141.00	-1023.68
27	DQ8	1008.92	-1023.68
28	DQ1	889.80	-1023.68
29	DQ9	757.72	-1023.68
30	DQ2	638.80	-1023.68
31	DQ10	506.52	-1023.68
32	DQ3	387.40	-1023.68
33	DQ11	255.32	-1023.68
34	V _{DD}	136.20	-1023.68
35	DQ4	-255.08	-1023.68
36	DQ12	-387.16	-1023.68
37	DQ5	-506.28	-1023.68
38	DQ13	-638.36	-1023.68
39	DQ6	-757.48	-1023.68
40	DQ14	-889.56	-1023.68
41	DQ7	-1008.68	-1023.68
42	DQ15	-1140.76	-1023.68
43	NC	-1266.36	-1023.68
44	V _{SS}	-1385.48	-1023.68
45	V _{DDQ}	-1504.60	-1023.68
46	A16	-1636.68	-1023.68

- Note: 1. All pad placements are referred to the center of the chip and center of the pad. The coordinates can be used to operate wire bonding equipment.
 2. NC = Pad not connected.
 3. Dimensions are given in microns.

PRODUCT TEST FLOW

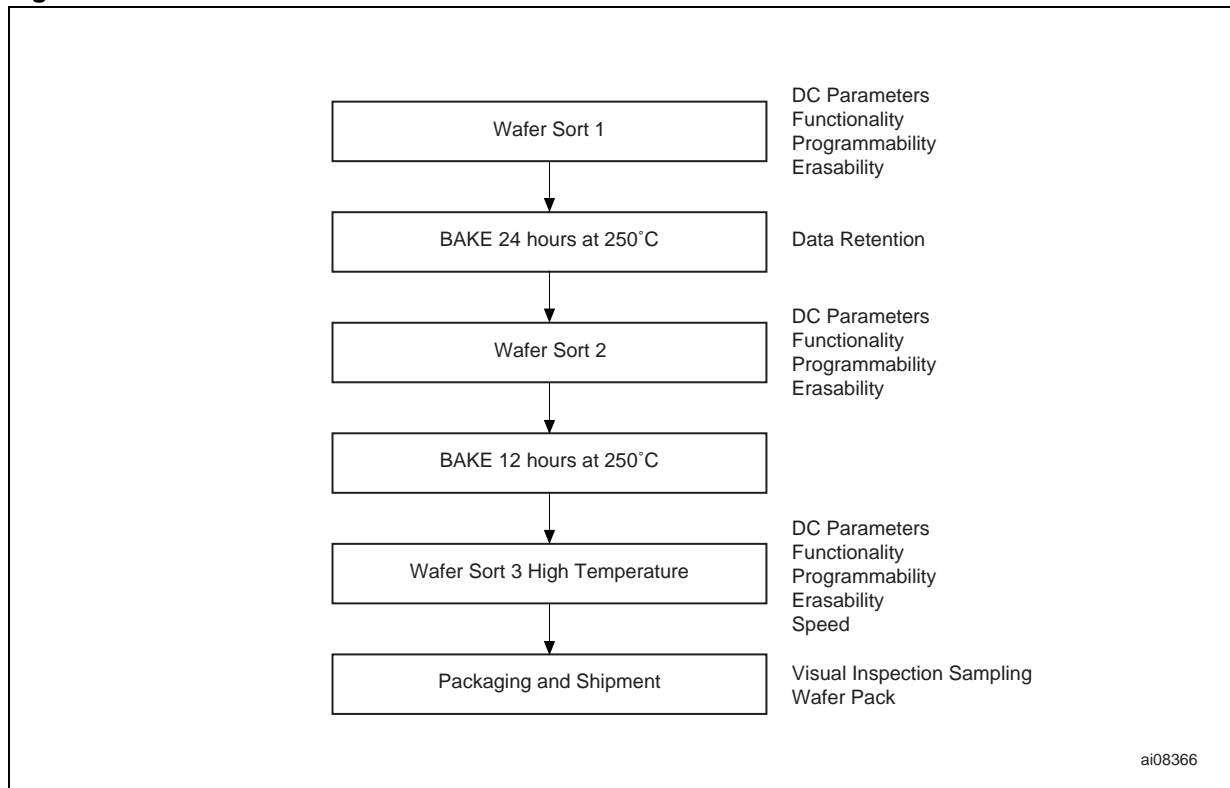
Figure 5 gives an overview of ST's Known Good Die test flow.

STMicroelectronics implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program is im-

plemented to ensure that ST's quality standards are met on Known Good Die products.

With ST's quality procedures, Known Good Die products can be produced without requiring burn-in.

Figure 5. Product Test Flow



HANDLING INSTRUCTIONS

Processing

Known Good Die products should not be exposed to ultraviolet light or be processed at temperatures greater than 250°C.

Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, ST recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

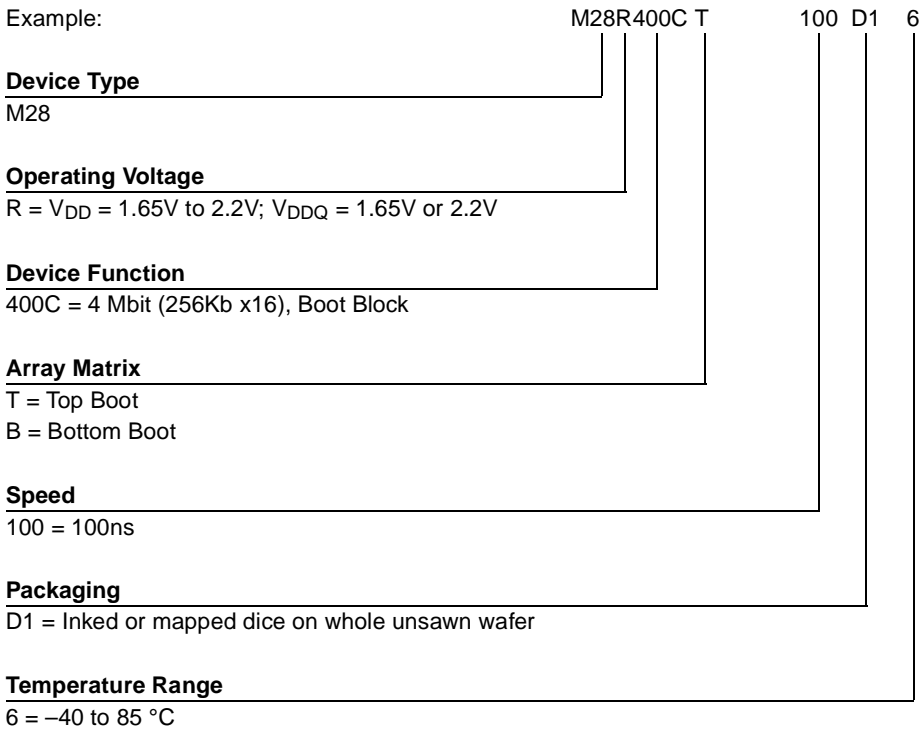
Storage

Known Good Die products should be stored at a maximum temperature of 30°C in a nitrogen-purged cabinet or a vacuum-sealed bag.

All standard ESD (ElectroStatic Discharge) handling procedures should be observed.

PART NUMBERING

Table 9. Ordering Information Scheme



Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed and Delivery Form) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 10. Document Revision History

Date	Version	Revision Details
12-Jun-2003	1.0	First Issue.

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