



STD60NH03L

N-CHANNEL 30V - 0.0075Ω - 60A - DPAK

STripFET™ III POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD60NH03L	30 V	< 0.009Ω	60 A

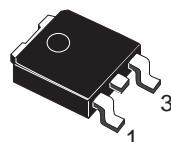
- TYPICAL R_{DS(on)} = 0.0075Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.009Ω @ 5 V
- R_{DS(on)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

The **STD60NH03L** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

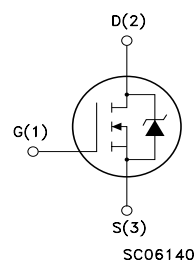
APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



**DPAK
TO-252**
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD60NH03LT4	D60NH03L	DPAK	TAPE & REEL

STD60NH03L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	30	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	60	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	43	A
$I_{DM}(1)$	Drain Current (pulsed)	240	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	70	W
	Derating Factor	0.47	W/ $^\circ\text{C}$
$E_{AS}(2)$	Single Pulse Avalanche Energy	300	mJ
T_{stg}	Storage Temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. Operating Junction Temperature		$^\circ\text{C}$

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case Max	2.14	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature for Soldering Purpose	275	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125\text{ }^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$ $V_{GS} = 5\text{ V}$, $I_D = 30\text{ A}$		0.0075 0.009	0.009 0.017	Ω Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (3)	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 30\text{ A}$		TBD		S
C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		2200		pF
C_{oss}	Output Capacitance			380		pF
C_{rss}	Reverse Transfer Capacitance			49		pF
R_G	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.5		Ω

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 30\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 5\text{ V}$ (see test circuit, Figure 3)		21		ns
t_r	Rise Time			95		ns
Q_g	Total Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 60\text{ A}$, $V_{GS} = 5\text{ V}$		15.7	21	nC
Q_{gs}	Gate-Source Charge			8.3		nC
Q_{gd}	Gate-Drain Charge			3.4		nC
Q_{gls} (4)	Third-Quadrant Gate Charge	$V_{DS} < 0\text{ V}$, $V_{GS} = 5\text{ V}$, $I_D = 60\text{ A}$		15		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 30\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 5\text{ V}$ (see test circuit, Figure 3)		19		ns
t_f	Fall Time			15		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				60	A
I_{SDM} (1)	Source-drain Current (pulsed)				240	A
V_{SD} (3)	Forward On Voltage	$I_{SD} = 30\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 60\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		32		ns
Q_{rr}	Reverse Recovery Charge			51		nC
I_{RRM}	Reverse Recovery Current			3.2		A

1. Pulse width limited by safe operating area
2. Starting $T_j = 25^\circ\text{C}$, $I_D = 30\text{ A}$, $V_{DD} = 20\text{ V}$
3. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
4. Gate charge for Synchronous Operation. See Appendix A

Fig. 1: Unclamped Inductive Load Test Circuit

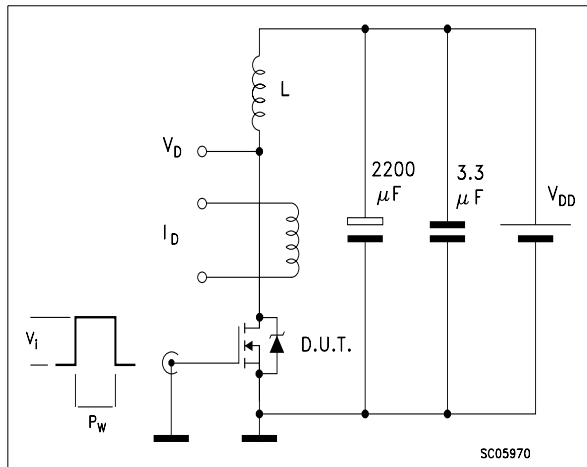


Fig. 2: Unclamped Inductive Waveform

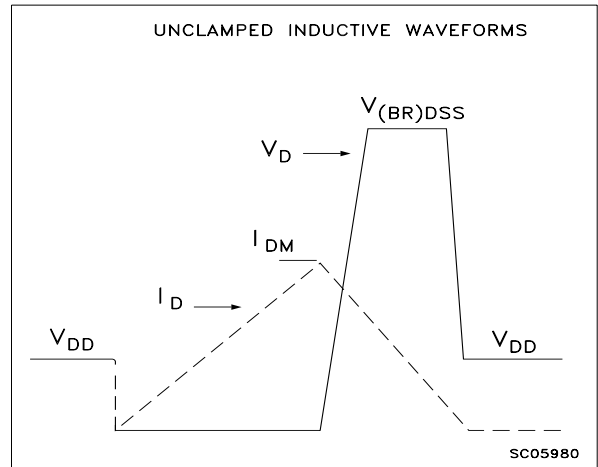


Fig. 3: Switching Times Test Circuit For Resistive Load

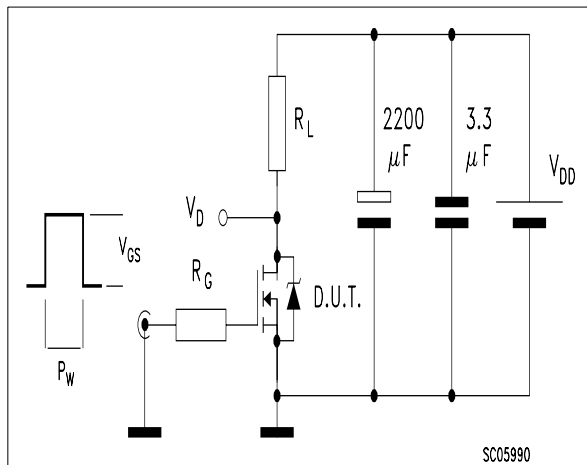


Fig. 4: Gate Charge test Circuit

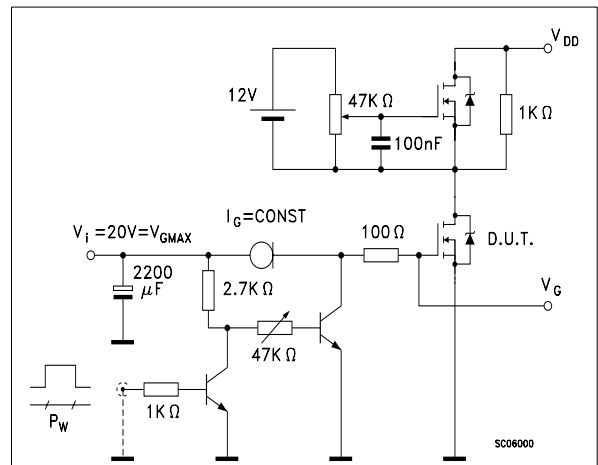
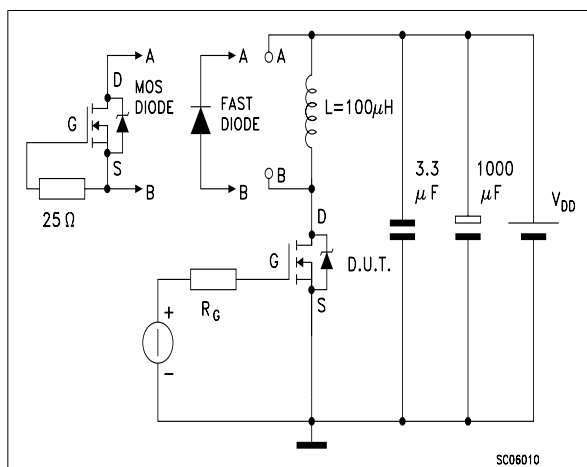
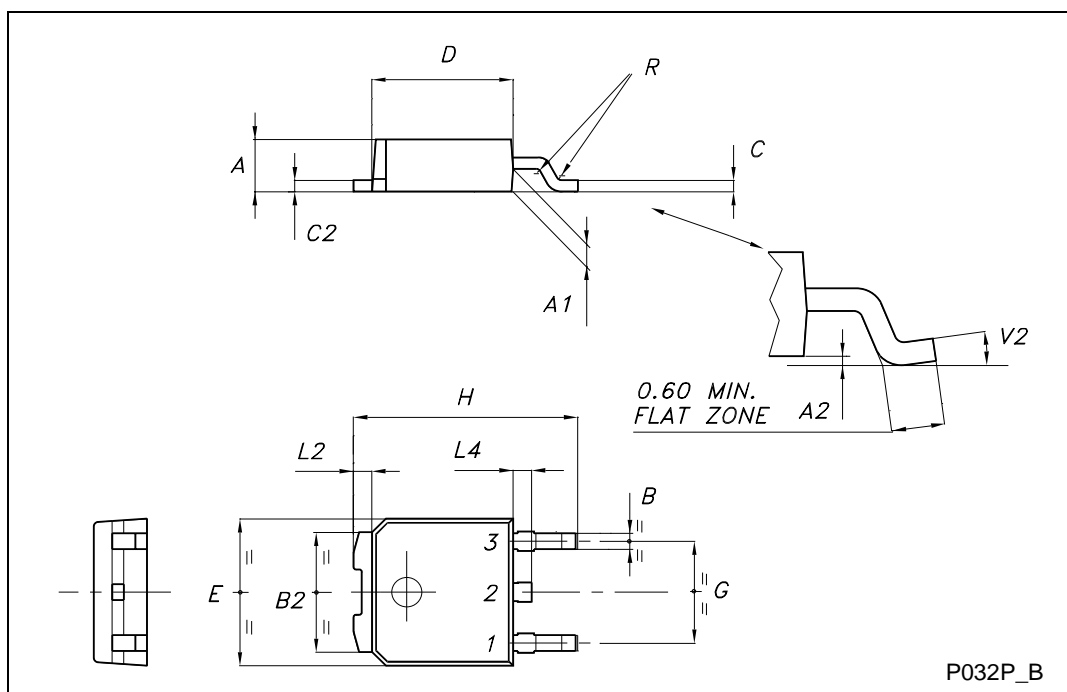


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

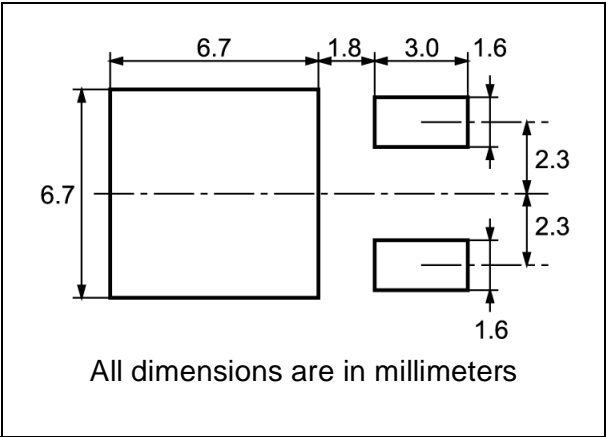


TO-252 (DPAK) MECHANICAL DATA

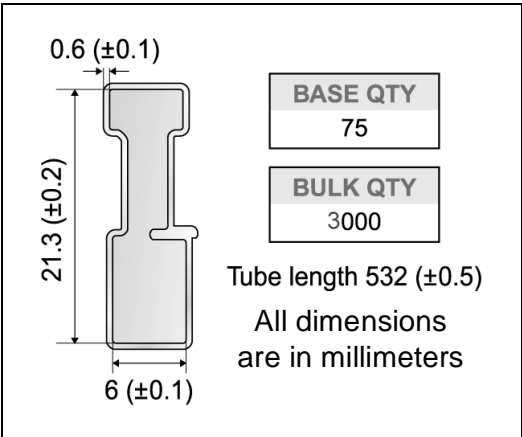
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



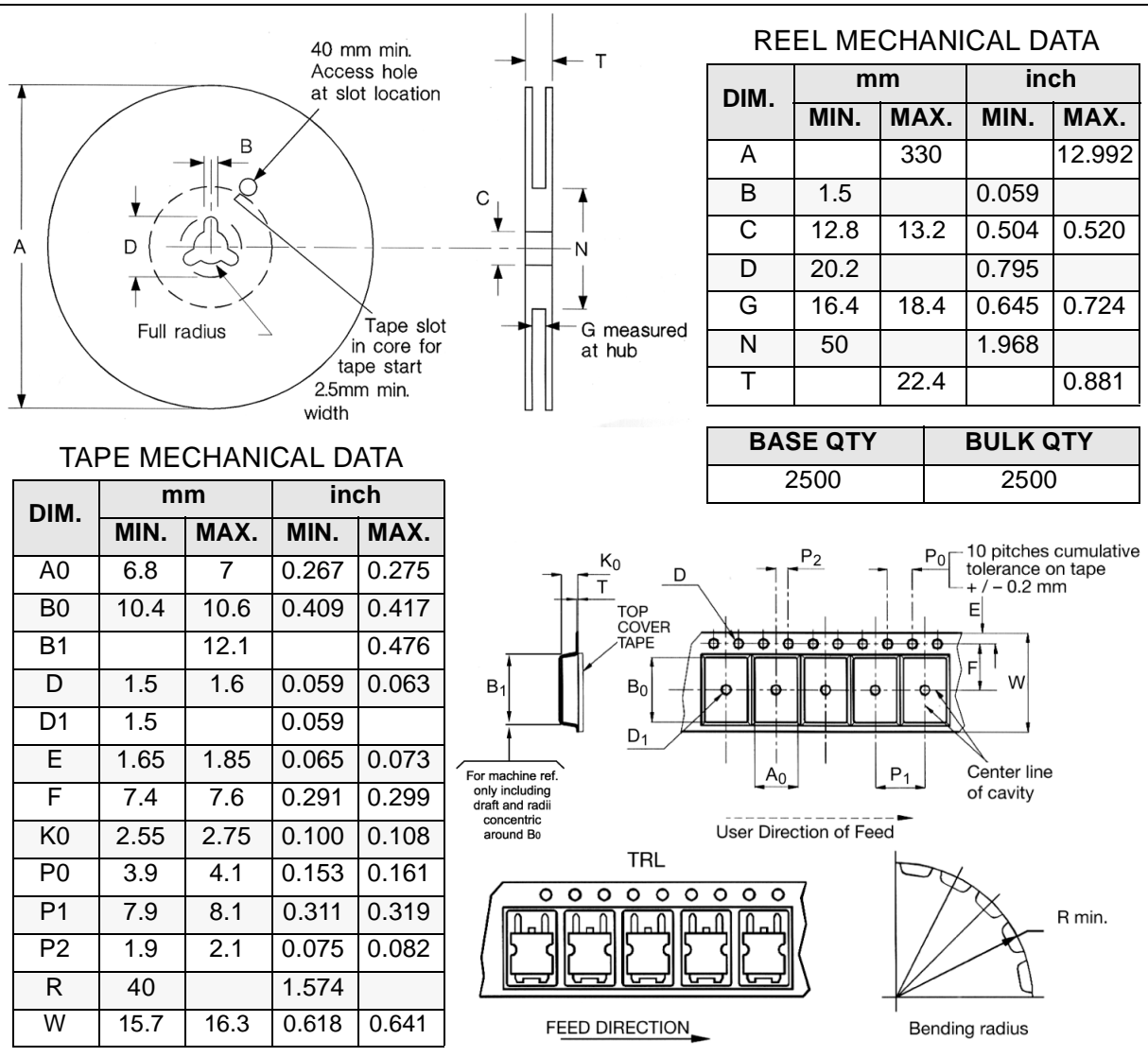
DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

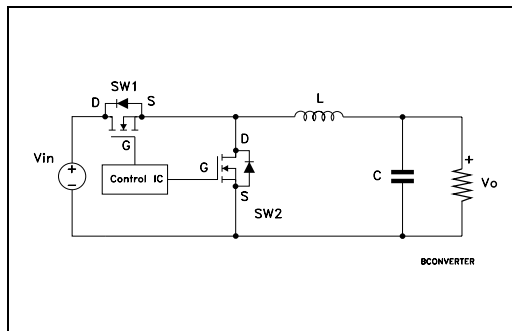


* on sales type

Appendix A: Buck Converter Power Losses Estimation

DESCRIPTION

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.



The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{GG} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
$P_{switching}$		$V_{in} * (Q_{gth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$1/2 V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{r(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_g)}$		$Q_{gs(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
δ	Duty-Cycle
Q_{gth}	Post Threshold Gate Charge
Q_{gls}	Third Quadrant Gate Charge
$P_{conduction}$	On State Losses
$P_{switching}$	On-off Transition Losses
P_{diode}	Conduction and Reverse Recovery Diode Losses
P_{diode}	Gate Drive Losses
P_{Qoss}	Output Capacitance Losses

¹ Dissipated by SW1 during turn-on

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