Spindle and loading motor driver for PD BA6852FP

The BA6852FP is a motor driver IC developed for use in PD, CD-ROM and DVD applications. In addition to having a conventional spindle motor driver, it includes a reversible motor driver for use with loading motors to allow easy system construction.

Applications

PD, CD-ROM and DVD.

Features

output.

- 1) Power save circuit (three-level switch) allows FG output in power save mode.
- put in power save mode. set using the
 2) FGSW allows selection between either three-phase composite output or single-phase output for the FG
- The output voltage for the loading motor driver can be set using the Vref pin.

Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	
Applid voltage	Vcc	7	v	
Applid voltage	VM1, 2	15	V	
Power dissipation	Pd	1700*1	mW	
Operating temperature	Topr	-20~+75	C	
Storage temperature	Tstg	-55~+150	Ĉ	
Junction temperature	Tjmax	150	C	
Output current		1300*2		
(spindle block) (loading block)	Ιομαχ	1000	mW	

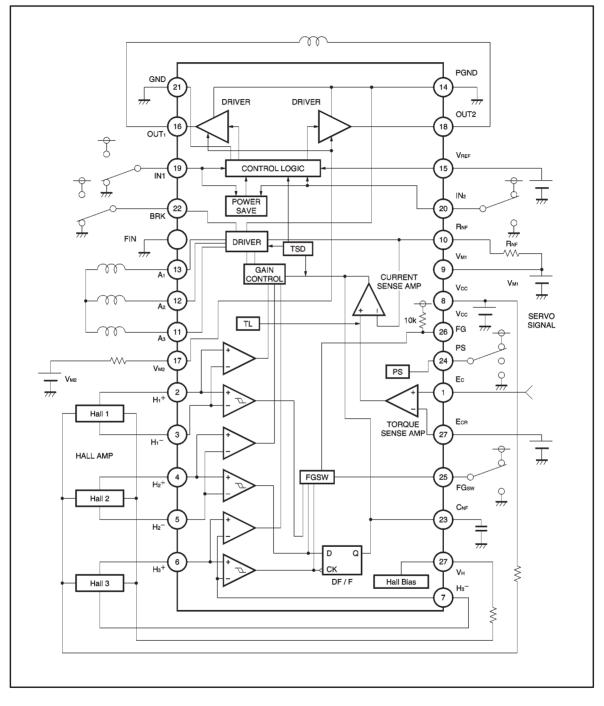
*1 When mounted on 70mm×70mm ×1.6mm glass epoxy board. Reduced by 13.6mW for each increase in Ta of 1℃ over 25℃.

*2 Should not exceed Pd or ASO values.

•Recommended operating conditions (Ta = 25° C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	4.5~5.5	V
(spindle block motor power supply)	V _{M1}	3~14	V
(loading block motor power supply)	V _{M2}	4.5~14	V

Block diagram



Pin descriptions

Pin No.	Pin name	Function
1	Ec	Spindle torque control
2	H1+	Hall signal input pin spindle
3	H1-	Hall signal input pin spindle
4	H2+	Hall signal input pin spindle
5	H2 [—]	Hall signal input pin spindle
6	H₃+	Hall signal input pin spindle
7	H₃	Hall signal input pin spindle
8	Vcc	Signal block power supply
9	V _{M1}	Spindle motor power supply
10	RNF	For connection of resistor for spindle output current detector
11	Аз	Spindle output A3
12	A2	Spindle output A2
13	A1	Spindle output A1
14	PGND	Driver GND
15	VREF	Loading output high level voltage setting
16	OUT1	Loading motor output 1
17	Vm2	Loading motor power supply
18	OUT2	Loading motor output 2
19	IN1	Loading logic input
20	IN2	Loading logic input
21	GND	Signal GND
22	BRK	Spindle brake
23	CNF	For connection of capacitor for spindle phase compensation
24	PS	Spindle power save
25	FGSW	Spindle FG output switch
26	FG	Spindle FG signal output
27	Vн	Hall bias
28	Ecr	Spindle torque control reference
FIN	FIN	Heatsink fin

* The heatsink fin must be connected to GND.



... 4:

Icc1							
Icc1					1	Measurement circuit	
	_	0.4	0.6	mA	Standby mode, $l_{PS} = -150 \mu A$	Fig.3	
Icc2	-	2.8	4.0	mA	Only Hall bias and FG operates	Fig.3	
Іссз	-	5.7	8.0	mA	Operation mode, Ec=EcR	Fig.3	
			1		1		
IPSON	-350	_	-150	μA	Standby mode	Fig.4	
IPSOP	-15	_	15	μA	Only Hall bias and FG operates	Fig.4	
IPSOFF	150	_	350	μA	Operation mode	Fig.4	
Vнв	-	0.9	1.5	V	IHB=10mA	Fig.5	
					1		
Іна	_	0.7	2.0	μA	_	Fig.6	
e Vhar	1.5	_	4.0	V	-	Fig.6	
VINH	50	-	_	mV _{P-P}	-	Fig.6	
VHYS	5	20	40	mV	_	Fig.12	
Ec, Ecr	1.0	-	4.0	V	_	Fig.7	
Ecof +	20	50	80	mV	With respect to Ec=2.5V	Fig.7	
E _{Cof} —	-80	-50	-20	mV	_	Fig.7	
ECIN	-3	-0.4	3	μA	Ec=2V, Ecr=2.5V	Fig.7	
GEC	0.4	0.5	0.6	A/V	Ec=1.5, 2.0V	Fig.7	
VSBON	3.5	_	-	V	Brake on mode	Fig.8	
VSBOFF	-	-	1.5	V	Brake off mode	Fig.8	
VswL	-	-	1.5	V	FG1 phase output	Fig.9	
е Vswн	3.5	—	_	V	FG3 phase composition output	Fig.9	
VFGH	4.5	4.9	5.0	V	IFg=−10 µ A	Fig.10	
VFGL	0	0.2	0.35	V	I⊧g=5.0mA	Fig.10	
Du	-	50	-	%	-	—	
Vон	_	1.0	1.5	v	lo=-600mA	Fig.11	
Vol	-	0.4	0.9	v	lo=600mA	Fig.11	
		50	85		Ec=0V Output open Fig.1		
	IPSOP IPSOFF VHB HA VHB IHA VHB EC, ECR ECof + ECof - ECof - ECof - ECof - VSBON VSBOFF VSWL VSWL VFGH VFGL Du VOH	IPSOP 15 IPSOFF 150 VHB - IHA - VHB - EC, ECR 1.0 ECof + 20 ECof + 20 ECof - -80 ECIN -3 GEC 0.4 VSBON 3.5 VSBOFF - VSWL - VSWL - VSWL 0 VFGH 4.5 VFGL 0 DU - VOH -	IPSOP 15 IPSOFF 150 VHB - 0.9 IHA - 0.7 VHB - 0.7 VHB - 0.7 VHB - 0.7 VHB - 0.7 VHR 1.5 - VHR 50 - VHR 50 - VHYS 5 20 EC, ECR 1.0 - ECof + 20 50 ECof + 20 50 ECof - -80 -50 ECIN -3 -0.4 GEC 0.4 0.5 VSBON 3.5 - VSBORFF - - VSWL - - VSWH 3.5 - VFGH 4.5 4.9 DU - 50 VOH - 1.0	IPSOP 15 15 IPSOFF 150 - 350 VHB - 0.9 1.5 IHA - 0.7 2.0 VHB - 0.7 2.0 VHB - 0.7 2.0 VHB - 0.7 2.0 VHR 1.5 - 4.0 VINH 50 - - VHYS 5 20 40 Ec, Ecr 1.0 - 4.0 Ecor + 20 50 80 VSBON 3.5 - - VSBOFF - - 1.5 VFGH 4.5 4.9 5.0	IPSOP 15 15 µA IPSOFF 150 - 350 µA VHB - 0.9 1.5 V IHA - 0.7 2.0 µA VHB - 0.7 2.0 µA VHR 1.5 - 4.0 V VINH 50 - - mVP.P VHYS 5 20 40 mV Ecor - 80 -50 mV Ecor - -80 -50 -20 mV Ecor - - 0.4 3 µA GEC 0.4 0.5 0.6 A / V VSBON 3.5	IPSOP -15 - 15 μ A Only Hall bias and FG operates IPSOFF 150 - 350 μ A Operation mode VHB - 0.9 1.5 V IHB=10mA IHA - 0.7 2.0 μ A - VHB 50 - - mVV - VHB 50 - - mVP.P - Ec.ECR 1.0 - 4.0 V - Ec.ECR 1.0 - 4.0 V - Ec.ECR - - 20 mV -	

 $\bigcirc \ensuremath{\mathsf{Not}}$ designed for radiation resistance.

Output limit current



840

mA

 $R_{NF}=0.5\Omega$

700

560

lτl

Fig.5

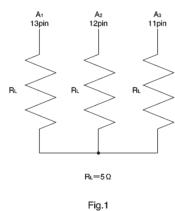
BA6852FP

Parameter	Symbol	Min.	Тур.	Max.	Unit	Coniditions	Measurement circuit
[Loading block]							
Circuit current 4	lcc4	12	24	36	mA	Forward or reverse mode	Fig.13
Circuit current 5	lcc5	29	48	67	mA	IN1="H", IN2="H"	Fig.13
Input voltage high level	Vін	2.1	—	-	V	_	Fig.13
Input voltage low level	Vı∟	_	-	0.8	V	_	Fig.13
High level input voltage	Ін	45	90	135	μA	VIN=2V	Fig.13
Outout saturation voltage*	Vce	_	1.0	1.5	V	lo=0.2A	Fig.14
VREF pin outflow current	IREF	_	2.0	5.0	μA	Io=0.1A, VREF=9V	Fig.15
VREF input voltage range	VREF	—	_	(V _{M2})-1	V	_	Fig.15

 $\ast\,$ The output saturation voltage is the sum of the upper and lower output Tr. ONot designed for radiation resistance.

Measurement circuits

(1) Measurement circuit resistance



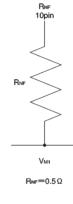


Fig.2

(2) Input/output table

	Input conditions						Output state						
								Forward			Reverse	e	
Pin No.	2	3	4	5	6	7	13	12	11	13	12	11	Measurement point
Pin Name	H1+	H1-	H ₂ +	H2 ⁻	H₃+	H₃−	A 1	A ₂	Аз	A 1	A 2	Аз	
Condition 1	L	М	н	М	М	М	н	L	L	L	н	н	13pin HIGH
Condition 2	н	М	L	М	м	м	L	н	н	н	L	L	13pin LOW
Condition 3	м	М	L	М	н	м	L	н	L	н	L	н	12pin HIGH
Condition 4	м	М	н	м	L	м	н	L	н	L	н	L	12pin LOW
Condition 5	н	М	М	М	L	м	L	L	н	н	н	L	11pin HIGH
Condition 6	L	м	М	м	н	м	н	н	L	L	L	н	11pin LOW
Note: Forward B	Note: Forward Ec < Ecr Input voltage H =								= 2.6V				

Reverse Ec > Ecr



(3) Measurement circuits

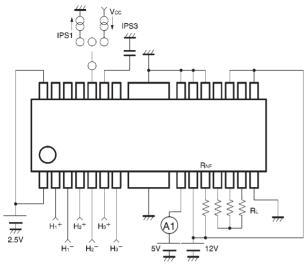
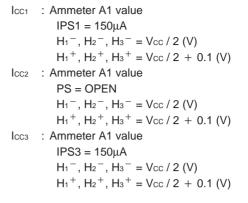
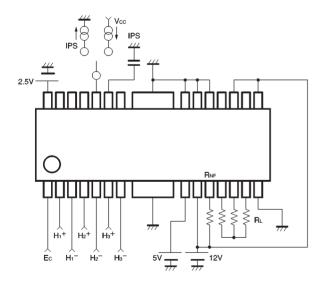


Fig.3





- IPSON : IPS range for which all output pins are open (input conditions 1 to 6)
- IPSOP : IPS range for only FG and the hall bias operate (input conditions 1 to 6)
- IPSOFF : PS range for which the output pins are as in the Input / output table (input conditions 1 to 6)

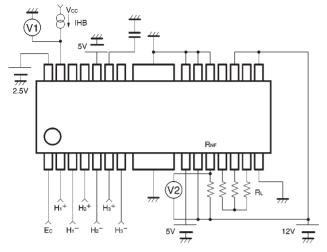
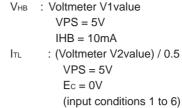
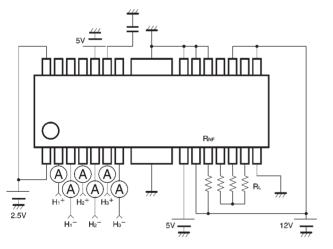


Fig.5







IHA : With $Hn^+ = 4.0V$, $Hn^- = 2.5V$, the current that flows into Hn^+ With $Hn^+ = 2.5V$, $Hn^- = 4.0V$, the current that flows into Hn^-

(n = 1, 2, 3)

- V_{HAR} : Hall input voltage range for which the output pin is as per the Input / output table.
- V_{INH} : Hall input level for which the output pin is as per the Input / output table. $| Hn^+ - Hn^- I$ $Hin^- = 2.5V$

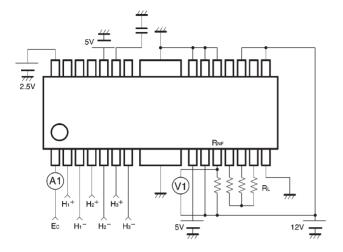
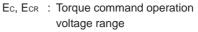


Fig.7



EcoF± : Vary Ec until EcR = 2.5V, then Vary Ec voltmeter V1 < 3mV. This Ec voltage range (see operation notes (2)).

ECIN : Ammeter value when Ec = 2V and Ecr = 2.5V

 $\begin{array}{ll} G_{\text{EC}} & : \mbox{ If the V1 value is V2 when} \\ & E_{\text{C}} = 1.5 \mbox{V}, \mbox{ and the V1} \\ & \mbox{ value is V3 when } E_{\text{C}} = 2.0 \mbox{V} \\ & \mbox{ G}_{\text{EC}} = \left\{ \left(\mbox{V2} - \mbox{V3} \right) / (2.0 - 1.5) \right\} / \\ & \mbox{ } R_{\text{NF}} \left(\mbox{ R}_{\text{F}} = 0.5 \Omega \right) \\ \end{array}$

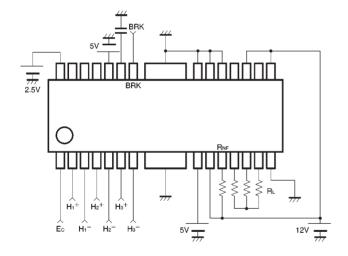
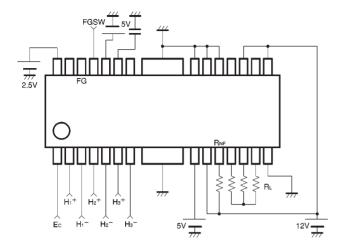


Fig.8

- VSBON : BRK pin voltage range when all output pins are low.
- VSBOFF : BRK pin voltage range when all output pins are as per the Input / output table.



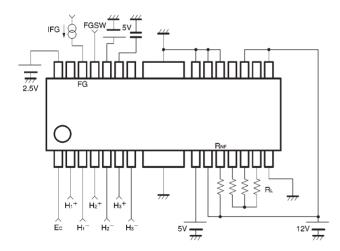


V_{SWL} : FGSW pin voltage range when the hall input and FG output are as per the table below.

H1 ⁺	H ₂ +	H₃+	FG	
L	н	н	L	
Н	L	L	н	_
H=2.6\				

V_{SWH} : FGSW pin voltage range when the hall input and FG output are as per the table below.

H1+	H2+	H₃+	FG
L	L	Н	L
Н	L	Н	Н
Н	L L		L
Н	н	L	н
L	н	L	L
L	н	н	Н
H=2.6V, L	Hn ⁻ =2.5V		





 V_{FGH} : Voltmeter V1 value (Input / output table, condition 2) IFG = $-10\mu A$ FGSW = 0V

 V_{FGL} : Voltmeter V1 value (Input / output table, condition 1) IFG = 3mA FGSW = 0V

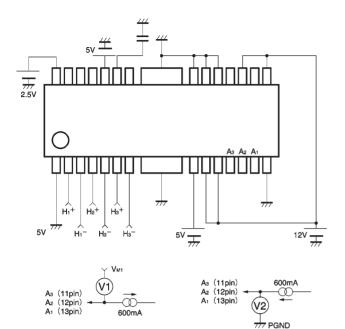
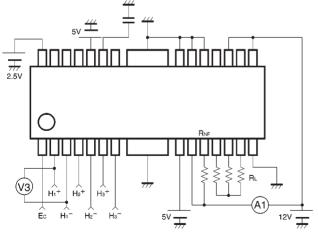


Fig.11

- VoH : With the output measurement pin made high level according to the input conditions, the V1 value when 600mA flows from that pin.
- VoL : With the output measurement pin made low level according to the input conditions, the V2 value when 600mA flows from that pin.



 H_1^+ and H_1^- that switch the FG pin. Ec = 2.5V FGSW = 0V

VHYS : The voltage difference V3 between

 I_{VMD} : Ammeter A1value $Output \ open \ (input \ conditions \ 1 \ to \ 6) \\ E_{\text{C}} = 0V$

Fig.12



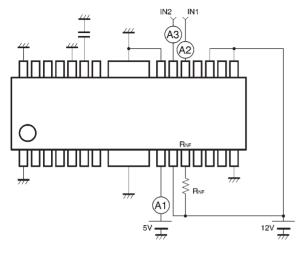


Fig.13

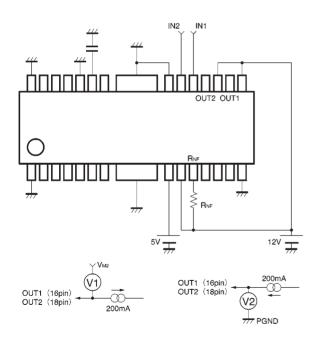
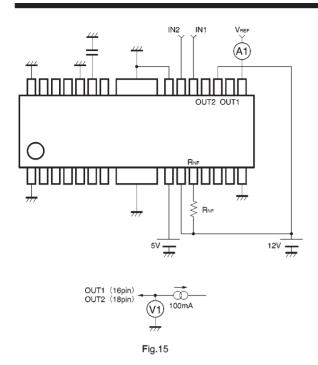


Fig.14

- I_{CC4} : Ammeter A1 value IN1 = 5V, IN2 = 0V
- I_{CC5} : Ammeter A1 value IN1 = 5V, IN2 = 5V
- V_{IH} : IN1 range for which OUT1 = High, OUT2 = Low (IN2 = Low)

IN2 range for which OUT1 = Low, OUT2 = High (IN1 = Low)

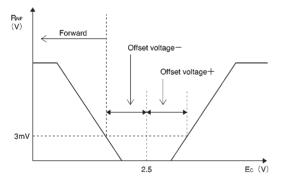
- V_{IL} : IN1 range for which OUT1 = Low, OUT2 = High (IN2 = High) IN2 range for which OUT1 = High, OUT2 = Low (IN1 = High)
- I_{IH} : Ammeter A2 value when IN1 = 2VAmmeter A3 value when IN2 = 2V
- VCE : Sum of V1 (the value when 200mA is flowing from the output high level pin) and V2 (the value when 200mA is flowing to the output low level pin).



- IREF : Ammeter A1 value Io = 100mA $V_{REF} = 9V$
- VREF : VREF pin voltage range for which the output voltage can be controlled

- Operation notes
- (1) Torque command

The R_{NF} pin voltage with respect to the torque command input (EC) is as follows.





	Rotation direction
Ec <ecr< td=""><td>Forward</td></ecr<>	Forward
Ec>Ecr	Reverse*

* Stops after reverse is detected.

The I / O gain G_{EC} from the Ec pin to the R_{NF} (output current) is determined by the R_{NF} detector resistance.

$$G_{EC} = 0.25 / R_{NF} (A / V)$$

The torque limit current $I_{\mathsf{T}\mathsf{L}}$ is given by

$$I_{TL} = 0.35 / R_{NF} (A).$$

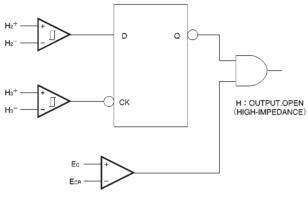
(2) Power save

The power save pin logic is as follows.

Mode	PS pin			
Power save mode	Outflow or pulled down to GND			
FG, hall bias operation mode	Open			
Spindle operation mode	Inflow or pulled up to Vcc			

(3) Reverse rotation detector

The construction of the reverse rotation detector circuit is shown in Fig. 17.



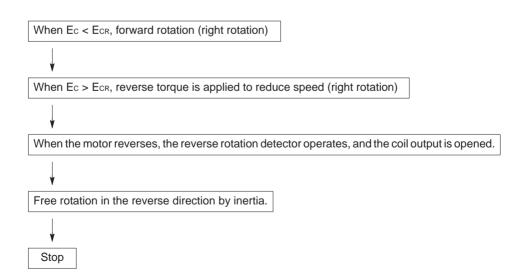


1) Forward (Ec < Ecr)

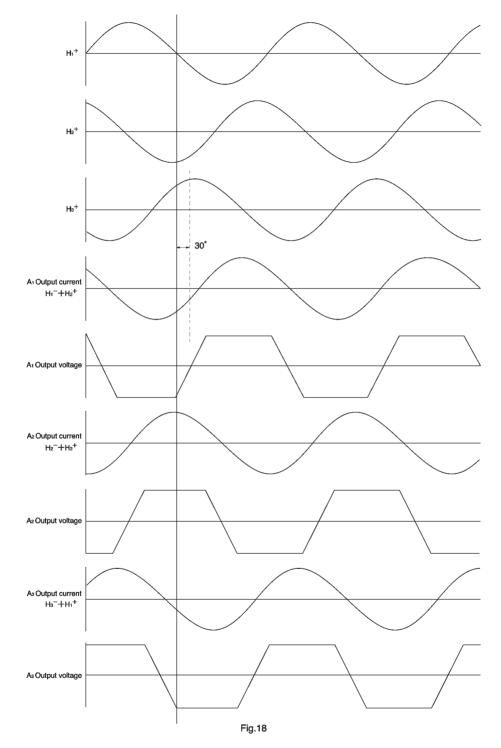
The phase relationship between the hall input signals H_2^+ and H_3^+ is as shown in Fig.18, and the reverse rotation detector circuit does not operate. 2) Reverse (Ec > EcR)

The phase relationship between H_2^+ and H_3^+ is opposite to that for forward rotation, and the reverse rotation detector circuit operates to switch the output off and leave it in the open state.

Motor operation during reverse detection

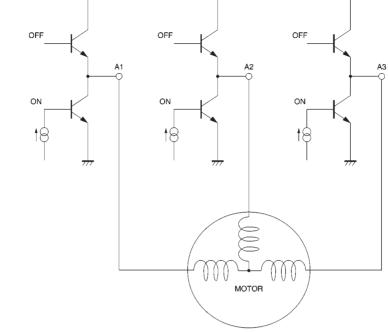


(4) Input / output timing chart (forward rotation)



BA6852FP







When the BRK pin goes to high level, the upper-side output transistors (three phase) go off, and the lower-side output transistors (three phase) go on.

(6) Hall input

The hall pins can be connected in series or parallel.

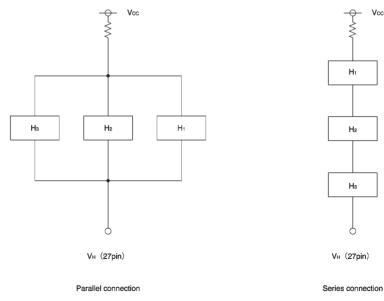


Fig.20



(7) FG output switch

The relationship between the FG output switch pin and the FG output is as follows.

	FG output mode
FGSW="H"	Three-phase composite output
FGSW="L"	Single-phase output

(8) About the input pin applied voltage

Do not apply voltage to any of the other pins when the Vcc voltage is not being supplied to the IC. In addition, when Vcc is being applied, do not apply a voltage more than Vcc to any of the other pins.

(9) Input pins

The loading input pin has a negative temperature characteristic, so when using it, give due consideration to the temperature characteristics. (10) V_{REF} pin (output high level voltage setting)

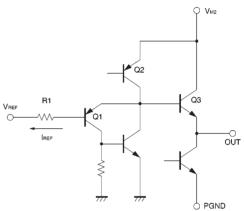
The loading block output high level voltage can be set using the $V_{\mbox{\scriptsize REF}}$ pin voltage.

The output high level voltage $V_{\mbox{\scriptsize OH}}$ is given by the following formula.

 $V_{\text{OH}} = V_{\text{REF}} + I_{\text{REF}} \times \text{R1} + \text{VBE} (\text{Q1}) - \text{VBE} (\text{Q3})$

The V_{REF} voltage that brings about the above formula is up to $V_{\text{M2}}-V_{\text{CE}}$ (Q2) – VBE (Q3).

Do not apply a voltage of more than V_{M2} to the V_{REF} pin. Short the V_{REF} pin to V_{M2} if you will not use it.





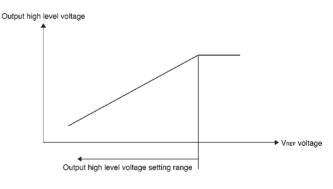


Fig.22

(11) Spindle and loading operation conditions

When IN1 or IN2 are high level, the spindle is off regardless of the PS pin input.

PS	Spindle operation mode	IN1	IN2	OUT1	OUT2
*	Refer to item (2) of the operation notes	L	L	OPEN	OPEN
**	OPEN	Н	L	Н	L
**	OPEN	L	н	L	н
**	OPEN	Н	Н	L	L

* : Refer to item of (2) the operation notes.

** : All input patterns.

(12) Driver section ground (GND)

PGND (pin 14) is the driver section GND, and is not connected to the signal section GND. This is the motor current path, so take care with the PCB track width and arrangement on the PC board.

(13) Thermal shutdown (TSD)

When the junction temperature reaches 175°C (Typ.), the motor output is opened. There is approximately 15°C (Typ.) of temperature hysteresis.

Electrical characteristics curves

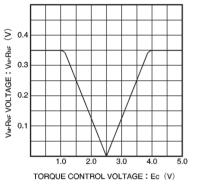


Fig.23 Torque gain / limit characteristics

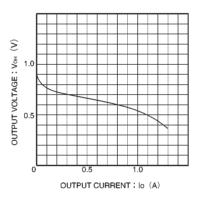


Fig.24 Spindle upper-side output saturation characteristics

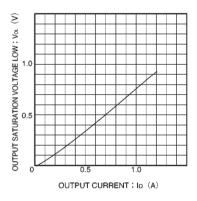


Fig.25 Spindle lower-side output saturation characteristics

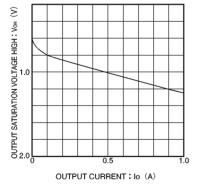
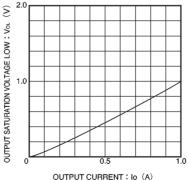


Fig.26 Loading section upper-side output saturation characteristics



OUTPUT CURRENT : 10 (A)

Fig.27 Loading section lower-side output saturation characteristics

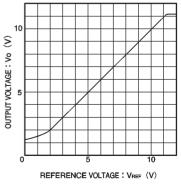


Fig.28 VREF VOUT characteristics



•External dimensions (Units: mm)

