Am29BL802C

8 Megabit (512 K x 16-Bit)
CMOS 3.0 Volt-only Burst Mode Flash Memory

DISTINCTIVE CHARACTERISTICS

- **32 words sequential with wrap around (linear 32), bottom boot**
- **One 8 Kword, two 4 Kword, one 48 Kword, three 64 Kword, and two 128 Kword sectors**
- **Single power supply operation**
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Read access times**

  Burst access times as fast as 17 ns at industrial temperature range (18 ns at extended temperature range)

  Initial/random access times as fast as 65 ns
- **Alterable burst length via BAA# pin**
- **Power dissipation (typical)**
  - — Burst Mode Read: 15 mA @ 25 MHz, 20 mA @ 33 MHz, 25 mA @ 40 MHz
  - — Program/Erase: 20 mA
  - — Standby mode, CMOS: 3 µA
- **5 V-tolerant data, address, and control signals**
- **Sector Protection**
  - — Implemented using in-system or via programming equipment
  - — Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention**
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
  - — Backward-compatible with AMD Am29LV and Am29F flash memories: powers up in asynchronous mode for system boot, but can immediately be placed into burst mode
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device for reading array data
- **Package Option**
  - — 56-pin SSOP

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GENERAL DESCRIPTION

The Am29BL802C is an 8 Mbit, 3.0 Volt-only burst mode Flash memory devices organized as 524, 288 words. The device is offered in a 56-pin SSOP package. These devices are designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply. A 12.0-volt V_{PP} or 5.0 V_{CC} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 65, 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Burst Mode Features

The Am29BL802C offers a Linear Burst mode—a 32 word sequential burst with wrap around—in a bottom boot configuration only. This devices require additional control pins for **burst operations**: Load Burst Address (LBA#), Burst Address Advance (BAA#), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

AMD Flash Memory Features

Each device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. The I/O and control signals are 5V tolerant.

The Am29BL802C is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

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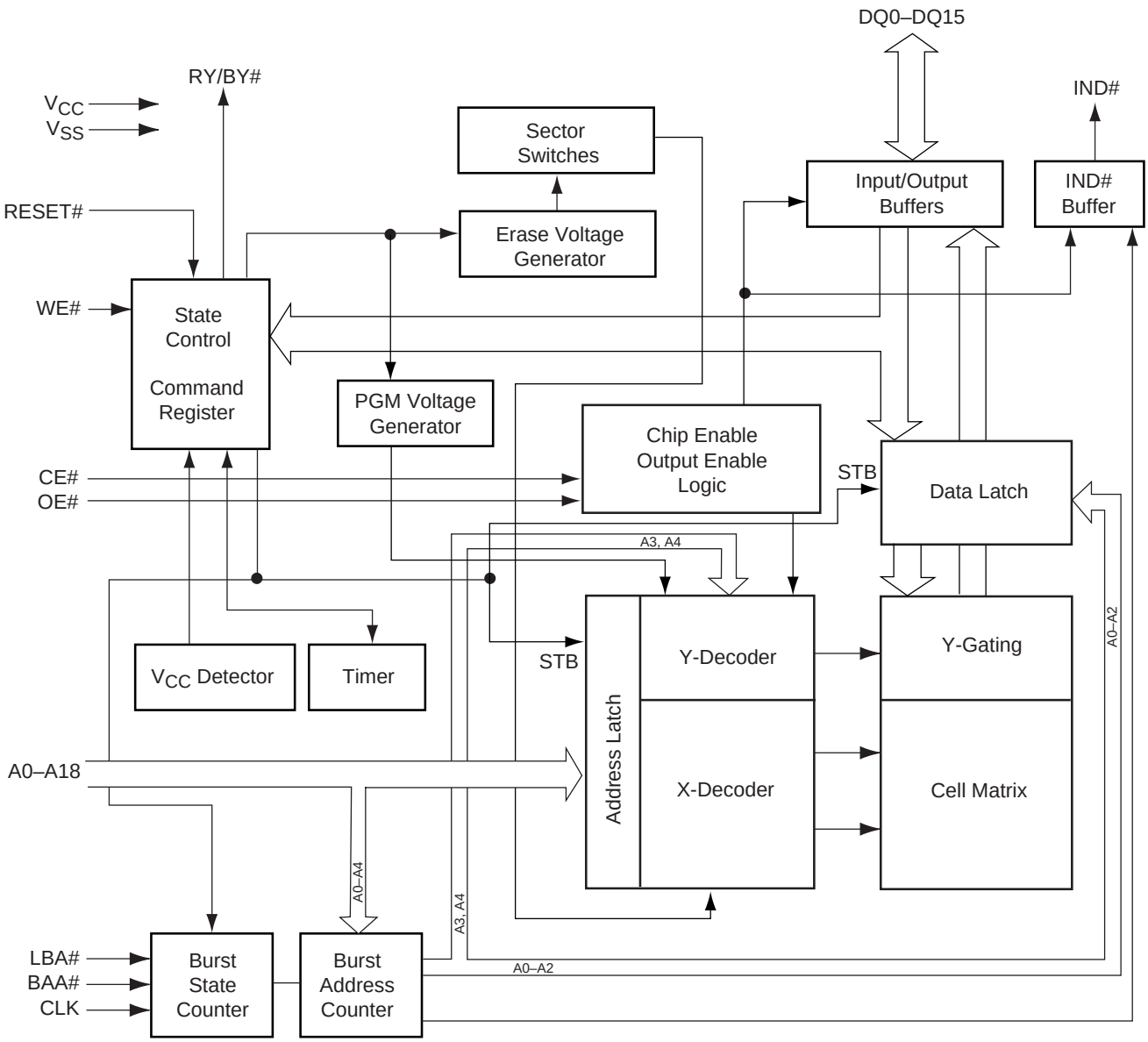
PRODUCT SELECTOR GUIDE

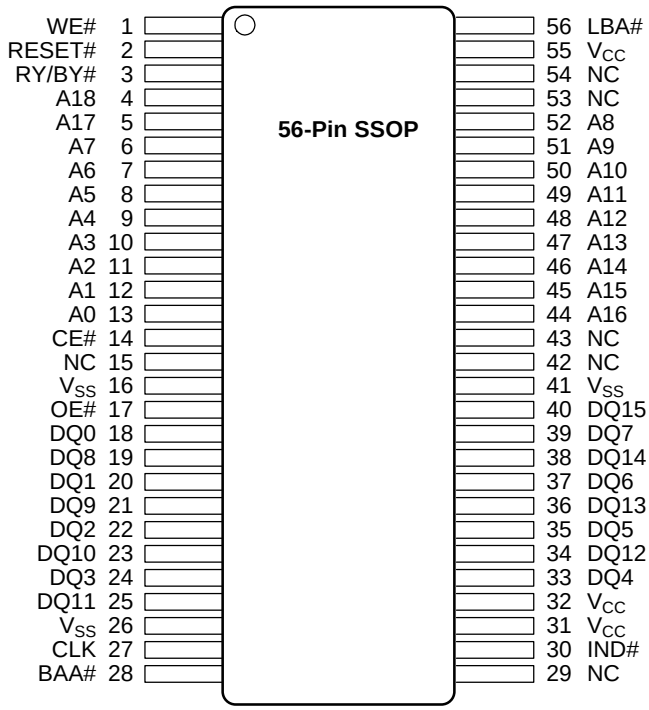
Family Part Number		Am29BL802C				
Speed Option	Regulated Voltage Range: V_{CC} =3.0–3.6 V	65R		70R	90R	120R
	Temperature Range: Industrial (I), Extended (E)	I	E	I, E	I, E	I, E
Max access time, ns (t_{ACC})		65		70	90	120
Max CE# access time, ns (t_{CE})		65		70	90	120
Max burst access time, ns (t_{BACC})		17	18	24	26	26

Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS



PIN CONFIGURATION

A0–A18 = 19 addresses

DQ0–DQ15 = 16 data inputs/outputs

CE# = Chip Enable Input. This signal shall be asynchronous relative to CLK for the burst mode.

OE# = Output Enable Input. This signal shall be asynchronous relative to CLK for the burst mode.

WE# = Write enable. This signal shall be asynchronous relative to CLK for the burst mode.

V_{SS} = Device ground

NC = No connect. Pin not connected internally

RY/BY# = Ready Busy output

CLK = Clock Input that can be tied to the system or microprocessor clock and provides the fundamental timing and internal operating frequency. CLK latches input addresses in conjunction with LBA# input and increments the burst address with the BAA# input.

LBA# = Load Burst Address input. Indicates that the valid address is present on the address inputs.

LBA# Low at the rising edge of the clock latches the address on the address inputs into the burst mode Flash device. Data becomes available t_{PACC} ns of initial access time after the rising edge of the same clock that latches the address.

LBA# High indicates that the address is not valid

BAA# = Burst Address Advance input. Increments the address during the burst mode operation

BAA# Low enables the burst mode Flash device to read from the next word when gated with the rising edge of the clock. Data becomes available t_{BACC} ns of burst access time after the rising edge of the clock

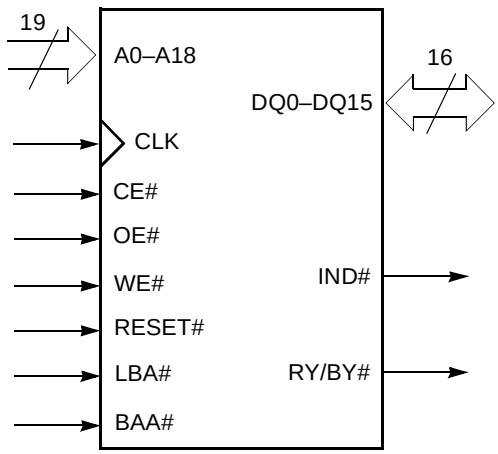
BAA # High prevents the rising edge of the clock from advancing the data to the next word output. The output data remains unchanged.

IND# = Highest burst counter address reached. IND# is low at the end of a 32-word burst sequence (when word Da + 31 is output). The output will wrap around to Da on the next CLK cycle (with BAA# low).

RESET# = Hardware reset input

Note: *The address, data, and control signals (RY/BY#, LBA, BAA, IND, RESET, OE#, CE#, and WE#) are 5 V tolerant.*

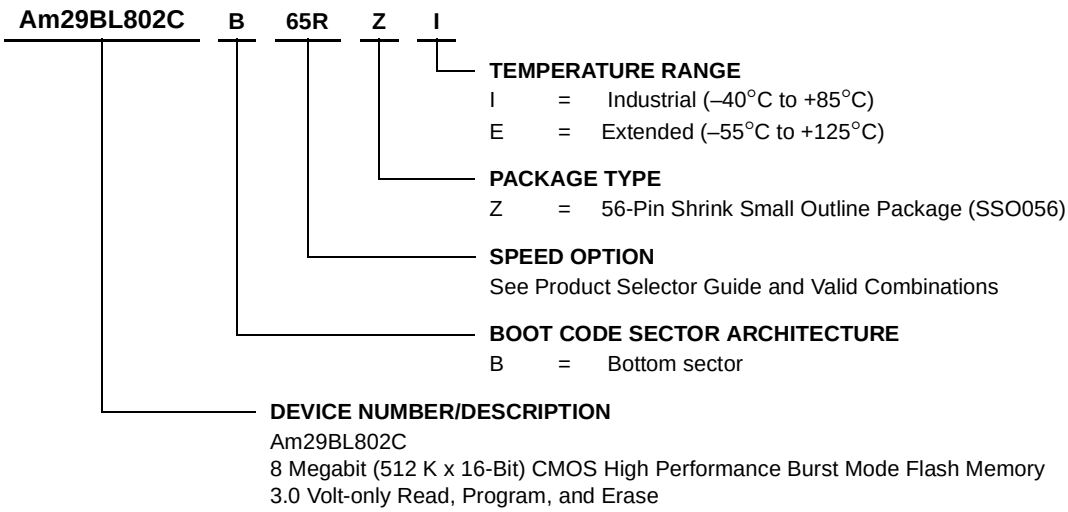
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29BL802CB-65R	ZI, ZE
Am29BL802CB-70R	ZI, ZE
Am29BL802CB-90R	ZI, ZE
Am29BL802CB-120R	ZI, ZE

For information on full voltage range options (2.7–3.6 V), please contact AMD.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	CLK	LBA#	BAA#	Addresses (Note 1)	Data (DQ0–DQ15)
Read	L	L	H	H	X	X	X	A_{IN}	D_{OUT}
Write	L	H	L	H	X	X	X	A_{IN}	D_{IN}
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	X	X	X	HIGH Z
Output Disable	L	H	H	H	X	X	X	HIGH Z	HIGH Z
Reset	X	X	X	L	X	X	X	X	HIGH Z
Sector Protect (Note 2)	L	H	L	V_{ID}	X	X	X	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}
Sector Unprotect (Note 2)	L	H	L	V_{ID}	X	X	X	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}
Temporary Sector Unprotect	X	X	X	V_{ID}	X	X	X	A_{IN}	HIGH Z
Burst Read Operations									
Load Starting Burst Address	L	X	H	H	↑	L	H	A_{IN}	X
Advance burst to Next address (no data presented on the data bus	L	H	H	H	↑	H	L	X	HIGH Z
Advance burst to Next address (appropriate data presented on the data bus	L	L	H	H	↑	H	L	X	Data Out DQ0-DQ15
Terminate Current burst Read Cycle	H	X	H	H	↑	X	X	X	HIGH Z
Terminate Current burst Read Cycle; Start New Burst Read Cycle	L	X	H	H	↑	L	H	A_{IN}	X
Burst Suspend: (All data is retained internally in the device)	L	H	H	H	X	H	H	X	HIGH Z
Burst Resume: (Same data as Burst suspend)	L	L	H	H	↑	H	H	X	Data Out DQ0–DQ15
Burst Resume: (Incremented data from Burst Suspend)	L	L	H	H	↑	H	L	X	Data Out DQ0–DQ15

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Notes:

1. *Addresses are A18:A0.*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Requirements for Reading Array Data Array in Asynchronous (Non-Burst) Mode

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output pins. The output enable access time is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

The internal state machine is set for reading array data in the upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Reading Array Data in Non-burst Mode” for more information. Refer to the AC Read Operations table for timing specifications and to Figure 15 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Requirements for Reading Array Data in Synchronous (Burst) Mode

The device offers fast 32-word sequential burst reads and is used to support microprocessors that implement an instruction prefetch queue, as well as large data transfers during system configuration.

Three additional pins—Load Burst Address (LBA#), Burst Address Advance (BAA#), and Clock (CLK)—allow interfacing to microprocessors and microcontrollers with minimal glue logic. Burst mode read is a synchronous operation tied to the rising edge of CLK. CE#, OE#, and WE# are asynchronous (relative to CLK).

When the device is in asynchronous mode (after power-up or RESET# pulse), any signals on the CLK, LBA#, and BAA# inputs are ignored. The device operates as a conventional flash device, as described in the previous section.

To enable burst mode operation, the system must issue the Burst Mode Enable command sequence (see Table 4). After the device has entered the burst mode, the system must assert Load Burst Address (LBA#) low for one clock period, which loads the starting address into the device. The first burst data is available after the initial access time (t_{IACC}) from the rising edge of the CLK that loads the burst address. After the initial access, subsequent burst data is available t_{BACC} after each rising edge of CLK.

The device increments the address at each rising edge of the clock cycles while BAA# is asserted low. The 5-bit burst address counter is set to 00000b at the starting address. *When the burst address counter is reaches 11111b*, the device outputs the last word in the burst sequence, and outputs a low on IND#. If the system continues to assert BAA#, on the next CLK the device will output the data for the starting address—the burst address counter will have “wrapped around” to 00000b. For example, if the initial address is xxxx0h, the data order will be 0-1-2-3.....28-29-30-31-0-1...; if the initial address is xxxx2h, the data order will be 2-3-4-5.....28-29-30-31-0-1-2-3...; if the initial address is xxxx8h, the data order will be 8-9-10-11.....30-31-0-1-2-3-4-5-6-7-8-9....; and so on. *Data will be repeated if more than 32 clocks are supplied*, and BAA# remains asserted low.

A burst mode read operation is terminated using one of three methods:

- In the first method, CE# is asserted high. The device in this case remains in burst mode; asserting LBA# low terminates the previous burst read cycle and starts a new burst read cycle with the address that is currently valid.
- In the second method, the Burst Disable command sequence is written to the device. The device halts the burst operation and returns to the asynchronous mode.
- In the third method, RESET# is asserted low. All opertations are immediately terminated, and the device will revert to the asynchronous mode.

Note that writing the reset command will not terminate the burst mode.

Burst Suspend/Burst Resume Operations

The device offers Burst Suspend and Burst Resume operations. When both OE# and BAA# are taken high, the device removes (“suspends”) the data from the outputs (because OE# is high), but “holds” the data internally. The device resumes burst operation when either OE# and/or BAA# is asserted low. Asserting the OE# only causes the device to present the same data that was held during the Burst Suspend operation. As long as BAA# is high, the device will continue to output that word of data. Asserting both OE# and BAA# low resumes the burst operation, and on the next rising edge of CLK, increments the counter and outputs the next word of data.

IND# End of Burst Indicator

The IND# output signal goes low when the device is ouputting the last word of a 32-word burst sequence

(word Da+31). When the starting address was loaded with LBA#, the 5-bit burst address counter was set to 00000b. The counter increments to 11111b on the 32nd word in the burst sequence. If the system continues to assert BAA# low, on the next CLK the device will output the starting address data (Da). The burst address counter will be again set to 00000b, and will have "wrapped around."

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The "Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to "AC Characteristics" for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics table, I_{CC3} and I_{CC4} represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of

t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 17 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size	Address Range
SA0	0	0	0	0	0	0	X	8 Kwords	00000h–01FFFh
SA1	0	0	0	0	0	1	0	4 Kwords	02000h–02FFFh
SA2	0	0	0	0	0	1	1	4 Kwords	03000h–03FFFh
SA3	0	0	0	01, 11		X	X	48 Kwords	04000h–0FFFFh
SA4	0	0	1	X	X	X	X	64 Kwords	10000h–1FFFFh
SA5	0	1	0	X	X	X	X	64 Kwords	20000h–2FFFFh
SA6	0	1	1	X	X	X	X	64 Kwords	30000h–3FFFFh
SA7	1	0	X	X	X	X	X	128 Kwords	40000h–5FFFFh
SA8	1	1	X	X	X	X	X	128 Kwords	60000h–7FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 1. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). Table 1 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 4. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3. Am29BL802C Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A18 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	0001h
Device ID: Am29BL802CB (Bottom Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	0081h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	0001h (protected)
												0000h (unprotected)
Burst Mode Status	L	L	H	X	X	V_{ID}	X	L	X	H	H	0000h (non-burst mode) 0001h (burst mode)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note: *The autoselect codes may also be accessed in-system via command sequences. See Table 4.*

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Sector protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 1 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Details on this method are provided in a supplement, publication number 22143. Contact an AMD representative to request a copy.

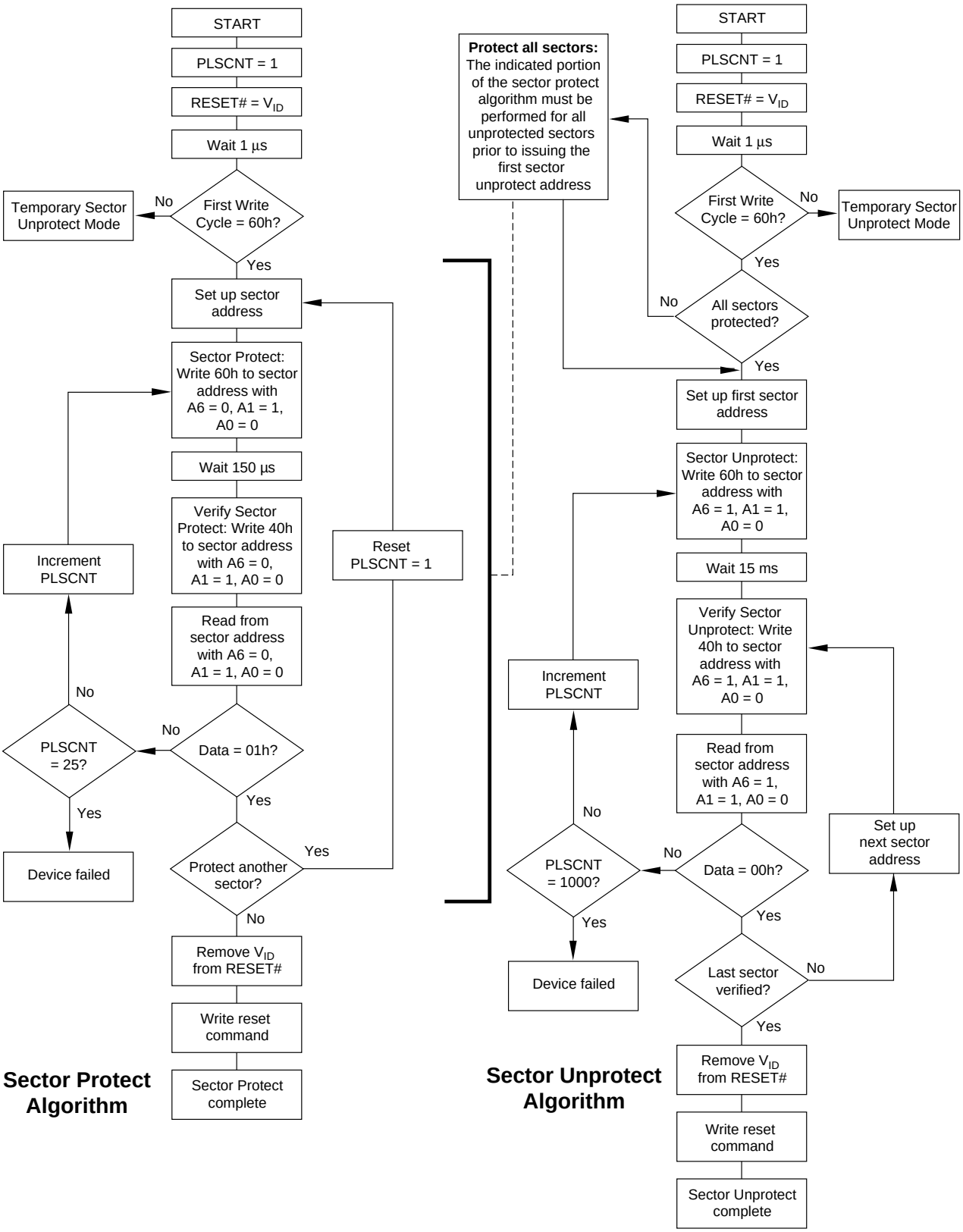
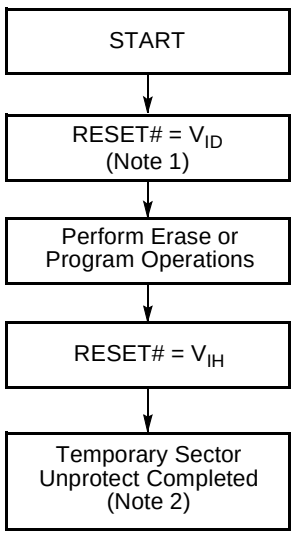


Figure 1. In-system Sector Protect/Unprotect Algorithms

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 2. Temporary Sector Unprotect Operation

HARDWARE DATA PROTECTION

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 4 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 4 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the AC Characteristics section.

Reading Array Data in Non-burst Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See “Erase Suspend/Erase Resume Commands” for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high,

or while in the autoselect mode. See the “Reset Command” section, next.

See also “Requirements for Reading Array Data Array in Asynchronous (Non-Burst) Mode” in the “Key to Switching Waveforms” section for more information. The Read Operations table provides the read parameters, and Figure 15 shows the timing diagram.

Reading Array Data in Burst Mode

The device powers up in the non-burst mode. To read array data in burst mode, the system must write the four-cycle Burst Mode Enable command sequence (see Table 4). The device then enters burst mode. In addition to asserting CE#, OE#, and WE# control signals, burst mode operation requires that the system provide appropriate LBA#, BAA#, and CLK signals. For successful burst mode reads, the following events must occur (refer to Figures 3 and 4 for this discussion):

1. The system asserts LBA# low, indicating to the device that a valid initial burst address is available on the address bus. LBA# must be kept low until at least the next rising edge of the CLK signal, upon which the device loads the initial burst address.
2. The system returns LBA# to a logic high. The device requires that the next rising edge of CLK occur with LBA# high for proper burst mode operation. Typically, the initial number of CLK cycles depends on the clock frequency and the rated speed of the device.
3. After the initial data has been read, the system asserts BAA# low to indicate it is ready to read the remaining burst read cycles. Each successive rising edge of the CLK signal then causes the flash device to increment the burst address and output sequential burst data.
4. When the device outputs the last word of data in the 32-word burst mode read sequence, the device outputs a logic low on the IND# pin. This indicates to the system that the burst mode read sequence is complete.
5. To exit the burst mode, the system must write the four-cycle Burst Mode Disable command sequence. The device will also exit the burst mode if powered down or if RESET# is asserted. The device will not exit the burst mode if the reset command is written.

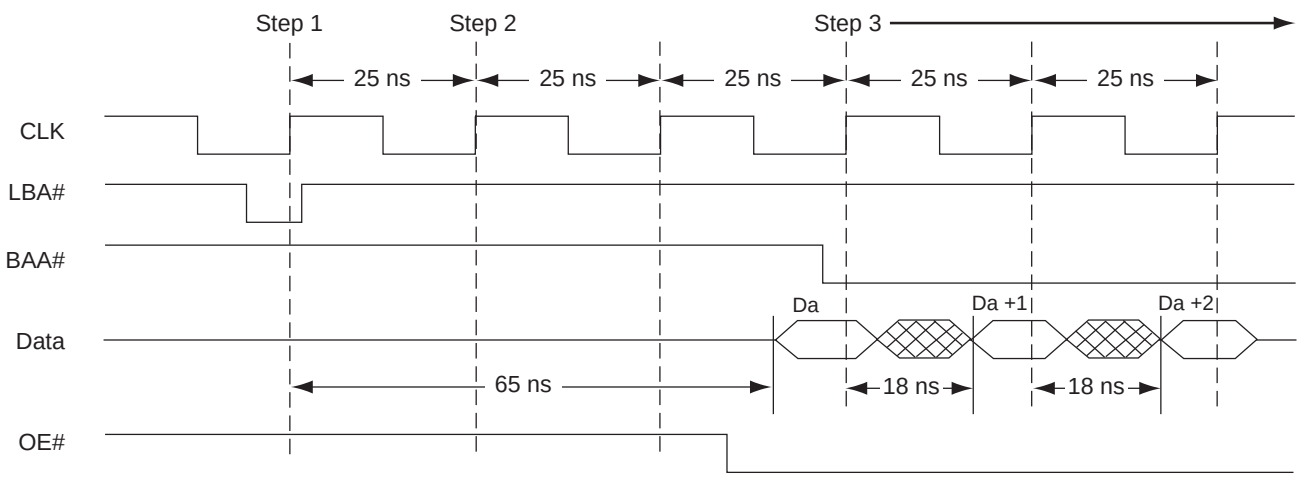


Figure 3. Burst Mode Read with 40 MHz CLK, 65 ns t_{IACC}, 18 ns t_{BACC} Parameters

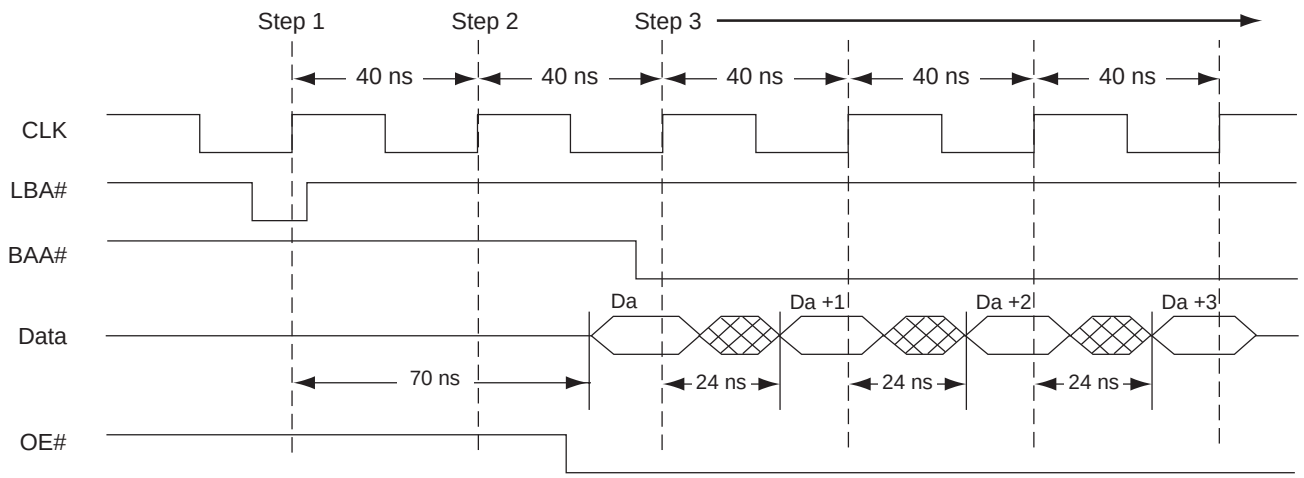


Figure 4. Burst Mode Read with 25 MHz CLK, 70 ns t_{IACC}, 24 ns t_{BACC} Parameters

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

See "AC Characteristics" for parameters, and to Figure 17 for the timing diagram.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 4 shows the address and data requirements. This method is an alternative to that shown in Table 1, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address 00h retrieves the manufacturer code. A read cycle at address 01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode returns 0001h if that sector is protected, or 0000h if it is unprotected. Refer to Table 2 for valid sector addresses. A read cycle at address 03h returns 0000h if the device is in asynchronous mode, or 0001h if in synchronous (burst) mode.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 4 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation.

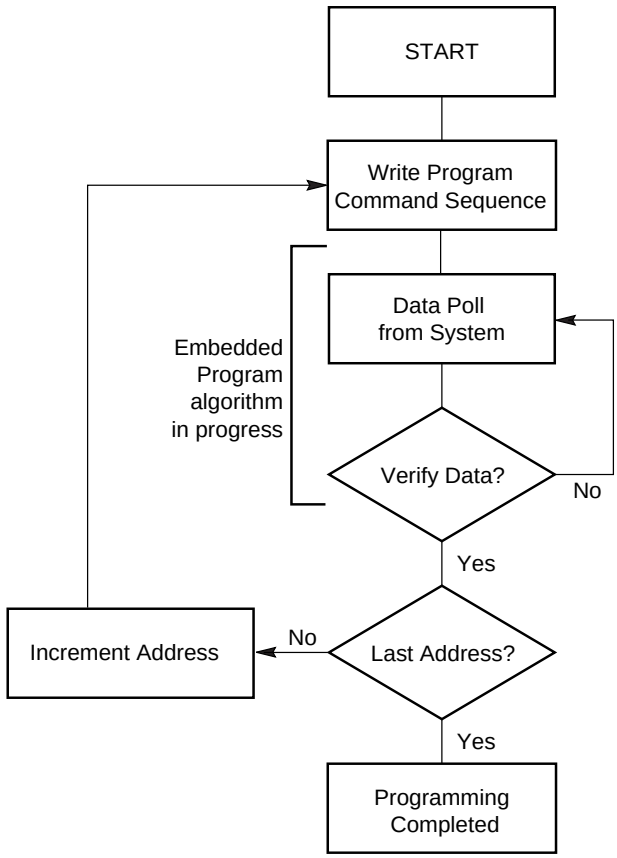
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a “0” back to a “1”.** Attempting to do so may halt the operation and set DQ5 to “1,” or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 4 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don’t care for both cycles. The device then returns to reading array data.

Figure 5 illustrates the algorithm for the program operation. See the Erase/Program Operations table in “AC Characteristics” for parameters, and to Figure 18 for timing diagrams.



Note: *See Table 4 for program command sequence.*

Figure 5. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 4 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 6 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 19 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 4 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to "Write Operation Status" for information on these status bits.)

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to Figure 19 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

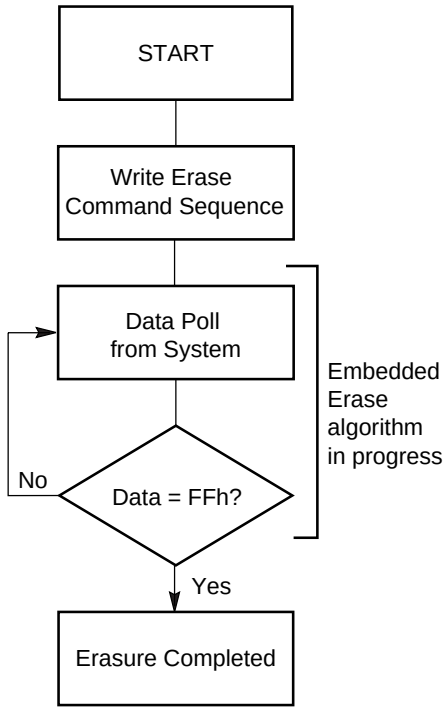
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the

codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Notes:

1. *See Table 4 for erase command sequence.*
2. *See “DQ3: Sector Erase Timer” for more information.*

Figure 6. Erase Operation

Command Definitions

Table 4. Am29BL802C Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID, Bottom Boot Block	4	555	AA	2AA	55	555	90	X01	2281				
	Sector Protect Verify (Note 9)	4	555	AA	2AA	55	555	90	(SA) X02	0000				
										0001				
	Burst Mode Status (Note 10)	4	555	AA	2AA	55	555	90	X03	0000				
										0001				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 11)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 12)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 13)		1	XXX	B0										
Erase Resume (Note 14)		1	XXX	30										
Burst Mode														
Burst Mode Enable		4	555	AA	2AA	55	555	C0	XXX	01				
Burst Mode Disable		4	555	AA	2AA	55	555	C0	XXX	00				

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A18–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
10. *The data is 00h if the device is in asynchronous mode and 01h if in synchronous (burst) mode.*
11. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
12. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
13. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
14. *The Erase Resume command is valid only during the Erase Suspend mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 5 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

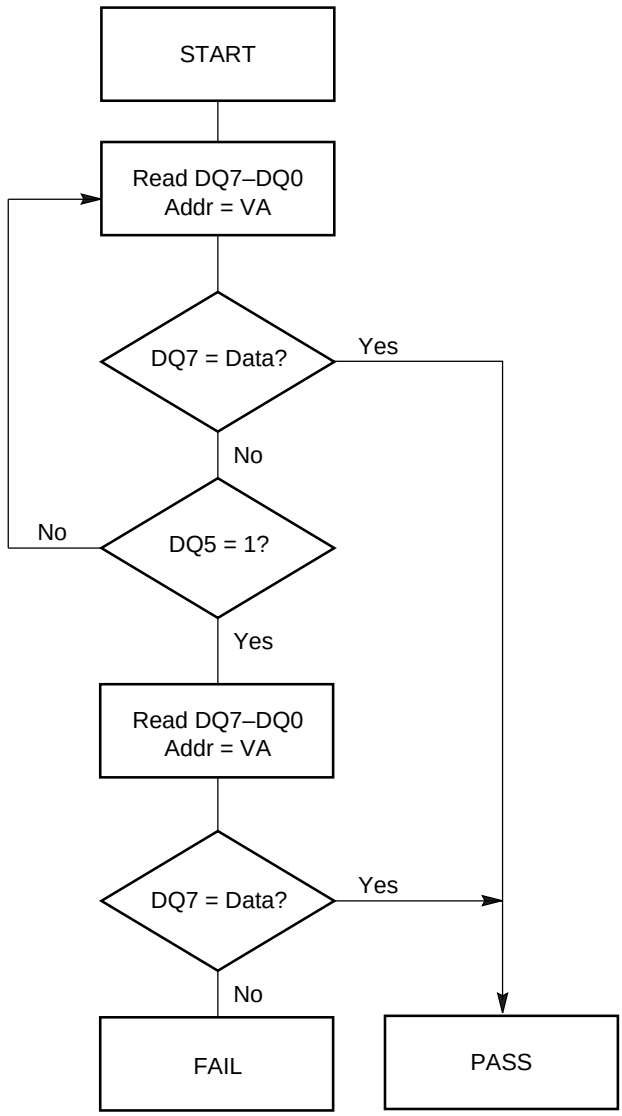
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 20, Data# Polling Timings (During Embedded Algorithms), in the “AC Characteristics” section illustrates this.

Table 5 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 7. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 5 shows the outputs for RY/BY#. Figures 15, 17, 18 and 19 shows RY/BY# for read, reset, program, and erase operations, respectively.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on “DQ7: Data# Polling”).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. Figure 21 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on “DQ2: Toggle Bit II”.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 5 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system

must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

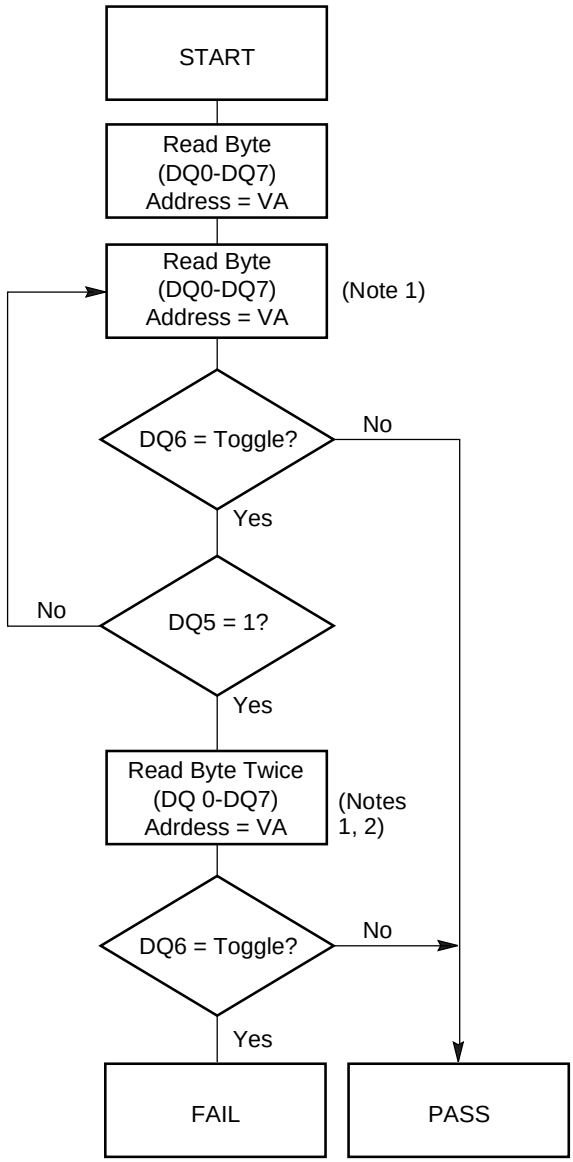
The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.”

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the “Sector Erase Command Sequence” section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 5 shows the outputs for DQ3.



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to “1”. See text.*

Figure 8. Toggle Bit Algorithm

Table 5. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and RESET# (Note 2) . . –0.5 V to +13.0 V

All other pins (Note 1) . . . . . –0.5 V to +5.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input and I/O pins is –0.5 V. During voltage transitions, input and I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions input and I/Os may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A9 and OE# is +13.0 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *3.No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *4.Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

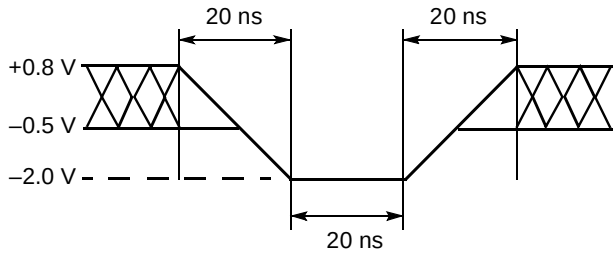


Figure 9. Maximum Negative Overshoot Waveform

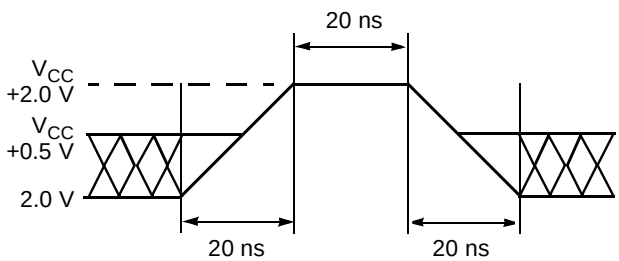


Figure 10. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range. . . . . 3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

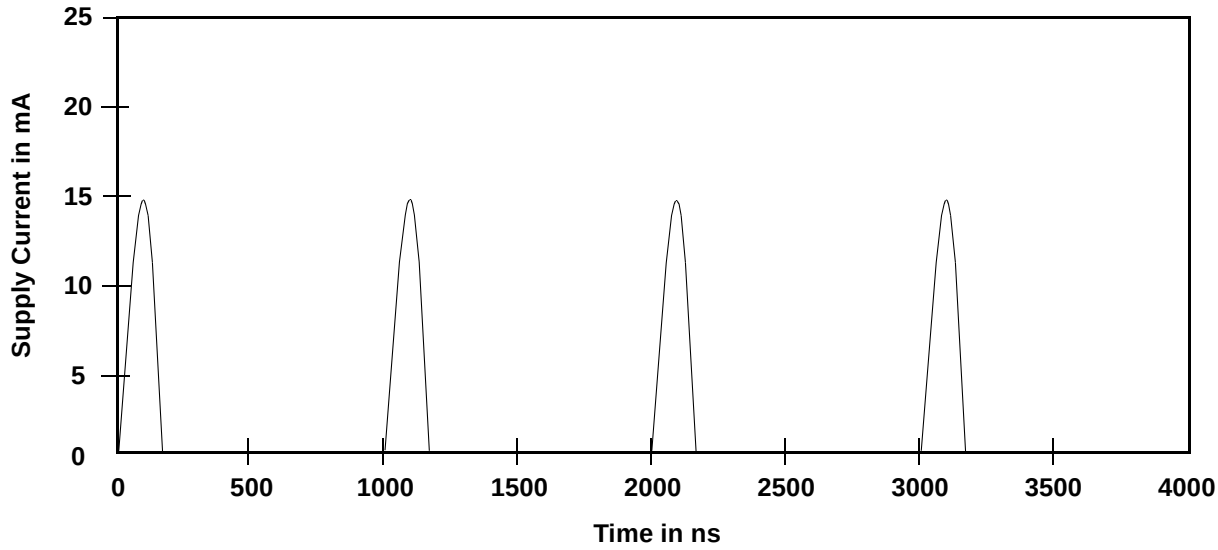
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to 5.5 V, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to 5.5 V, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}, 5 MHz			9	16	mA
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 6)	CE# = V_{IL}, OE# = V_{IH}			20	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC}±0.3 V			3	10	µA
I_{CC4}	V_{CC} Standby Current During Reset (Note 2)	RESET# = V_{SS} ± 0.3 V			3	10	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V	OE# = V_{IH}		3	10	µA
			OE# = V_{IL}		8	20	µA
I_{CC6}	V_{CC} Burst Mode Read Current (Notes 2, 5)	CE# = V_{IL}, OE# = V_{IH}	25 MHz		15	30	mA
			33 MHz		20	35	mA
			40 MHz		25	40	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		5.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 3 µA.*
5. *32-word average.*
6. *Not 100% tested.*

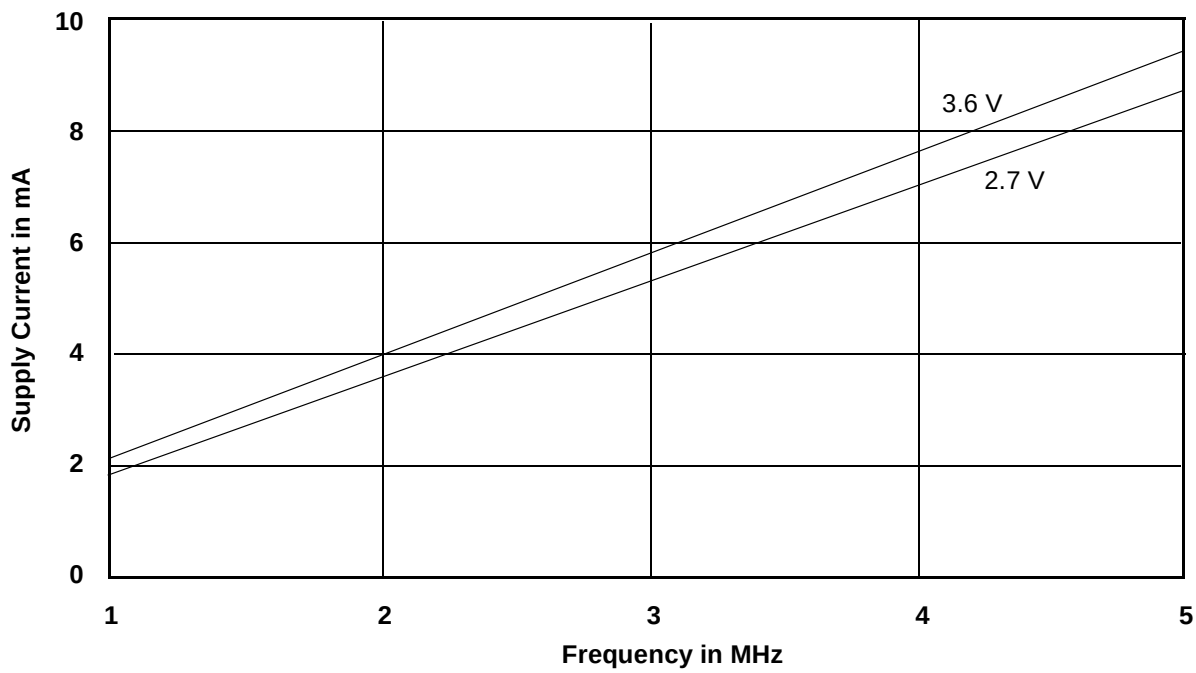
DC CHARACTERISTICS (Continued)

Zero Power Flash



Note: *Addresses are switching at 1 MHz*

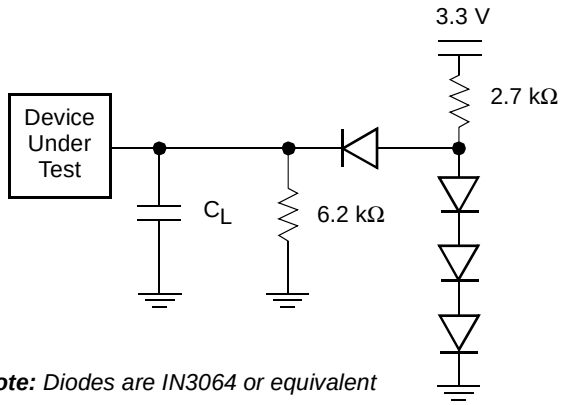
Figure 11. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 12. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 13. Test Setup

Table 6. Test Specifications

Test Condition	65R, 70R	90R, 120R	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

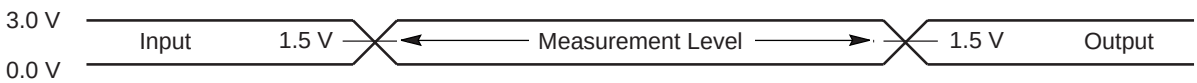


Figure 14. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Options and Temperature Ranges					Unit
						65R		70R	90R	120R	
JEDEC	Std.					I	E	I, E	I, E	I, E	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	65		70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	65		70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	65		70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	17	18	24	26	26	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	17	18	24	26	26	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20		25	30	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0					ns
			Toggle and Data# Polling		Min	10					ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0					ns

Notes:

1. *Not 100% tested.*
2. *See Figure 13 and Table 6 for test specifications*

AC CHARACTERISTICS

Burst Mode Read

Parameter				Speed Options and Temperature Ranges					
				65R		70R	90R	120R	
JEDEC	Std.	Description		I	E	I, E	I, E	I, E	Unit
	t_{IACC}	Initial Access Time LBA# Valid Clock to Output Delay (See Note)	Max	65		70	90	120	ns
	t_{BACC}	Burst Access Time BAA# Valid Clock to Output Delay	Max	17	18	24	26	26	ns
	t_{LBAS}	LBA# Setup Time	Min	6					ns
	t_{LBAH}	LBA# Hold Time	Min	2					ns
	t_{BAAS}	BAA# Setup Time	Min	6					ns
	t_{BAAH}	BAA# Hold Time	Min	2					ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Max	4					ns
	t_{ACS}	Address Setup Time to CLK (See Note)	Min	6					ns
	t_{ACH}	Address Hold Time from CLK (See Note)	Min	2					ns
	t_{OE}	Output Enable to Output Valid	Max	17	18	24	26	26	ns
	t_{OEZ}	Output Enable to Output High Z	Max	20		25	30	30	ns
	t_{CEZ}	Chip Enable to Output High Z	Min	20		25	30	30	ns
	t_{CES}	CE# Setup Time to Clock	Min	6					ns

Note: *Initial valid data will be output after second clock rising edge of LBA# assertion.*

AC CHARACTERISTICS

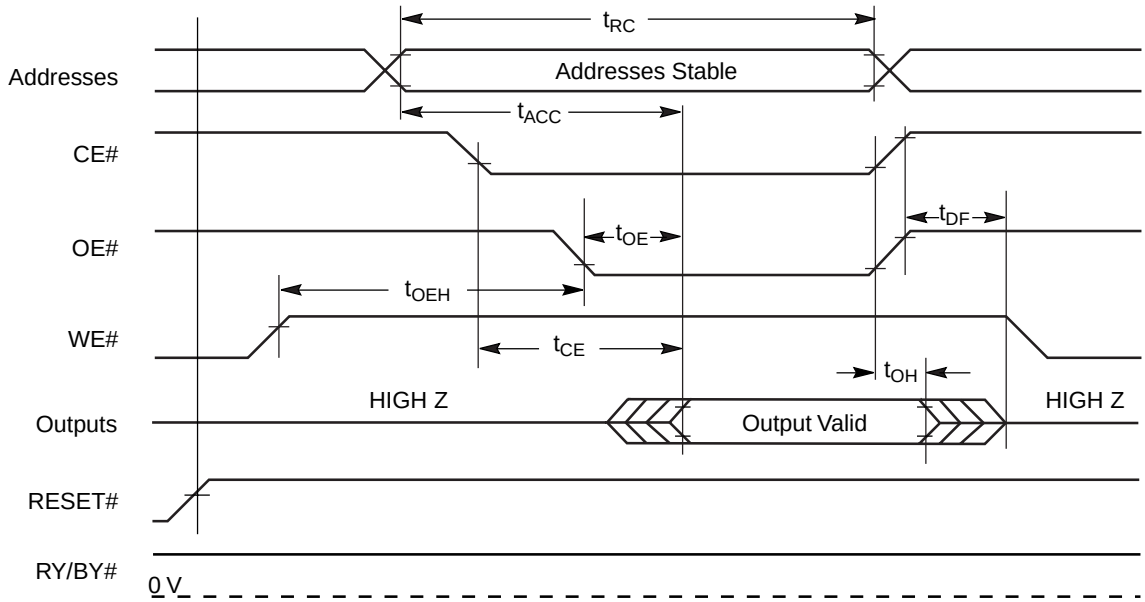


Figure 15. Conventional Read Operations Timings

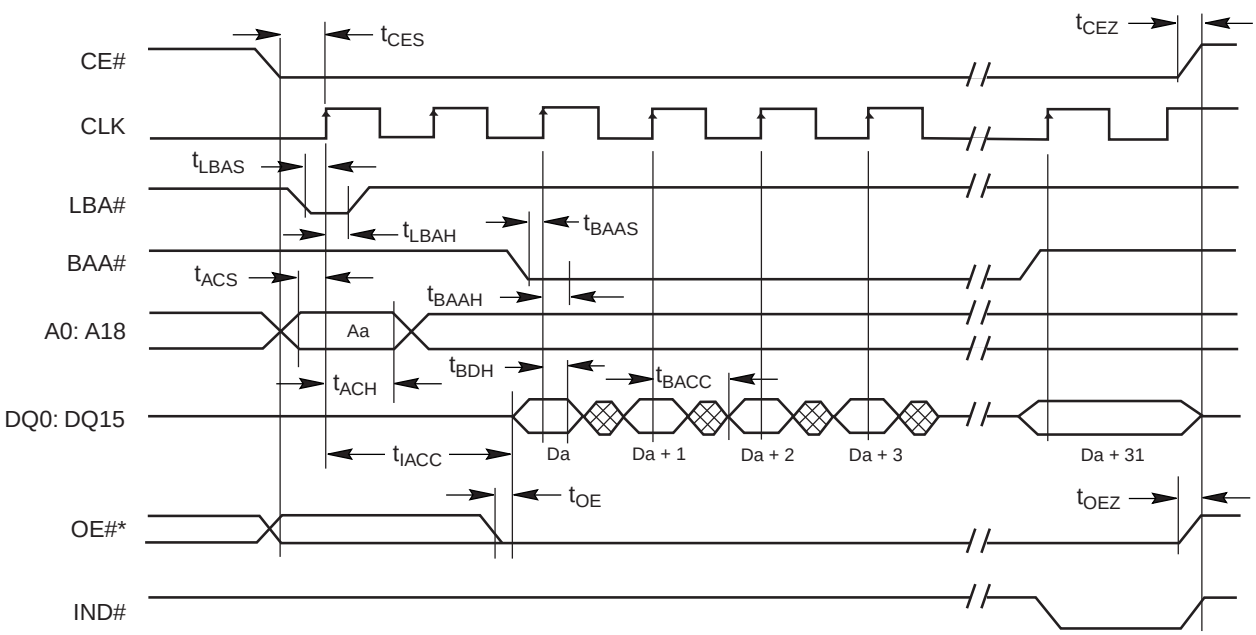


Figure 16. Burst Mode Read

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

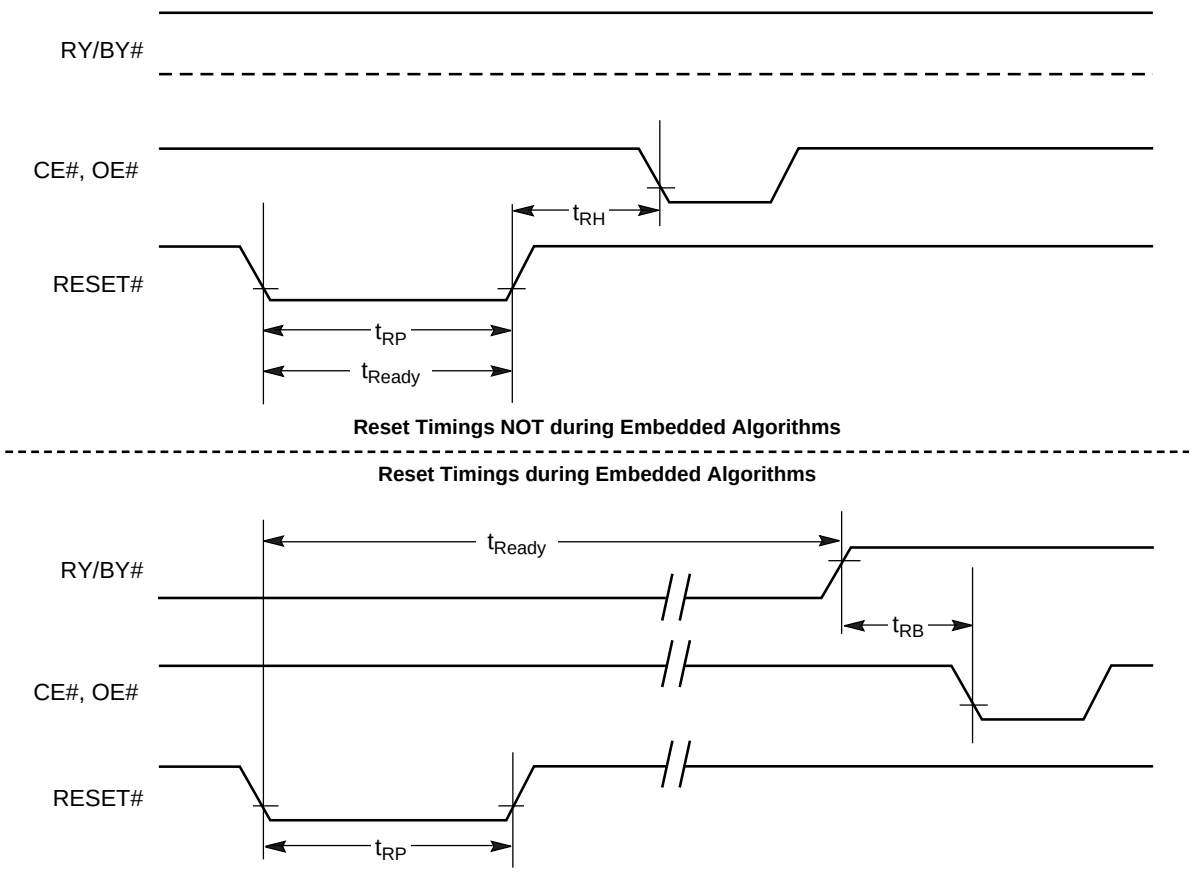


Figure 17. RESET# Timings

AC CHARACTERISTICS

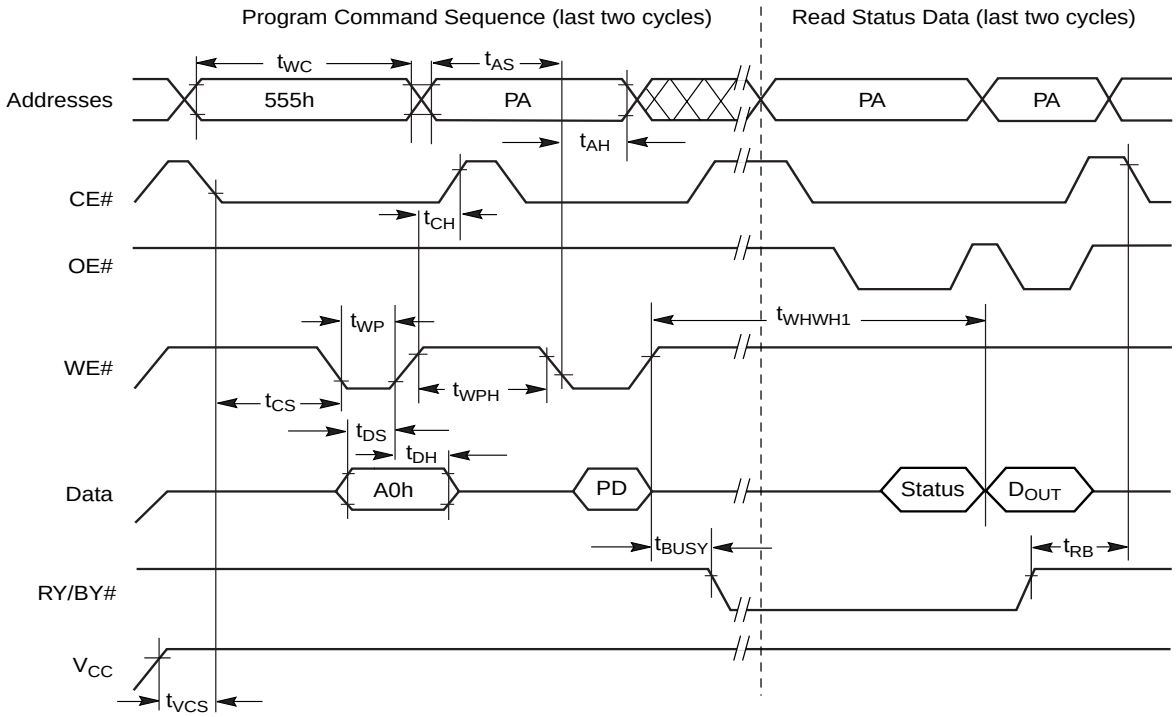
Erase/Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			65R	70R	90R	120R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	65	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	3				sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50				µs
	t_{RB}	Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

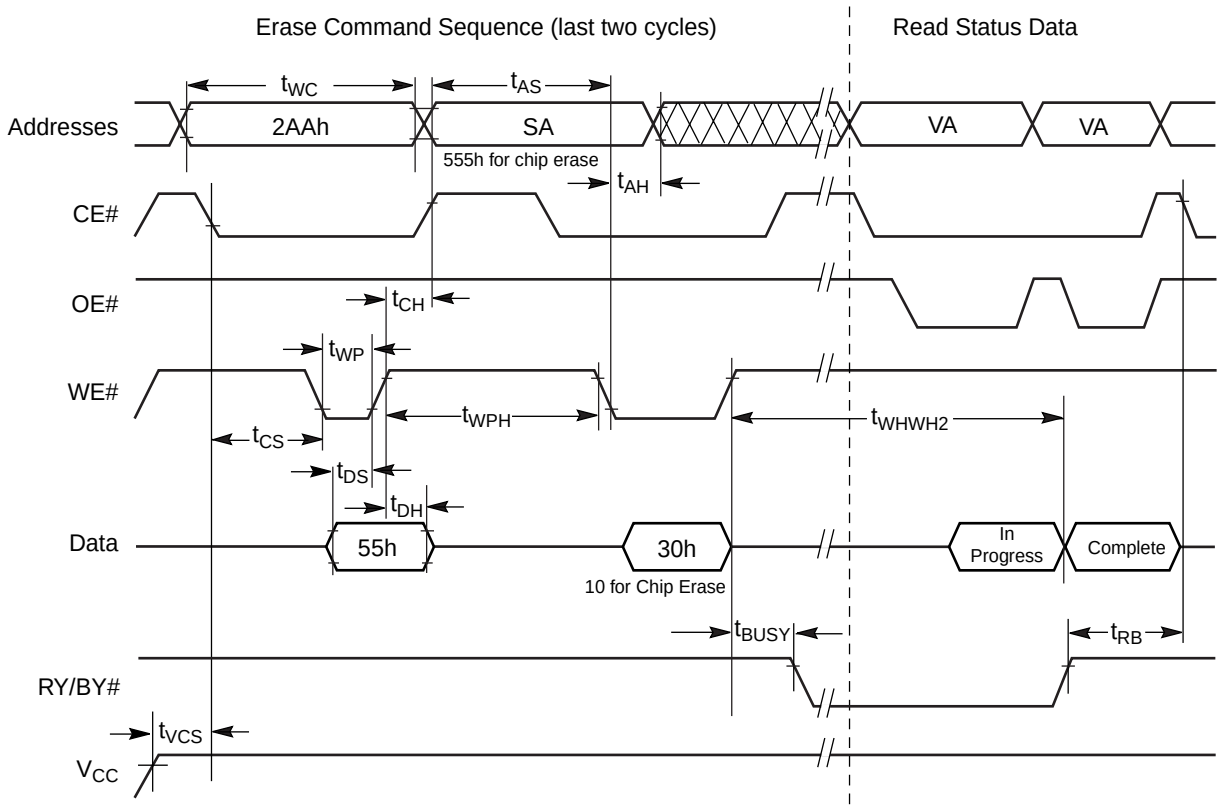
AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 18. Program Operation Timings

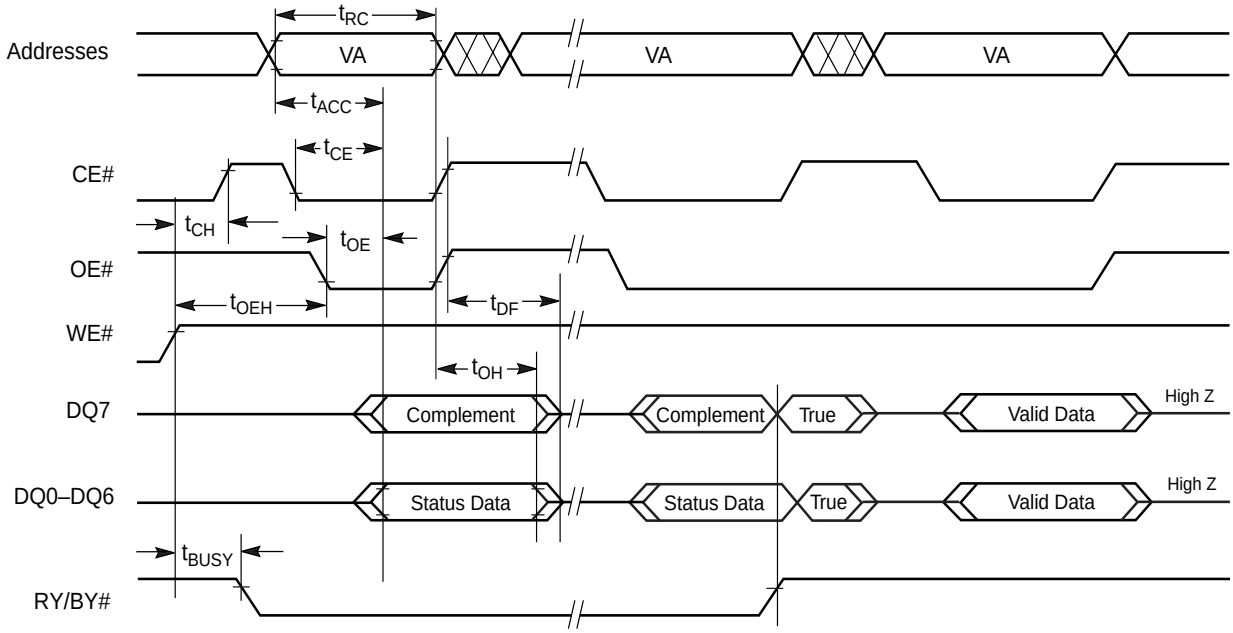
AC CHARACTERISTICS



Note: *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*

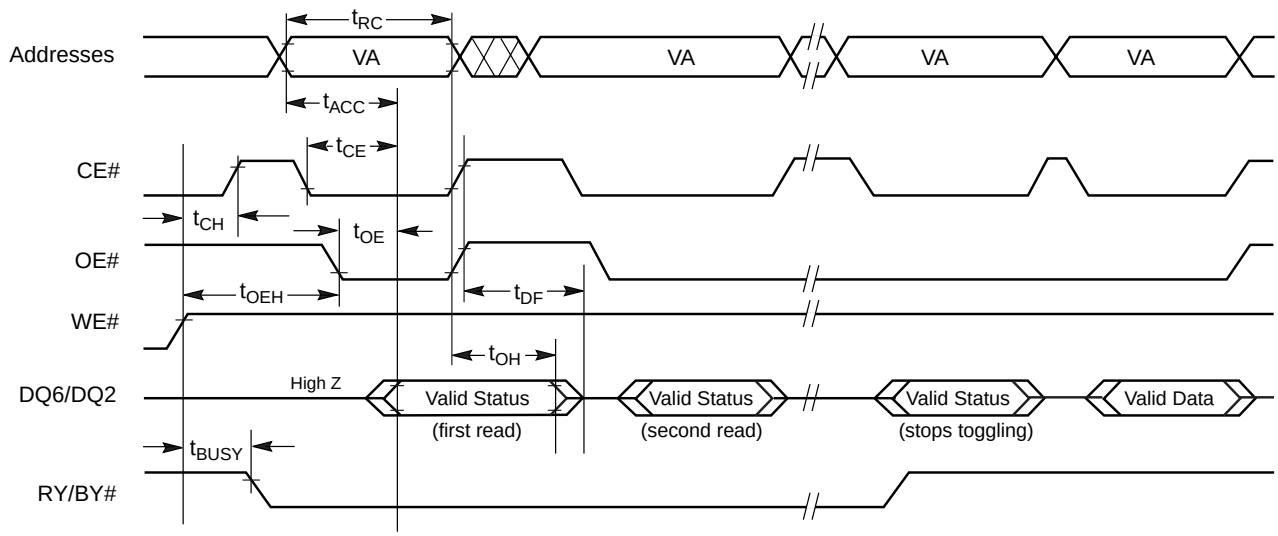
Figure 19. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

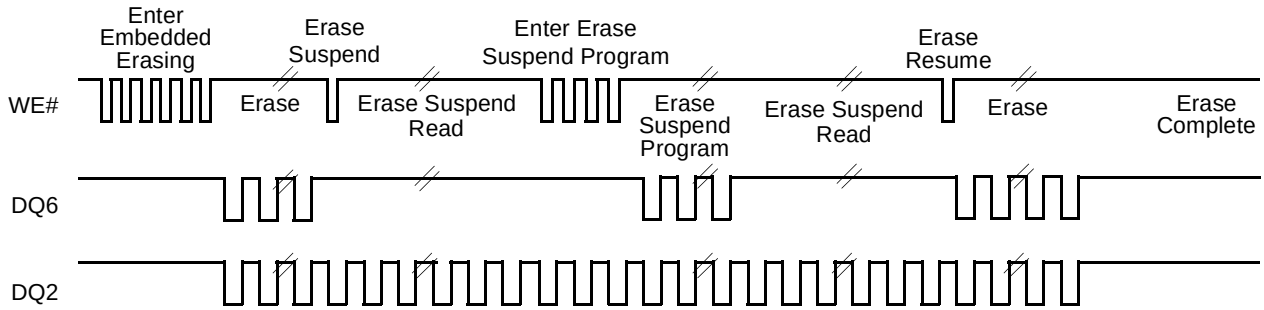
Figure 20. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 22. DQ2 vs. DQ6 for Erase and Erase Suspend Operations

Temporary Sector Unprotect

Parameter					
JEDEC	**Std.**	**Description**		**All Speed Options**	**Unit**
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

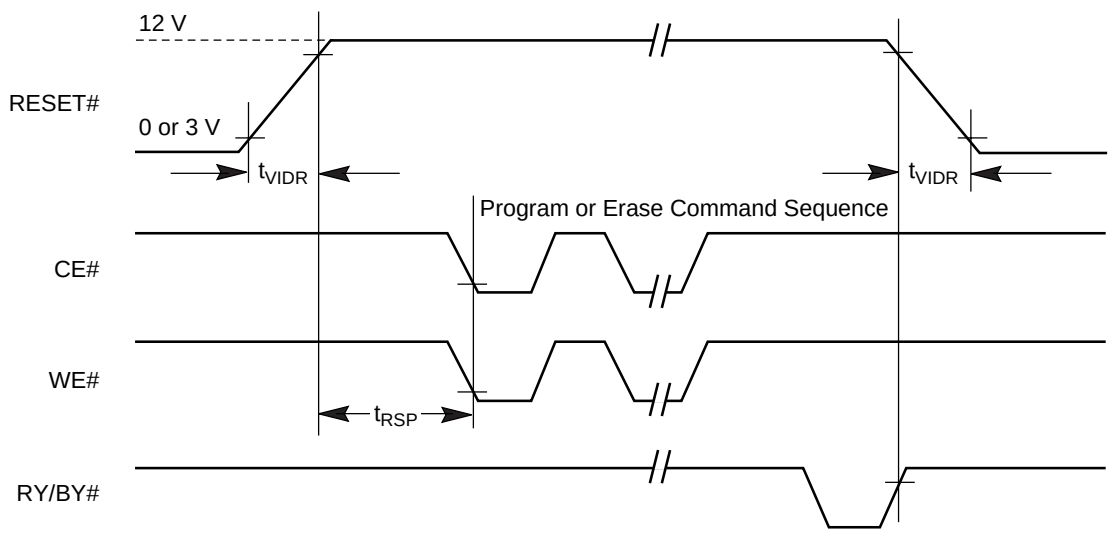
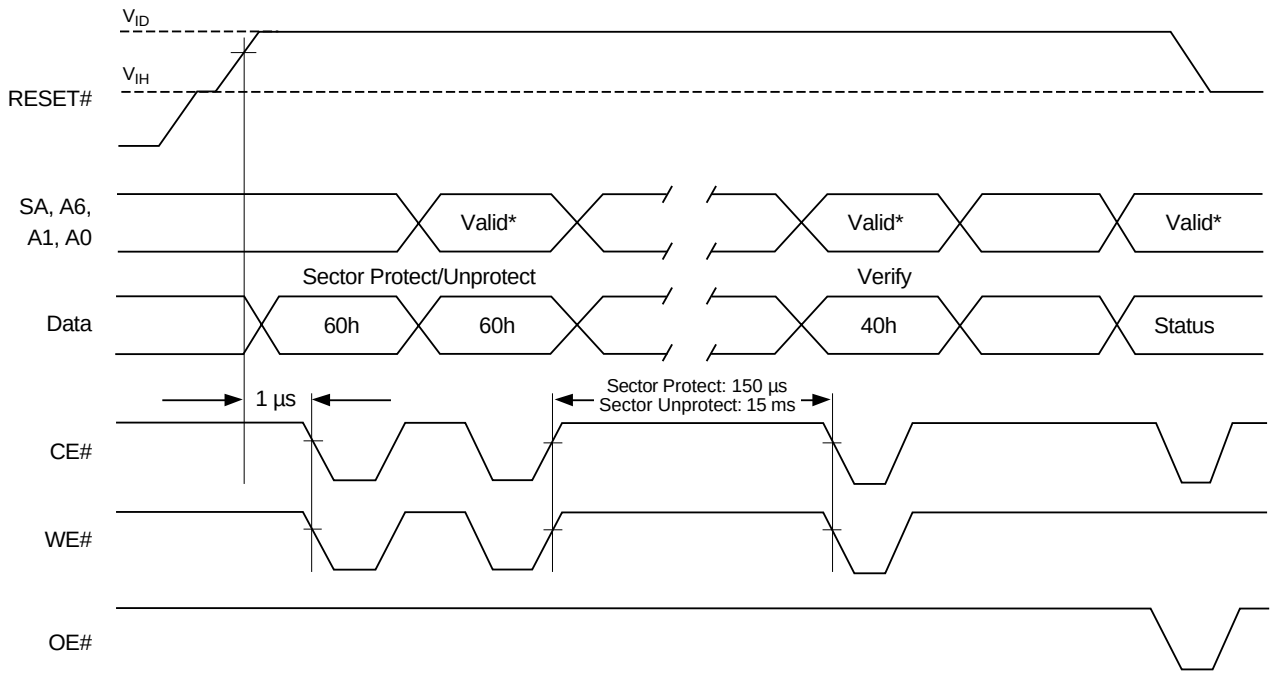


Figure 23. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



Note: *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 24. Sector Protect/Unprotect Timing Diagram

AC CHARACTERISTICS

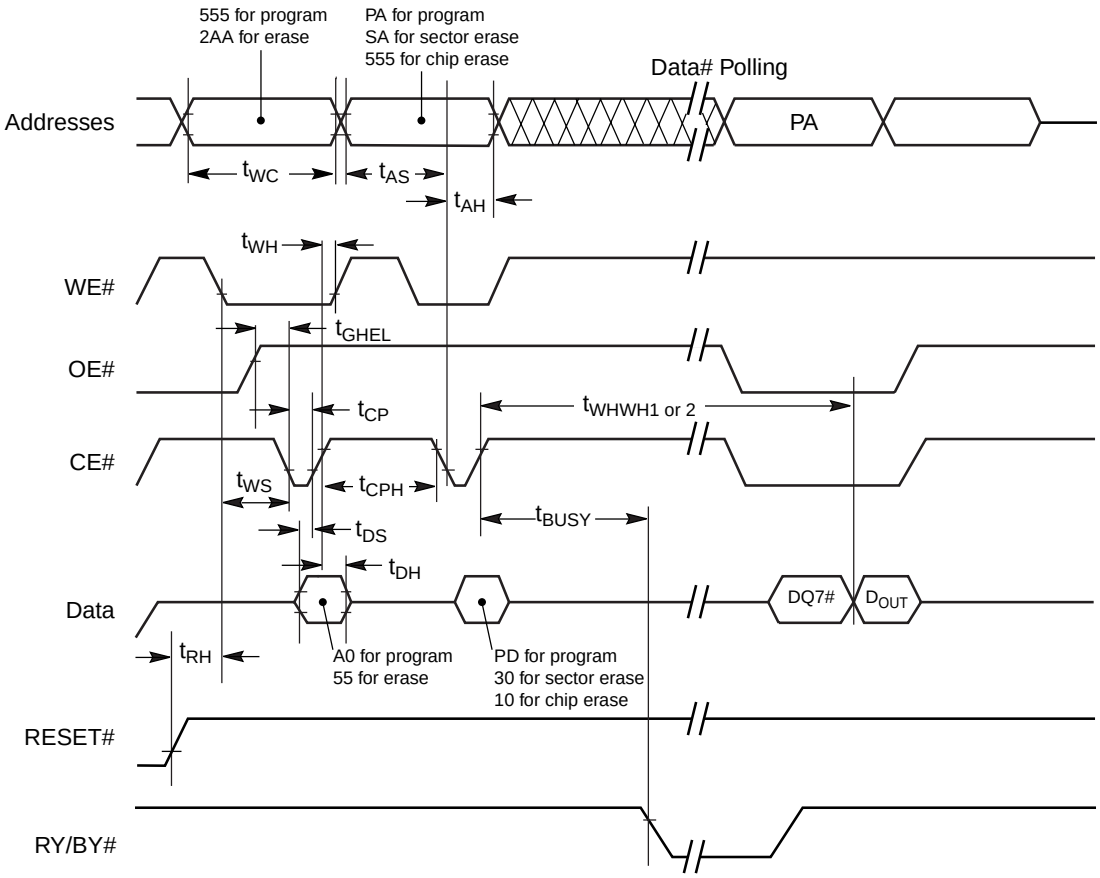
Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			65R	70R	90R	120R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	65	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30				ns
t_{WHWSH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	3				sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*

Figure 25. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	3	60	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	22		s	
Word Programming Time	9	360	µs	Excludes system level overhead (Note 5)
Chip Programming Time (Note 3)	9	27	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 4 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

SSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

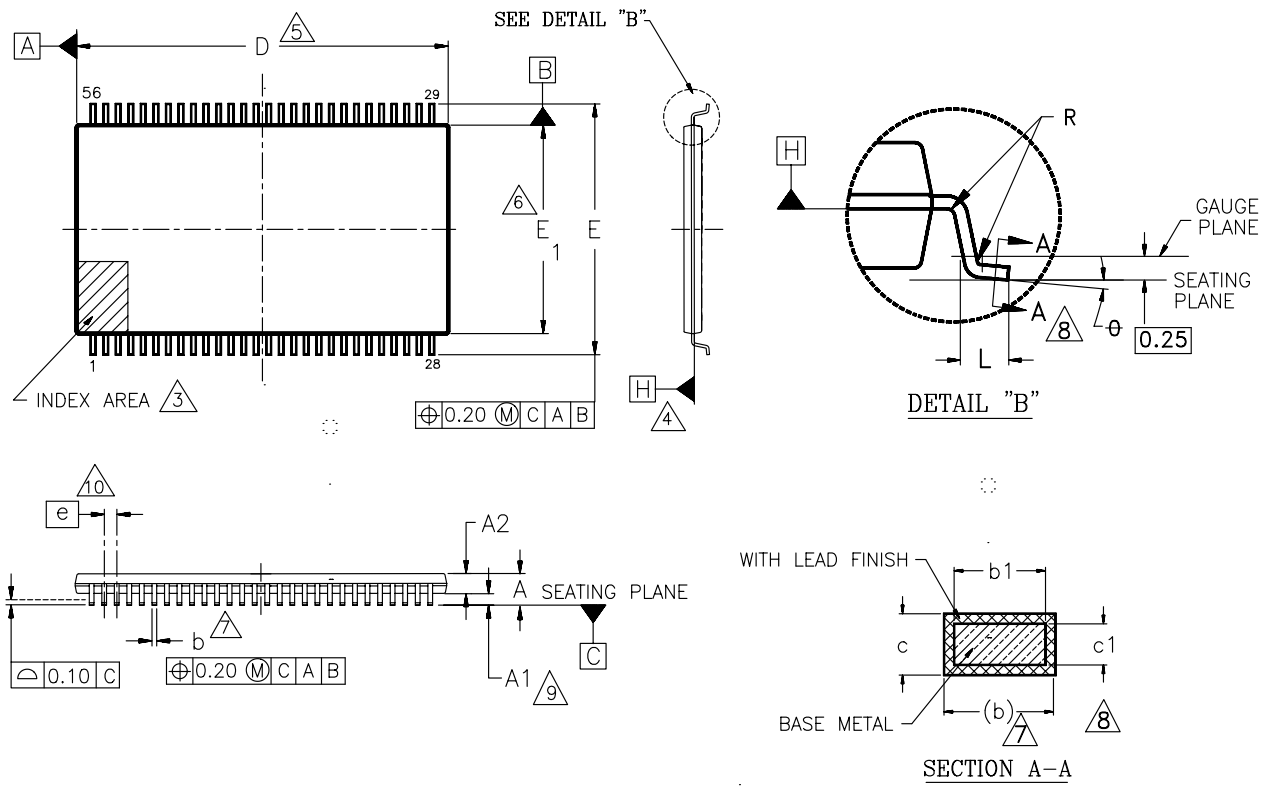
DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

SSO056—56-Pin Shrink Small Outline Package



Dwg rev AB; 10/99

PACKAGE	SSO 056		
JEDEC	MO–180 (A) BA		
SYMBOL	MIN	NOM	MAX
A	—	—	2.00
A1	0.45	—	0.65
A2	1.15	1.25	1.35
b	* 0.25	—	0.45
b1	0.30	0.35	0.40
c	0.10	—	0.21
c1	0.10	0.15	0.18
D	23.40	23.70	24.00
E	15.70	16.00	16.30
E1	13.10	13.30	13.50
e	0.80 BSC		
L	0.60	0.80	1.00
R	0.09	—	—
θ	0°	4°	8°

* —DEVIATES FROM JEDEC (0.30)

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm).
2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
4. DATUMS A AND B AND DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.
6. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07 mm AT LEAST MATERIAL CONDITION.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIPS.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.
10. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
11. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

REVISION SUMMARY

Revision A (June 1, 1999)

Initial release.

Revision A+1 (June 25, 1999)

General Description

Corrected the device density in the first paragraph.

Command Definitions

Reading Array Data in Burst Mode: Added reference to Figure 3 in the first paragraph.

Revision B (November 29, 1999)

Global

All speed options are now offered only at the regulated voltage range of 3.0 to 3.6 V. The 90 and 120 speed options now have a t_{OE} of 26 ns at the industrial temperature range. The 70 ns speed option is now available at the extended temperature range.

AC Characteristics

In Figures 17 and 18, deleted t_{GHWL}; modified OE# waveform.

Physical Dimensions

Updated drawing of SSOP to new version.

Revision C (June 20, 2000)

Global

The “advance information” data sheet designation has been changed to “preliminary.” Only minor parameter changes, if any, may occur. Speed, package, and temperature range combinations may also change in future data sheet revisions.

Distinctive Characteristics

Changed burst access time specification for the 65R speed option in the industrial temperature range from 19 to 18 ns.

Product Selector Guide

Replaced t_{OE} with t_{BACC} to more clearly distinguish burst mode access from asynchronous access times. Note however, that in burst mode, t_{OE} and t_{BACC} specifications are identical. Changed t_{BACC} for the 65R speed option in the industrial temperature range from 19 to 18 ns.

Ordering Information

Burn-in processing is no longer available.

Requirements for Reading Array Data Array in Asynchronous (Non-Burst) Mode

Clarified the description of how to terminate a burst mode read operation.

Burst Mode Read with 40 MHz CLK figure

Changed t_{BACC} for the 65R speed option in the industrial temperature range from 19 to 18 ns.

Read Operations table

Changed t_{OE} and t_{DF} for the 65R speed option in the industrial temperature range from 19 to 18 ns.

Burst Mode Read table

Changed t_{OE} and t_{BACC} for the 65R speed option in the industrial temperature range from 19 to 18 ns.

Burst Mode Read figure

Corrected BAA# waveform to return high before the final clock cycle shown.

Erase and Programming Performance table, Erase and Program Operations table, Alternate CE# Controlled Erase and Program Operations table

Resolved differences in typical sector erase times. The typical sector erase time for all sectors is 3 sec.

Revision C+1 (November 16, 2000)

Global

Deleted Preliminary status from document. Added table of contents. Added Figure 1, In-system Sector Protect/Unprotect Algorithms figure to document (was missing from previous revisions).

Revision C+2 (July 22, 2002)

Pin Description, IND# End of Burst Indicator

Clarified description of IND# function.

Table 1, Device Bus Operations

In burst read operations section, changed BAA# to “H” for “Load starting Burst Address” and Terminate Current Burst Read Cycle; Start New Burst Read Cycle.”

Requirements for Reading Array Data in Synchronous (Burst) Mode

Modified section to clarify the description of the IND# and burst read functions.

Burst Sequence Table

Deleted table.

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