Application Note

CS4235 REVIEW CHECKLIST

By Mark Shipley and Brian Straup

Overview

This application note is prepared as a basic checklist for the CS4235 Multimedia codec. A general pin-for-pin checklist of the CS4235 is in the *Digital Power & Ground Pins* section, and a support circuitry and PC board layout checklist is in the *Board Layout checklist* section. The checklist is intended to be used as a guide to the design engineer that may not be familiar with multimedia audio codecs and the correct implementation of the CS4235. Three areas are highlighted: avoiding simple connectivity errors, suggestions for good audio performance, and identifying conditions that may lead to component damage or unreliable circuit operation. This checklist addresses the multi-function pins on the CS4235 and allows variations in the design for add-in cards as well as motherboard applications. Please refer to the CRD4235-8 and CRD4235-6 reference designs for additional information.

Digital Power & Ground Pins

- Pin 45 VD1 (ISA Digital Supply Voltage)

  Digital supply for the codec's ISA parallel data bus drivers. This pin should be decoupled with a 0.1 µF capacitor and connected to the +5 Volt plane or ISA bus pins D16, B29 and B3.

- Pin 46 DGND1 (ISA Digital Ground)

  Digital ground reference for the codec bus drivers that interface to the ISA parallel data bus. The DGND1 pin is isolated from the other digital grounds. This pin should be connected to either the motherboard digital ground plane or the ISA bus ground pins B1, B31, D18, and B10. It is very important the analog plane and digital plane be tied together at some point to establish a common voltage between analog and digital sections of the audio codec. Without a common tie point, severe damage to the CS4235 audio codec may occur. In most layouts, the best tie point is close to a chassis ground location, at the analog voltage regulator, or at the power supply connector entry point. A wide copper connection permanently etched into the printed circuit board provides a good connection between both grounds at all frequencies.

- Pins 17, 65, 98 VDF1, VDF2, VDF3 (Digital Filtered Supply Voltage)

  +5 Volt digital supply pins for the internal digital section of the codec (except for the parallel data bus). These pins should be filtered from the +5 Volt digital power supply using a ferrite bead and capacitors.

- Pins 18, 66, 97, 53 SGND<1:4 >(Digital GND)

  Ground reference pins for the internal digital portion of the codec. These pins should be connected to either the motherboard digital ground plane or ISA bus ground pins B1, B31, D18, and B10. It is very important the analog plane and digital plane be tied together at some point to establish a common voltage between analog and digital sections of the audio codec. Without a common tie point, severe damage to the CS4235 audio codec may occur. In most lay-

Cirrus Logic, Inc.
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

outs, the best tie point is close to a chassis ground location, at the analog voltage regulator, or at the power supply connector entry point. A wide copper connection permanently etched into the printed circuit board provides a good connection between both grounds at all frequencies.

- Pin 71 TEST (Input)

  The TEST pin must be tied to digital ground for proper operation.

Analog Power & Ground Pins

- Pin 81 VA (Analog Supply Voltage)

  +5 Volt supply to the analog section of the codec. This pin is usually connected to the output of a +5 Volt linear 78M05 regulator and decoupled with a 0.1 µF capacitor.

- Pin 80 AGND (Analog Ground)

  Ground reference pin for the analog section of the codec. This pin should be separated from other codec grounds and connected to the analog ground plane. It is very important the analog plane and digital plane be tied together at some point to establish a common voltage between analog and digital sections of the audio codec. Without a common tie point, severe damage to the CS4235 audio codec may occur. In most layouts, the best tie point is close to a chassis ground location, or located at the power supply connector entry point. A wide copper connection permanently etched into the printed circuit board provides a good connection between both grounds at all frequencies.

CDROM Interface Pins

- If the design does not have a CDROM interface or another device attached to the CDROM interface pins, this section is not applicable. Skip to section *ISA Bus Interface Pins*.

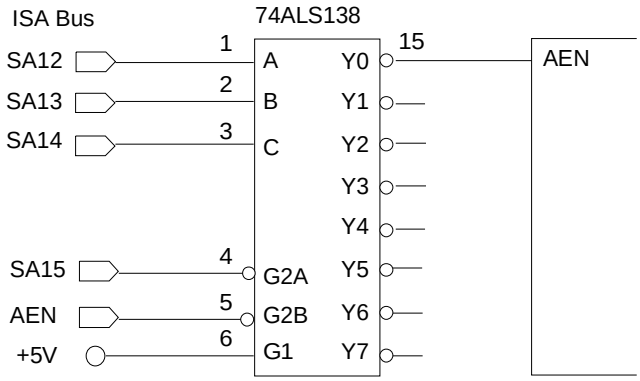


Figure 1. CDROM Address Decode

- Pin 39 AEN (Input)

  The CDROM interface is enabled (in lieu of the upper four ISA address pins) when the CDROM enable (pin 3) of the codec is pulled low with a 10 kΩ resistor. Since Windows 95 (OSR2) requires a 16-bit address decode to eliminate aliasing, the upper addresses must be decoded with external logic gated with AEN. A typical circuit is shown in Figure 1.

- Pin 3 MCLK (CDROM enable) (Output)

  When this pin is pulled low with a 10 kΩ resistor to SGND, it enables the CDROM interface (in lieu of the upper four ISA address pins).

- Pin 5 SDOUT (Alternate CDROM Chip Select Enable) (Output)

  When this pin is pulled low with a 10 kΩ resistor to SGND, it enables the alternate CDROM chip select $\overline{\text{ACDCS}}$. Hardware volume control (VCEN) must be off (0) for the $\overline{\text{ACDCS}}$ pin to function properly. Loading on SDOUT must be limited to CMOS inputs.

- Pin 94 $\overline{\text{CDCS}}$ (Output)

  The CDROM chip select pin is normally connected to pin 37 of the 20x2 IDE header connector. This pin goes low whenever an address is decoded that matches the value programmed

into the CDROM base address register. This pin is capable of driving 4 mA.

- Pin 92 CDINT (Input)

  The CDROM Interrupt pin is used to input an interrupt signal from the CDROM interface and connects to pin 31 of the 20x2 IDE header connector. The polarity of this input can be programmed through CTRLbase+1 register, bit ICH, or the Hardware Configuration data. The default is active high.

- Pin 16 $\overline{\text{ACDCS}}$ (Output)

  The Alternate CDROM chip select is normally connected to pin 38 of the 20x2 IDE header connector. This pin goes low whenever an address is decoded that matches the value programmed into the alternate CDROM base address register. This pin is capable of driving 4 mA. Hardware volume control (VCEN) must be off (0) for the $\overline{\text{ACDCS}}$ pin to function properly.

- Pin 91 CDRQ (Input)

  The CDROM DMA Request pin is usually not used and is tied to +5 Volts through a 6.8 kΩ pull-up resistor. However, this pin can be used to input the DMA request signal from the CDROM interface and can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus DRQ line.

- Pin 93 $\overline{\text{CDACK}}$ (Output)

  Normally $\overline{\text{CDACK}}$ is not connected to any circuitry. The $\overline{\text{CDACK}}$ pin can be used to output the ISA bus-generated DMA acknowledge signal to the CDROM interface. This pin is capable of driving 4 mA.

ISA Bus Interface Pins

- Pins 25-36 SA<0:11> System Address Bus (Inputs)

  These lower ISA System Address Bus interface signals are decoded during I/O cycles to determine access to the various functional blocks within the codec as defined by the configuration data written during a Plug and Play configuration. These pins connect to ISA pins A31-A20.

- Pins 94-91 SA<12:15> Upper System Address Bus (Inputs)

  These signals are multi-function pins that default to the upper address bits SA12 through SA15. They connect to ISA bus pins A19-A16. Using these pins as upper address bits forces the codec to only accept valid address decodes when A12-A15 = 0. Windows 95 (OSR2) requires 16 bit addressing to eliminate address decode aliasing, so these signals must be decoded either directly or with external logic gated with AEN (see Figure 1 in section *CDROM Interface Pin*).

- Pins 41-50 SD<0:7> (Bi-directional)

  These System Data Bus ISA bus signals are used to transfer data to and from the codec and feature 24 mA drive capabilities. They connect to ISA bus pins A9-A2.

- Pin 37 $\overline{\text{IOR}}$ (Input)

  Read Command Strobe is an active low signal that defines a read cycle to the CS4235 codec. Connect this signal to the ISA bus pin B14.

- Pin 38 $\overline{\text{IOW}}$ (Input)

  Write Command Strobe is an active low signal that defines a write cycle to the CS4235 codec. Connect this signal to ISA bus pin B13.

- Pin 90 RESDRV (Input)

  RESDRV is an active high input signal and should be connected to ISA bus pin B2. In applications where it is desirable to disable the on-board audio subsystem, an external active high disable signal may be gated with the RESDRV signal from the ISA bus.

- Pin 39 AEN Address Enable (Input)

  The Address Enable signal indicates whether the current bus cycle is an I/O cycle or a DMA cycle, and connects to ISA bus pin A11. This signal is low during an I/O cycle and high during a DMA cycle.

- Pin 40 IOCHRDY (Open Drain Output)

  The audio codec forces IOCHRDY low to extend the current bus cycle. This pin should be connected to the ISA bus connector pin A10.

- Pins 55, 51, 52 DRQ<A,B,C> (Outputs)

  These active high outputs are used to request a DMA transfer. The default connections are shown in Table 1, but can be changed by modifying the Hardware Resource data in the E^2PROM.

CS4235		ISA BUS
DRQA (pin 55)	=	DRQ0 (ISA pin D9)
DRQB (pin 51)	=	DRQ1 (ISA pin B18)
DRQC (pin 52)	=	DRQ3 (ISA pin B16)

Table 1. DMA Requests

- Pins 58, 56, 57 $\overline{\text{DACK}}$<A,B,C> (Inputs)

The default connections for the DMA Acknowledge signals on the ISA bus are shown in Table 2. The defaults can be changed by modifying the Hardware Resource data and the E^2PROM.

CS4235		ISA BUS
DACKA (pin 58)	=	DACK0 (ISA pin D8)
DACKB (pin 56)	=	DACK1 (ISA pin B17)
DACKC (pin 57)	=	DACK3 (ISA pin B15)

Table 2. DMA Acknowledge

- Pins 24-19, 54 IRQ <A:G> (Outputs)

  The Interrupt Requests are individually enabled by configuration data that is generated during a Plug and Play configuration sequence. The default connections to the ISA bus are shown in Table 3. IRQG is new to the CS4235 and defaults to unconnected for compatibility reasons. For new designs, IRQG is typically connected to IRQ10. The defaults can be changed by modifying the Hardware Configuration data loaded from the E^2PROM.

CS4235		ISA BUS
IRQA (pin 24)	=	INT5 (ISA pin B23)
IRQB (pin 23)	=	INT7 (ISA pin B21)
IRQC (pin 22)	=	INT9 (ISA pin B4)
IRQD (pin 21)	=	INT11 (ISA pin D4)
IRQE (pin 20)	=	INT12 (ISA pin D5)
IRQF (pin 19)	=	INT15 (ISA pin D6)
IRQG (pin 54)	=	INT10 (ISA pin D3)

Table 3. Interrupt Requests

E^2PROM Interface Pins

The CS4235 has only 768 bytes of RAM, therefore the size of the E^2PROM can be reduced to a 24C08. An E^2PROM is required on add-in cards to pass WHQL testing, since they require unique vendor IDs for certification. A 24C01 E^2PROM can be used to provide the unique OEM ID required by Microsoft WHQL, but no firmware updates or resource changes will fit into this smaller device. The 24C08 E^2PROM will allow full resource changes and firmware updates along with the OEM ID, and is the recommended device for designs requiring an E^2PROM. Please contact your Cirrus Logic representative for more information on the option of going with the 24C01 E^2PROM. Motherboard designs may incorporate resource and patch code data via a BIOS host load.

- Pin 8 SDA (Bi-directional)

  The SDA data pin is open-drain, and must have an external 3.3 kΩ to 4.7 kΩ pull-up resistor.

SDA is used in conjunction with SCL to access an external serial E^2PROM. When an external E^2PROM is used, the SDA pin should be connected to the pin 5 of the E^2PROM device and provides a bi-directional data port.

- Pin 14 SCL/PnP Address Port (Output)

  When an E^2PROM is used, this dual function pin is connected to the external E^2PROM clock input (pin 6). At power-up, this pin is an input (with an internal 100 kΩ pull-up) that selects between two alternate PnP Address Ports used to configure the CS4235. Assuming APSEL (CS4235 pin 89) has a pull-down resistor attached, SCL without a pull-down resistor selects 308h as the PnP Address Port. When SCL is pulled low with a 10 kΩ resistor to ground, the Address Port is 388h. This strapping scheme is illustrated in Table 4.

PnP ADDR	SCL (Pin 14)	APSEL (Pin 89)
0x279	No Pull-down	No Pull-down
0x308	No Pull-down	10 kΩ Pull-down
0x388	10 kΩ Pull-down	10 kΩ Pull-down

Table 4. PnP Address Selection

Joystick Interface Pins

- Pins 68, 63 JACX, JACY (Inputs)

  These pins are the X/Y coordinates for Joystick A. They should have a 5.6 nF capacitor to ground and a 2.2 kΩ resistor to the joystick connector pins 3 and 6, respectively.

- Pins 67, 64 JBCX, JBCY (Inputs)

  These pins are the X/Y coordinates for the second joystick, Joystick B. Each signal should have a 5.6 nF capacitor to ground and a 2.2 kΩ series resistor to the joystick connector pins 11 and 13, respectively.

- Pins 70, 61 JAB1, JAB2 (Inputs)

  These pins are the switch inputs for Joystick A. These signals should connect to joystick connector pins 2 and 7 respectively, as well as have a 1 nF capacitor to ground. Unlike the CS423xB codecs, external 4.7 kΩ pull up resistors are not required on these pins. The pull-up resistors are internal to the CS4235.

- Pins 69, 62 JBB1, JBB2 (Inputs)

  These pins are the switch inputs for the second joystick, Joystick B. These signals should connect to joystick connector pins 10 and 14 respectively, as well as have a 1 nF capacitor to ground. Unlike the CS423xB codecs, external 4.7 kΩ pull up resistors are not required on these pins, the pull-ups are internal to the CS4235.

- Pin 60 MIDOUT (Output)

  This output is used to send MIDI data serially to an external MIDI device. Normally this signal connects directly to pin 28 of the CS9236 wavetable device, through a transistor buffer circuit to pin 12 of the joystick connector, and through a TTL buffer to pin 10 of the CS4610 X-link connector.

- Pin 59 MIDIN (Input)

  This input is used to receive serial MIDI data from an external MIDI device. This pin should be connected to pin 15 of the joystick connector for use with break-out boxes. This pin has an internal pull-up and does not require external pull-up resistors.

CS4610 DSP Interface Pins

- Pin 4 FSYNC (Output)

  Frame Sync is a 4 mA output pin and serves as the serial frame sync signal when the serial port is enabled (SPE=1 in I16). This pin should be connected through a buffer to pin 2 on the CS4610 X-link connector, or directly to pin 77 on the CS4610 if no cabling is required.

- Pin 7 SCLK (Output)

  Serial Clock is a 4 mA output drive pin and functions as the DSP serial clock signal when SPE=1 in I16. This pin should be connected through a buffer to pin 8 on the CS4610 X-link connector, or pin 74 on the CS4610 if no cabling is required.

- Pin 5 SDOUT ($\overline{\text{ACDCS}}$ enable)(Output)

  Serial Data Output is a dual function pin and also serves as the Alternate CDROM Chip Select Enable when pulled low with a 10 kΩ resistor to SGND. This 4 mA drive output pin is the serial data output when the serial port is enabled (SPE=1 in I16), and should be connected through a buffer to pin 4 on the CS4610 X-link connector, or directly to pin 76 on the CS4610 if no cabling is required. Loading must be limited to CMOS inputs if this pin has the 10 kΩ resistor attached.

- Pin 6 SDIN Input (Input)

  The Serial Data pin is the serial data input when the serial port is enabled (SPE=1 in I16). This pin connects to pin 6 on the CS4610 X-link connector, or directly to pin 75 on the CS4610 if no cabling is required.

CS9236 Interface Pins

- Pin 1 SDATA (Input)

  This pin should be connected to the SOUT output (pin 8) on the CS9236. This pin should also have a weak pull-down resistor of approximately 100 kΩ to minimize power-down currents and allow for stuffing options.

- Pin 2 LRCLK (Input)

  This input pin should be connected to the LRCLK output (pin 7) on the CS9236. This pin should also have a weak pull-down resistor of approximately 100 kΩ to minimize power-down currents and allow for population options.

- Pin 3 MCLK (Output)

  MCLK is a dual function pin that supplies the 16.9344 MHz master clock that controls all the timing on the CS9236, and should be connected to pin 2 (MCLK) on the CS9236. When this pin is pulled low with a 10 kΩ resistor to SGND, it enables the CDROM interface (over the upper four ISA address pins). If the MCLK trace length is greater than 2 inches, add a 33 Ω series terminator resistor.

- Pin 15 $\overline{\text{BRESET}}$ (Output)

  This pin provides the software power down and reset control over devices connected to the codec. This pin should be connected to pins 31-32 on the CS9236.

Volume Control Pins

- Pin 16 $\overline{\text{DOWN}}$ (I/O)

  This pin is enabled when VCEN is set in Control register C0 or the Hardware Configuration data. When $\overline{\text{DOWN}}$ is low, the master volume output is decremented. VCEN has precedence over the other pin functions. This pin is multiplexed with two other functions, and defaults to the XCTL1 output controlled by the XCTL1 bit

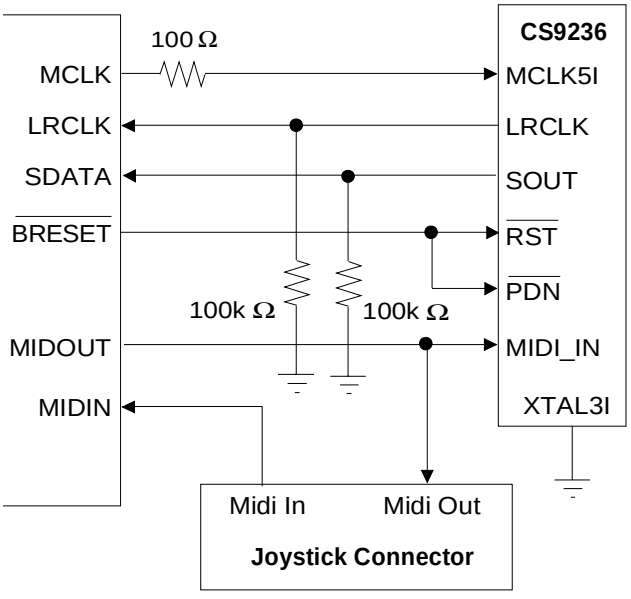


Figure 2. CS9236 Interface

in the WSS I10. This pin can also be configured at a second CDROM Chip Select, $\overline{ACDCS}$, to support the alternate IDE CDROM decode (see section *CDROM Interface Pins*). To us this pin as an CDROM alternate chip select, an external 10 kΩ resistor is tied between SDOUT and SGND. Note the capacitor values shown in Figure 3 are now 0.01 µF.

- Pin 9 $\overline{UP}$ (Input)

  The volume $\overline{UP}$ pin is enabled when VCEN is set in Control register C0 or the Hardware Configuration data. When $\overline{UP}$ is low, the master volume output is incriminated.

- Pin 95 $\overline{MUTE}$ (Input)

  The volume Mute pin is enabled when VCEN is set in Control register C0 or the Hardware Configuration data. The MUTE function can be momentary, or non-existent based on VCF1 bit.

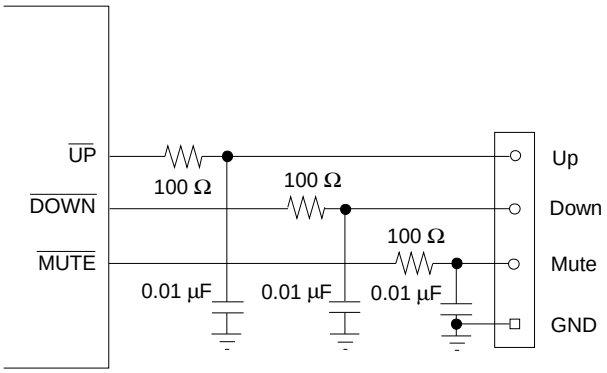


Figure 3. Volume Control

Crystal Oscillator Pins

- Pin 100 XTALI (Input)

  XTALI is used for a crystal placed between this pin and XTALO (pin 99), but will accept an external CMOS clock. The crystal frequency must be 16.9344 MHz and is designed for fundamental mode, parallel resonance operation. The parallel capacitor value is typically 22 pF.

- Pin 99 XTALO (Output)

  XTALO is used for a crystal placed between this pin and XTALI (pin 100). The crystal frequency must be 16.9344 MHz and is designed for fundamental mode, parallel resonance operation. The parallel capacitor value is typically 22 pF. If an external 16.9344 MHz clock is used on XTALI, this pin must be left floating with no traces or components connected to it.

Analog Filter Pins

- Pin 78 VREF (Output)

  This pin is nominally biased at 2.1 Volts and should be filtered with a 0.1 µF and 10 µF capacitor in parallel. VREF is normally used to bias the Line Out and Microphone Input amplifier circuits. If the VREF trace is long, the RC filter shown in Figure 4 should be used to attenuate coupled noise before reaching the amplifies.

  NOTE: VREF can only supply 0.4 mA or less of DC current.

- Pin 79 REFFLT (Input)

  Voltage reference used internal to the codec. Connect a 0.1 µF and a 1 µF capacitor with short thick traces between this pin and AGND. No other connections should be made to this pin.

- Pin 87 FLT3D (Input)

  This pin is the 3D filter and requires a 0.01 µF capacitor attached from this pin to AGND.

- Pin 77 FLTO (Output)

  A 1000 pF NPO or COG capacitor must be attached between this pin and FLTI (pin 76). Exercise care to use the absolute minimum trace length.

- Pin 76 FLTI (Input)

  A 1000 pF NPO or COG capacitor must be attached between this pin and FLTO (pin 77). Ex-

ercise care to use the absolute minimum trace length.

Analog Input Pins

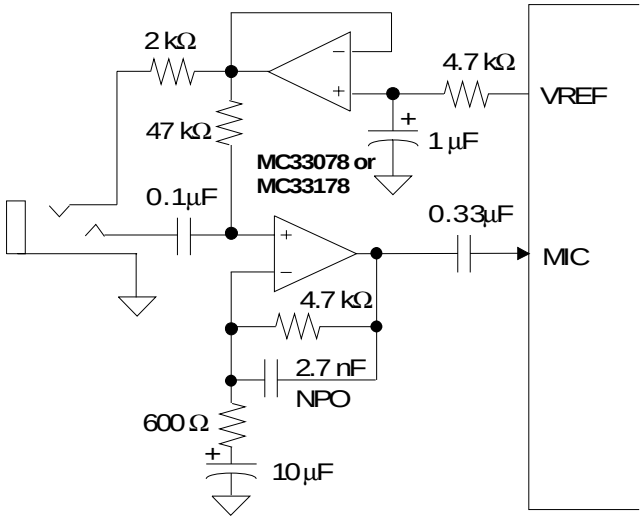


Figure 4. Mic Input

- Pin 83 MIC (Input)

  MIC is normally used as the microphone input and centered around VREF. This input must be AC coupled with a 0.33 µF or larger NPO capacitor. The schematic is shown in Figure 4. The 20 dB gain microphone preamplifier should be powered from a single +5 Volt analog source to prevent reverse biasing the input. Stereo microphone inputs are not supported on the CS4235.

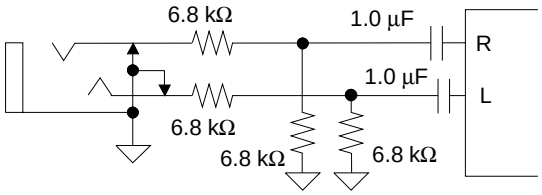


Figure 5. Line Input

- Pin 75 LAUXI (Input)

  Typically used for an external Left Line input and centered around VREF, this pin is connected to the Line In jack through a 1.0 µF capacitor and -6 dB resistor-divider. With the -6 dB resistor-divider, the maximum input signal level is 2 V_{RMS} at the Line In jack. A programmable gain block is located in register I2.

- Pin 74 RAUX1 (Input)

  Typically used for an external Right Line input and centered around VREF, this pin is connected to the Line In jack through a 1.0 µF capacitor and -6 dB resistor-divider. With the -6 dB resistor-divider, the maximum input signal level is 2 V_{RMS} at the Line In jack. A programmable gain block is located in register I3.

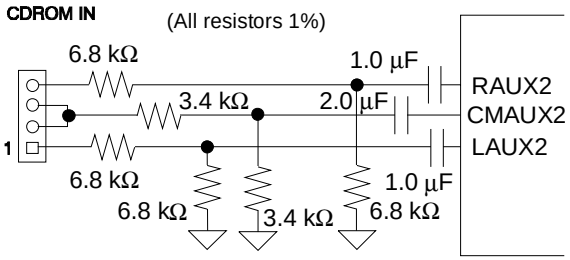


Figure 6. CDROM Input

- Pin 85 LAUX2 (Input)

  Typically the left channel CDROM input and centered around VREF, this pin is connected to the CDROM audio connector through a 1.0 µF capacitor and -6 dB resistor-divider. With the -6 dB resistor-divider, the maximum input signal level is increased to 2 V_{RMS} at the CD connector. A programmable gain block is located in register I4. The schematic for the CDROM analog input is illustrated in Figure 6.

- Pin 84 RAUX2 (Input)

  Typically the right channel CDROM input and centered around VREF, this pin is connected to the CDROM audio connector through a 1.0 µF capacitor and -6 dB resistor-divider. With the -6 dB resistor-divider, the maximum input signal level is 2 V_{RMS} at the CD connector. A programmable gain block is located in register I5. The CDROM input schematic is illustrated in Figure 6.

- Pin 96 CMAUX2 (Input)

  Common mode ground input for the LAUX2 (pin 85) and RAUX2 (pin 84) inputs. Typically this pin is connected to the CDROM ground connector through a 2.0 µF capacitor and -6 dB resistor-divider to provide common-mode noise rejection. The impedance on this pin should be one half the impedance on LAUX2 and RAUX2.

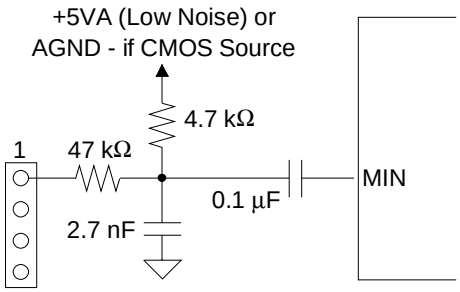


Figure 7. MIN In

- Pin 88 MIN (Input)

  Nominally used to mix the typical "beeper" signal on most computers into the audio system. This pin is connected to a 0.1 µF capacitor, a 4.7 kΩ pull-up resistor, and RC filter as shown in Figure 7. This input has a programmable gain stage (I26) into both channels of the output mixer. Any pull-up resistor used in the Mono In circuitry must be connected to regulated +5 VA. Connecting mono in circuitry to V_{CC} will results in excessive system noise.

Analog Output Pins

- Pin 73 LOUT (Output)

  Analog output from the codec for the left channel. The maximum signal level is 1 V_{RMS}, centered around VREF (2.1 Volts). A 1000 pF NPO or COG capacitor must be attached from this pin to AGND with a short trace. This signal can be DC coupled to the output amplifier if the amplifier is biased at VREF, otherwise a AC coupling capacitor is required. The analog output cannot be used to directly drive headphones or loads less than 10 kΩ. Therefore, this output should always be buffered before the output jack.

- Pin 72 ROUT (Output)

  Analog output from the codec for the right channel. The maximum signal level is 1 V_{RMS}, centered around VREF (2.1 Volts). A 1000 pF NPO or COG capacitor must be attached from this pin to AGND with a short trace. This signal can be DC coupled to the output amplifier if the amplifier is biased at VREF, otherwise a AC coupling capacitor is required. The analog output cannot be used to directly drive headphones or loads less than 10 kΩ. Therefore, this output should always be buffered before the output jack.

Unused Pins

- Pins 82, 86 NC

  These pins are not connected on the CS4235 audio codec.

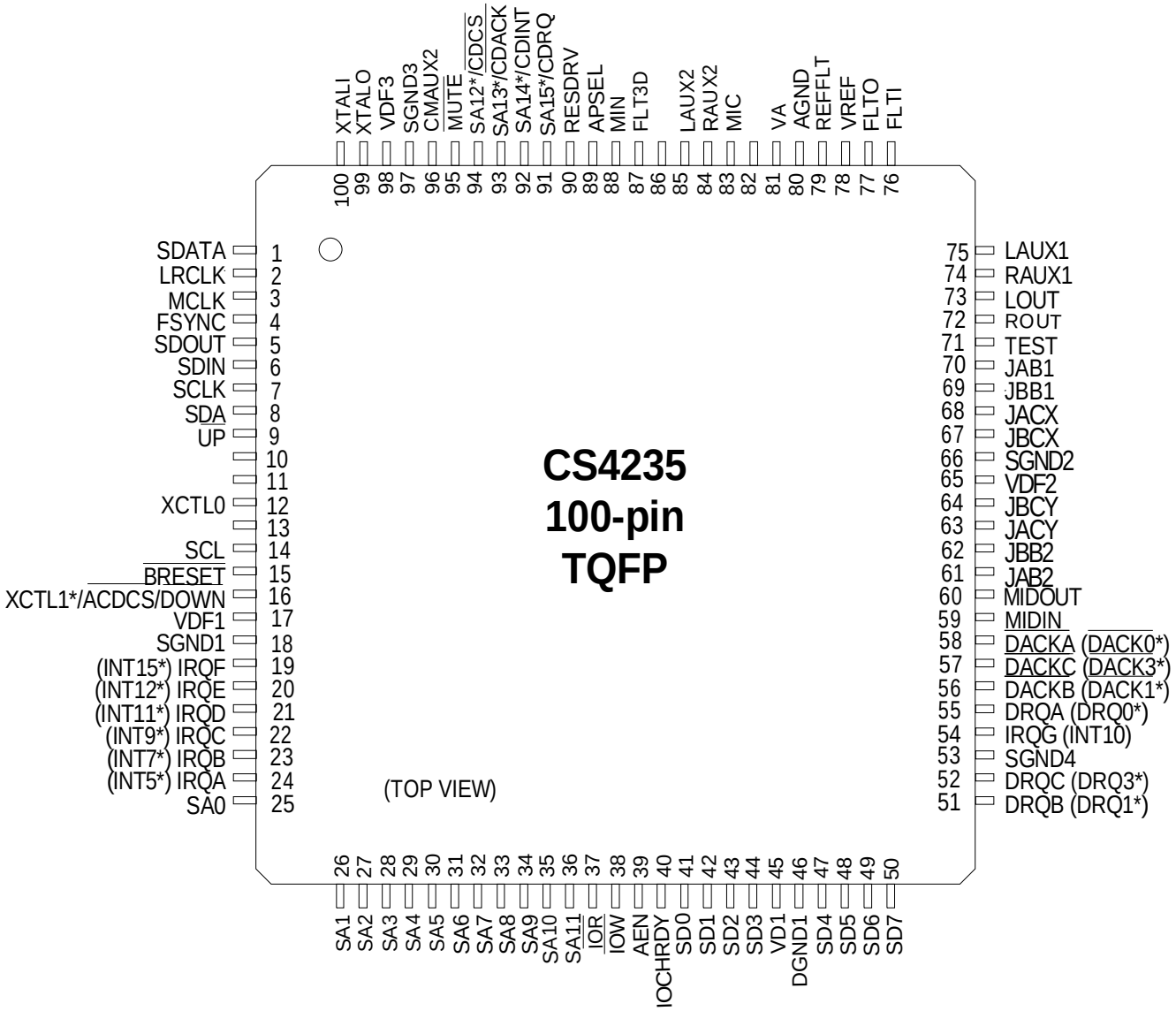
Board Layout checklist

This checklist should be used by the audio circuit designer and board layout specialist as a general guideline in the planning, layout, and review process to insure the highest sound quality.

- ❑ The analog pins of the CS4235 are internally biased near 2.1 Volts. In the cases where electrolytic polarized capacitors are used for cost or frequency response considerations, the positive terminal must be connected to the codec pin. Reversing the polarity will reverse bias the capacitor. Although there is inadequate current to damage the capacitor, it may become excessively leaky. This leakage will result in pops and "zipper" noise when changing the mixer input settings.
- ❑ Avoid using vias under the audio codec to reduce the risk of flux contamination, or use solder mask to cover the vias. Modify the spacing of through hole crystals to suspend them off the printed circuit board to aid the cleaning process.
- ❑ Select the proper size voltage regulators (do not use a 78L05). Use the regulator calculator at www.crystal.com to help select the properly rated device.
- ❑ Use multi-layer boards with internal power and ground planes to improve audio performance and EMI compliance. Do not overlap digital and analog planes.
- ❑ Partition the audio circuitry in one section and the digital circuitry in another. The separation should be duplicated on all layers including the power and ground planes.
- ❑ Route analog signal traces only above the analog ground and digital traces above the digital ground.
- ❑ When placing audio on a mother board, never create an audio "island" in the center of the board. The audio partitions should be located at the edge of the board.
- ❑ Analog and digital grounds should be connected together at one point to establish a common voltage. In most layouts the best tie point is close to a chassis ground location, at the analog voltage regulator, or at the power supply connector entry point. Typical designs connect these two planes together with a ferrite bead next to the power supply pins. Provide other locations for alternative connections and characterize the audio performance for the optimum location.
- ❑ Decoupling capacitors should be located next to the component power supply pins, connected with short traces. Avoid the use of vias on decoupling capacitors. Using two different decoupling capacitor values will increase the spectral bandwidth RF suppression.
- ❑ Use bypass capacitors at I/O locations to remove unwanted RF energy. Use SMT components for bypassing, since their self resonance is ten times greater than leaded components.
- ❑ Use ground guards in the high speed digital sections to reduce magnetic coupling between signal traces.
- ❑ Route clock traces first, on internal layers if possible, and never near the edge of the printed circuit board.
- ❑ The +5 Volt supply to the joystick (pins 1, 8, and 9) must be current limited to comply with UL safety regulations. Do no use the +5 VA voltage regulator to limit the current supply. A polyfuse is desirable, since it will reset itself when allowed to cool down. A separate 78L05 voltage regulator will work well also.
- ❑ Use quality amplifiers with low noise numbers to drive analog signals. Using single supply opamps on the microphone inputs avoids the risk of negative voltage transients.

APPENDIX A

CS4235 Pinout



APPENDIX B

CS4235 & CS423xB Differences

1) RFILT and LFILT capacitors are no longer needed and should be removed. On the CS4235, these pins are renamed FLTI and FLTO and should have a capacitor placed between them. They are used for the Crystal 3D Sound circuitry. Not populating this capacitor will not have any adverse affects on the part, but will result in non-optimum 3D Sound.
2) The external L/RLINE analog inputs are no longer supported. LLINE is now FLT3D and is used for the 3D Sound function. A 0.01 µF capacitor should be placed between this pin and analog ground. When external analog wavetable is desired, the AUX1 analog inputs should be used.
3) The analog microphone inputs are now mono. LMIC is changed to MIC, and RMIC has been removed.
4) Mono Out, MOUT, has been removed. The pin is redefined as APSEL and used to change the PnP Address Port. APSEL has an internal pull-up, setting the Address Port to 0x279 for backwards compatibility.
5) VDF4 has been changed to IRQG - a seventh interrupt (typically used for INT10). The default is disabled to provide backwards compatibility.
6) The Modem Logical Device has been removed. This includes MCS and MINT.
7) Support for an external synthesizer has been removed. This includes SCS and SINT.
8) The peripheral port has been removed. This includes XD<7:0>, $\overline{\text{XIOR}}$, $\overline{\text{XIOW}}$, and XA<0:2>. CDROM applications must now drive the ISA bus directly or through buffers.
9) The hardware strap enable for the CDROM has been moved. CS423xB designs have a pull-down on $\overline{\text{XIOR}}$. To support the CDROM interface on the CS4235, the pull-down must be moved to the MCLK pin. Also, to enable the alternate CDROM chip select pin ACDCS, a pull-down must be added to pin SDOUT.
10) The DSP serial port is no longer supported as an option on the 2nd Joystick connector. The DSP port is still located on pins 4 through 7.
11) There is no 3.3 V ISA support.
12) The consumer IEC-958 (S/PDIF) output, supported on the CS4237B and CS4238B, has been removed.
13) Only two modes of Hardware Volume Control are supported: 2-button, and 3-button with momentary mute.
14) Pull-up resistors have been added to the four Joystick Button pins, three Hardware Volume Control pins, and the MIDIN pin.
15) The capacitor values for the hardware volume control circuitry must be increase to 0.01 µF.

• Notes •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