Jitter Attenuation Performance of the CS61575 and CS61574A PCM Line Interface Circuits

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SUMMARY

This application note helps customers choose between the CS61575 and CS61574A. Both the CS61575 and CS61574A are pin-compatible, higher performance alternatives to the CS61574. Performance improvements include a reduction in power requirements by 50%, a guarantee of 14 dB of transmitter return loss, and an optional B8ZS/AMI/HDB3 coder. Both the CS61575 and CS61574A provide all these advantages, and differ only in the areas of receiver jitter transfer function and receiver propagation delay.

In summary, the CS61575 is designed for systems needing to meet AT&T 62411 jitter transfer requirements. The CS61574A is the logical choice for all other systems (i.e., those systems not requiring AT&T 62411 certification). The CS61575 has improved jitter transfer relative to the CS61574A and CS61574 when the input jitter amplitude exceeds 23 Unit Intervals (UIs) at a frequency in the attenuation range. This improved transfer comes at the expense of longer propagation delay through the receiver; typically a 96-bit delay for the CS61575 versus 16-bits for the CS61574A and CS61574. Also, attenuation begins at a jitter frequency of 3 Hz for the CS61575 compared to 6 Hz for the CS61574A.

However, the summary statement that the CS61575 should be used for 62411 applications is qualified as follows: If a system employing the CS61574 has previously been certified as compliant with 62411, a system upgraded to the CS61574A will continue to pass the same certification procedure. (The CS61575 would also pass the same certification tests). This qualification is elaborated upon in a later section.

JITTER ATTENUATOR CIRCUIT DESCRIPTION

This section describes the jitter attenuator circuitry of the CS61575 and CS61574A. This provides a basis for more detailed discussion of the performance differences of the two ICs.

Figure 1 shows the attenuator circuitry. The jitter attenuator reduces jitter in the recovered clock signal. It consists of a FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted in fine steps

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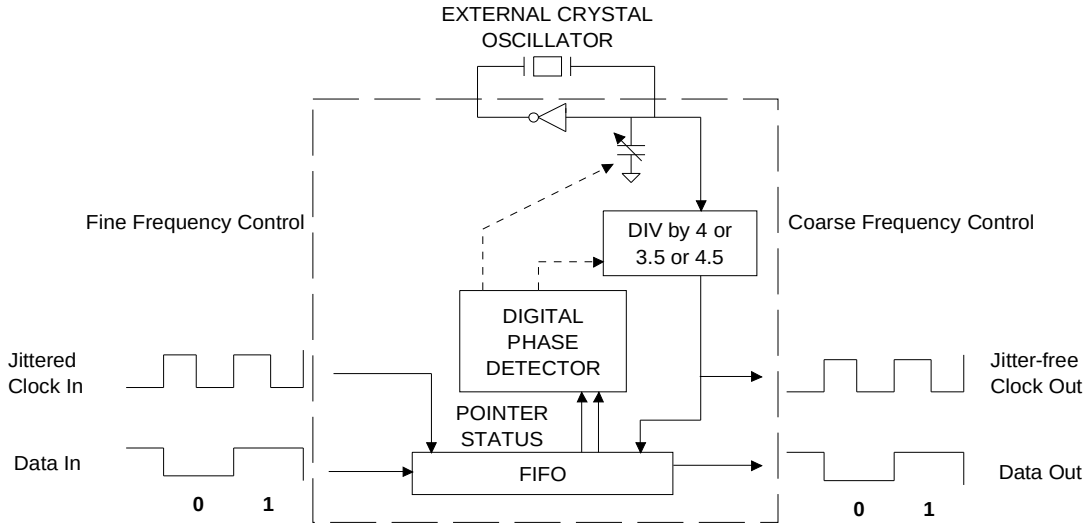

Figure 1 - Jitter Attenuator Block Diagram

to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Signal jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3.5 or divide by 4.5 to prevent the FIFO overflow or underflow. This is a coarse adjustment of the outgoing clock. During this activity, data will never be lost, but jitter gain occurs.

The jitter attenuator of the CS61575 contains a 192-bit FIFO, and will tolerate 138 UIs at 1 Hz and 28 UIs at 300 Hz as required by 62411 (Figure 2), while attenuating the jitter. The jitter attenuators of the CS61574A and CS61574 contain a 32-bit FIFO, and will typically tolerate 23 UIs (at a frequency in the attenuation range) before the overflow or underflow mechanism takes effect increasing output jitter to prevent data loss.

PERFORMANCE IMPLICATIONS OF ATTENUATOR DESIGN

As shown in Figure 2, the CS61575, CS61574A and CS61574 all tolerate the input jitter defined by AT&T 62411. (Note that all other recent standards require a maximum tolerance of 10 UIs). However, when the input amplitude exceeds 23 UIs, the CS61575 continues to provide a continuous jitter transfer function. As shown in Figure 2, when more than 23 UIs are input to the CS61574A, CS61574 or similar devices (such as the LXT300), the divide by 3.5 or 4.5 mechanism produces jitter gain.

If the CS61574 has discontinuities in the transfer function, then how can it be that systems using the CS61574 have routinely passed 62411?

One answer is that most sophisticated systems contain a system synchronizer (PLL) and one frame buffer (FIFO) per trunk (Figure 3). In fact, all systems which meet Stratum 4 (Type 1), Stratum 3 or Stratum 2 requirements will have a synchronizer. The synchronizer/FIFO can provide attenuation which is incremental to that provided by the CS61574A or CS61574 on the trunk card.

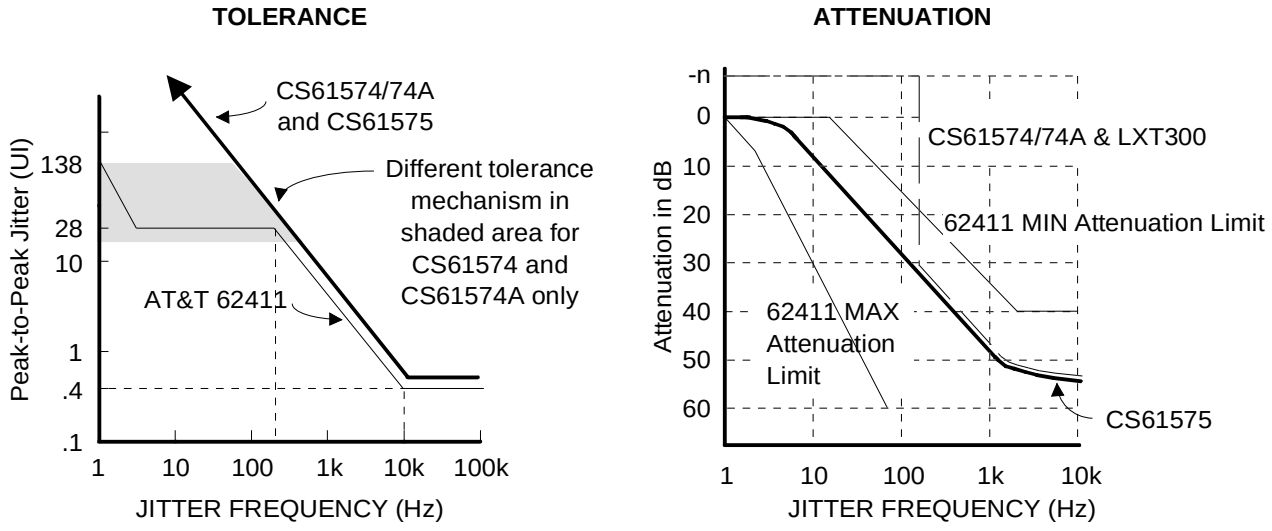

Figure 2 - Jitter Performance Differences of CS61575 and CS61574A/CS61574

Note that smaller systems (typically systems with a single T1 trunk attached) are often Stratum 4 (Type 2) systems. See Figure 4. These systems lack a system synchronizer, and should always use the CS61575.

Another answer to the question "how can systems using the CS61574 pass 62441" is that many test laboratories have historically not been equipped to generate and receive more than 10 UIs of jitter. These labs would be unable to distinguish the performance difference of the CS61575 and CS61574A. Newer test equipment (often custom equipment designed by a lab) is capable of generating/receiving more than 10 UIs of jitter. For example, the AT&T labs now have the capability to measure the length of frame buffers located inside a system. With that sophisticated test capability, jitter gain by a divide by 3.5 or 4.5 is detectable.

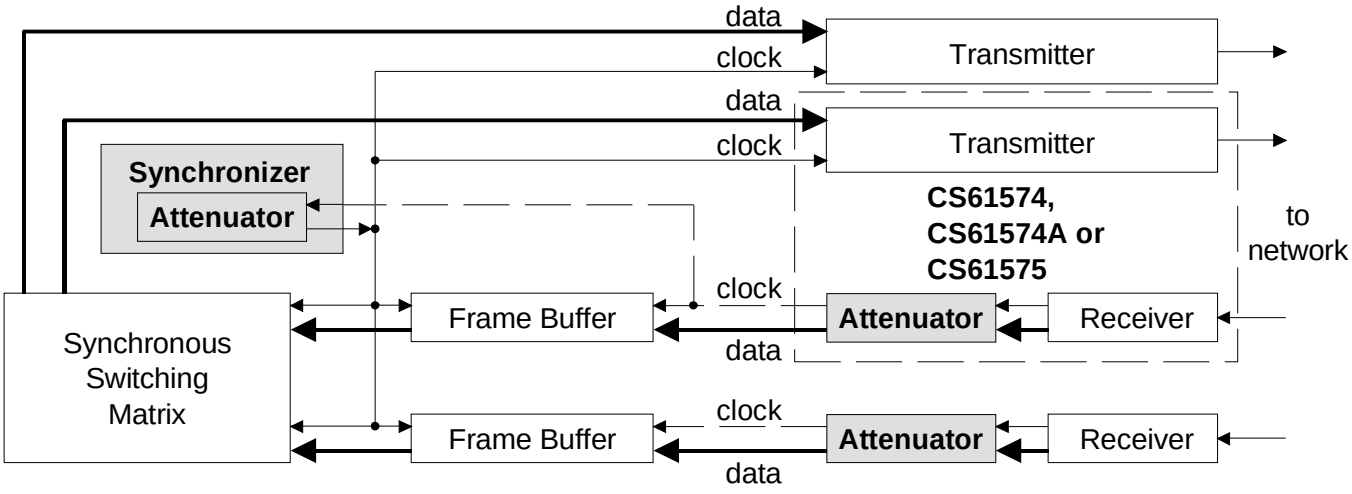

Figure 3 - Using the CS615x4 in AT&T 62411 Stratum 2,3 or 4(Type 1) Systems

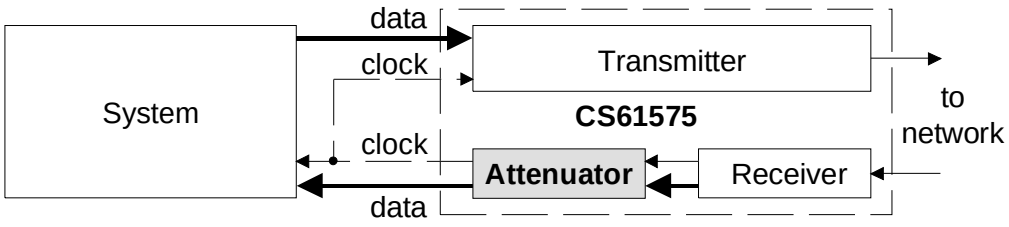

Figure 4 - Using the CS61575 in AT&T Stratum 4 (Type 2) Systems

CHANGES IN AT&T 62411 REQUIREMENTS

In December 1990, AT&T changed the high-frequency jitter transfer test procedures used at 62411 certification labs. Whereas 62411 formally required 60 dB of attenuation (a performance level not achieved under all operating conditions by any line interface IC from any vendor), the latest 62411 spec requires only 40 dB of attenuation.

AT&T made this change at the request of equipment manufacturers who demonstrated that the attenuation performance of the CS61574 was consistent with the requirements for robust and reliable network performance. Note that 60 dB of attenuation implies 0.0002 UI of output jitter at spot frequencies. This amplitude is so small as to be barely measureable. 40 dB of attenuation implies 0.002 UI of output jitter at spot frequencies.