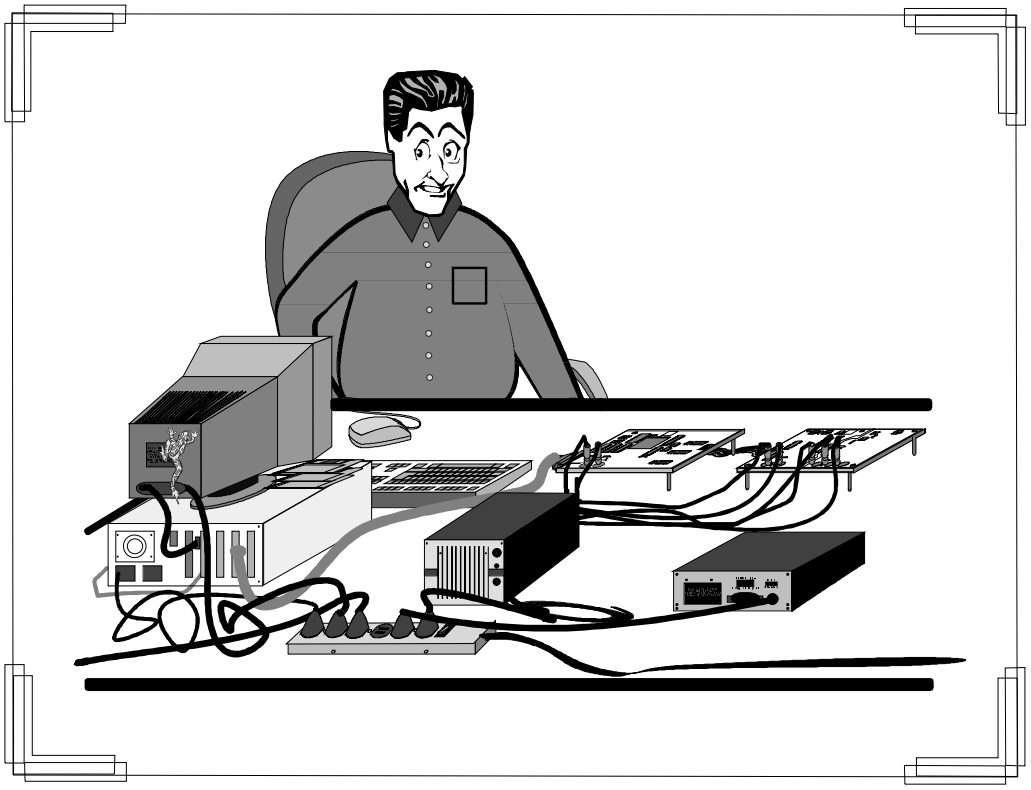
A Cirrus Logic Company

AN38

Application Note

Using The Capture Evaluation System

By John Lis



The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor analog to digital converter to a PC-compatible computer. It is software adaptable to be used with a variety of Crystal Semiconductor ADCs. When operating, digital data is collected from the analog to digital converter, then transferred to the PC over a serial COM port. Once the data is in the PC, evaluation software is included to analyze the data and display the analog to digital converter's performance. The evaluation software permits time domain, frequency domain and noise histogram analysis.

The Crystal Semiconductor evaluation equipment is very easy to setup and use, and it will actually expedite system design and development. Setup time for the CDBCAPTURE evaluation system using a Crystal Semiconductor evaluation board is less than one hour. This includes clearing a work area, reading the instructions, and troubleshooting minor problems. Using the evaluation board, the performance of the analog to digital converter can be verified against data sheet specifications. As development continues, the evaluation system can then be used to measure system

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performance and isolate noise sources. Later on, the evaluation software can be modified for production test.

INITIAL SETUP:

Setup of the CAPTURE evaluation system is very easy. The setup begins with installing the CAPTURE Evaluation software on the PC. Next the power and signal cables are connected to the CAPTURE board, evaluation board, PC, signal generator and power supplies. With the setup complete, evaluation and test can begin.

Before installing the CAPTURE software on the PC, read the INSTALL.DOC file on the CDBCAPTURE Evaluation software diskette. This file contains instructions on software installation. After the software installation is complete, read the README.DOC file in the PC's CAPTURE directory. The README.DOC file contains valuable information concerning hardware requirements, setup, evaluation board configuration, software operation, PC setup, and special notes.

The PC used for the CAPTURE evaluation system has to be a PC AT, PS/2 or compatible with at least four megabytes of Extended Memory. If the CAPTURE evaluation system does not operate properly upon setup, investigate the following items:

- Availability and configuration of Extended Memory on the PC (4 meg, VCPI compatible)
- Sufficient amount of disk space available on the PC (4 meg required)
- CONFIG.SYS proper modification (see README.DOC)
- EMM386 the only memory manager
- Run "CAPTURE -config" to adjust PC hardware
- Power supply voltage and current levels
- Carefully check all the power cables
- Carefully check all the signal cables
- Verify the appropriate COM port
- Possible hardware conflict among PC add-in circuit boards
- Evaluation board jumpers and DIP switch settings

CDBCAPTURE EVALUATION SOFTWARE:

Execution of the evaluation software begins by typing "CAPTURE<RTN>". The screen shown in Figure 1 is displayed, prompting the user to select a part number and interface method. This is done from "SETUP" on the menu bar. Note that "SETUP" and "QUIT" are the only options available on this screen. With the evaluation software running, select the appropriate part number and capture board COM port by pointing and clicking on "SETUP". This procedure will download configuration software to the CDBCAPTURE circuit board via the COM port. When the "SETUP" is properly configured, the "TEST" option becomes enabled, permitting Time Domain, FFT and Noise Histogram tests.

The first test to perform is TIME DOMAIN, found under the "TEST" menu bar. The time domain test is used to verify proper operation and adjust the signal from the generator to the evaluation board. A sinusoid input signal is used, with its frequency adjusted to about 1 percent of the analog to digital converter's output word rate. The "COLLECT" button is pressed, and data is collected. A sine wave should be observed if everything is working. The amplitude is adjusted until it is near full scale. Figure 2 shows a near full scale signal for a CS5101A analog to digital converter. Exceeding full scale will cause the signal to clip and distort.

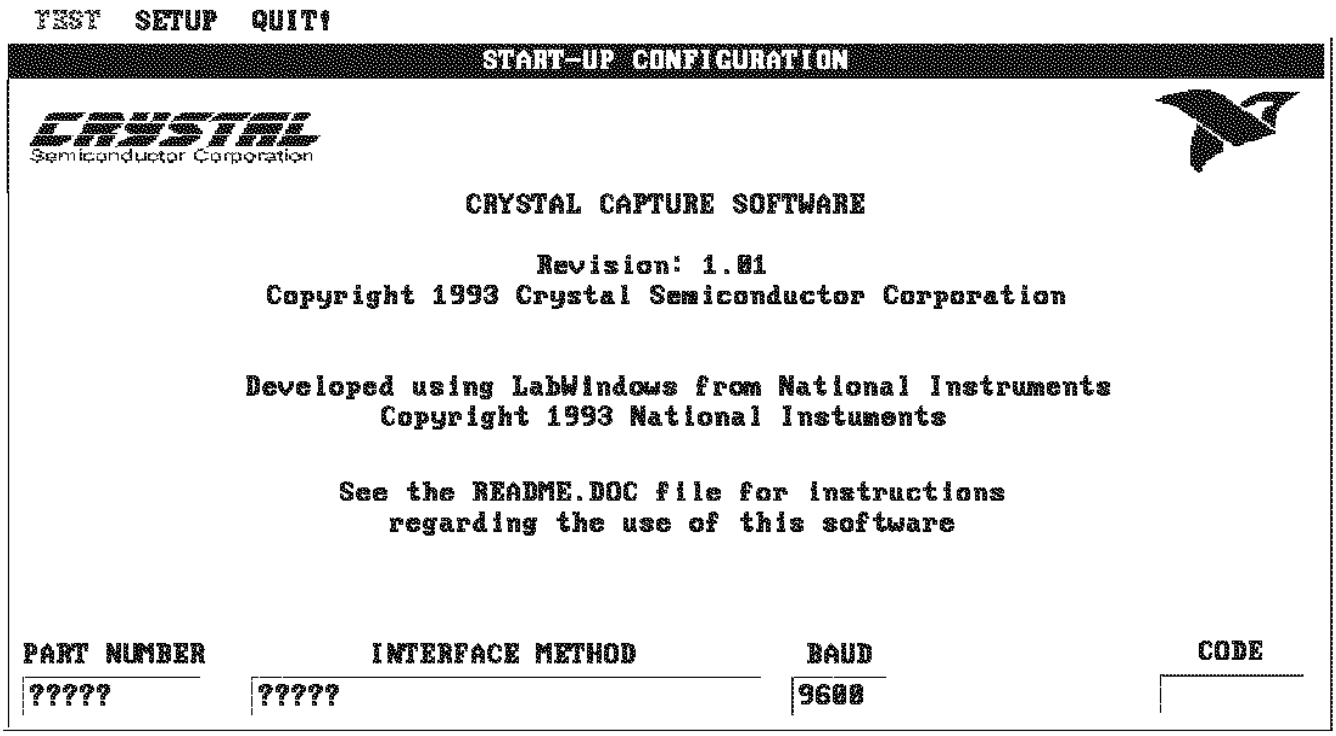

Figure 1

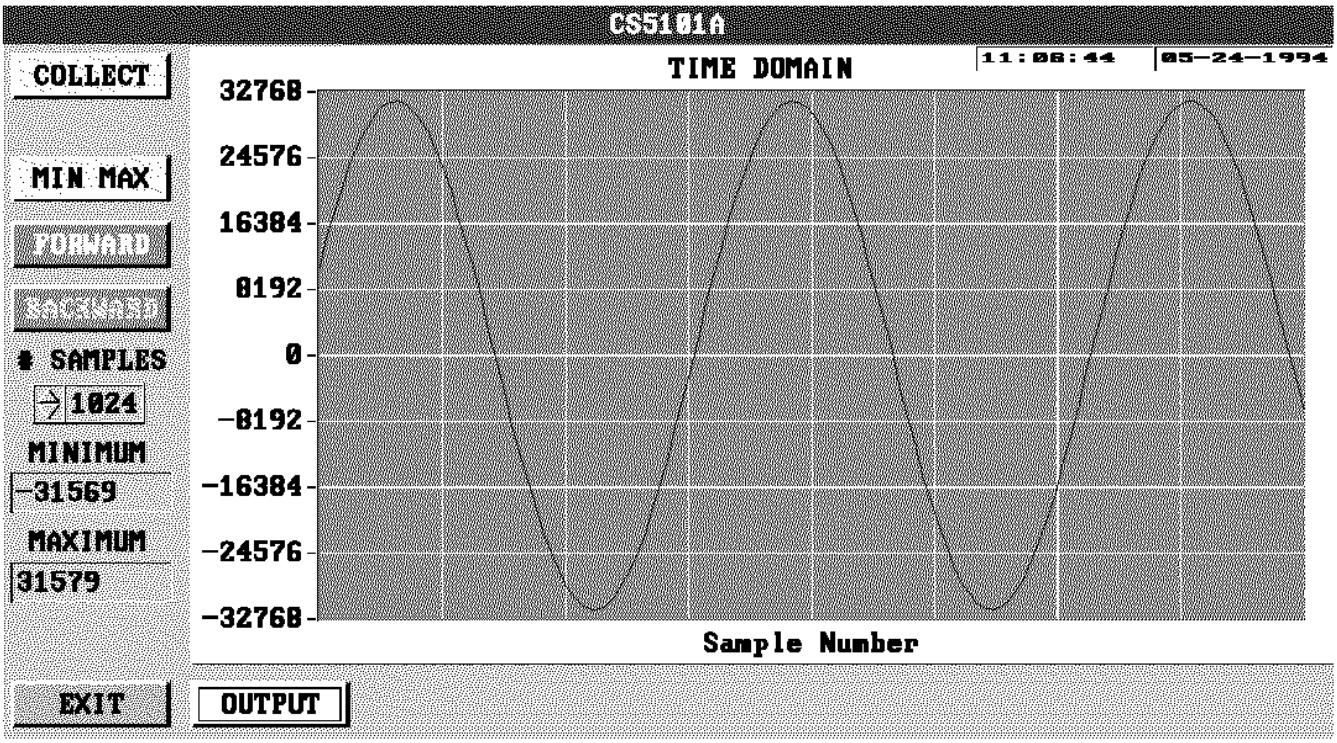

Figure 2.

With the amplitude of the input signal set to the desired value, the analog to digital converter can be tested in the frequency domain. Exit the "TIME DOMAIN" test and select the "FREQUENCY DOMAIN" test from the "TEST" menu bar. Adjust the frequency of the sinusoidal input to about 5 percent of the analog to digital converter's output rate. Figure 3 is an FFT of a 5kHz signal input to a CS5101A.

In Figure 3, the Signal to Noise Ratio (S/N) is 92.884 dB, this translates to 15.14 effective bits. The Signal to Distortion Ratio (S/D) of 95.146 dB is equivalent to 0.00175% Total Harmonic Distortion. These numbers reflect the performance of the entire system including the analog to digital converter, input filters, op-amps, and signal source.

The graph and statistics shown in Figure 3 are calculated from a sample set of data. These calculated values have an uncertainty that depends upon the variance of the sampled population. This uncertainty can be reduced by averaging multiple independent data sets. Figure 4 is an average of 25 FFTs and its uncertainty is five times less than the FFT in Figure 3. Notice how the noise floor at -120dB is much smoother.

1024 sample points of data were used in the FFTs shown in Figures 3 and 4. This translates to a frequency bin width of 50 Hz (Sample Rate/ Number of Samples =51200 Hz/1024). Collecting more samples (2048, 4096, 8192) for the FFT increases the frequency resolution. Figure 5 is a plot of an 8192 sample FFT averaged 25 times. Here the bin width decreased to 6.25 Hz, thus improving the resolution.

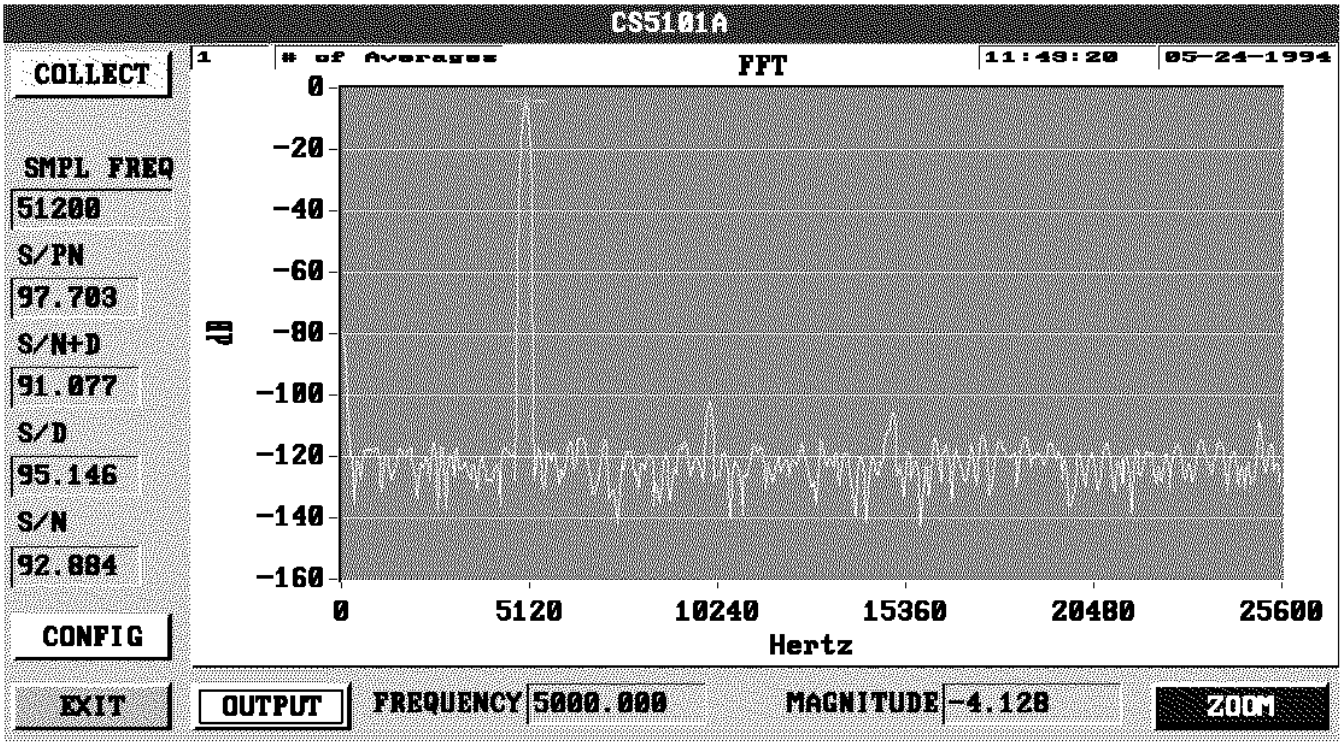

Figure 3.

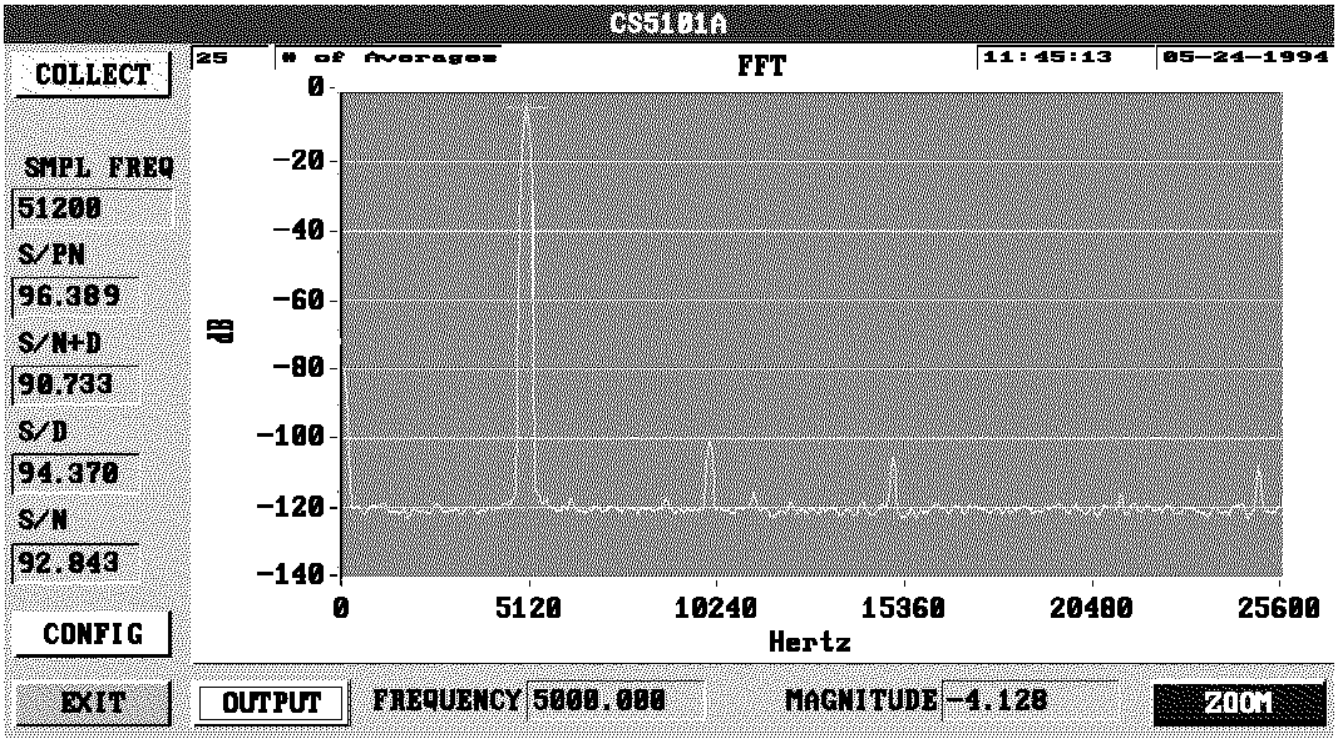

Figure 4.

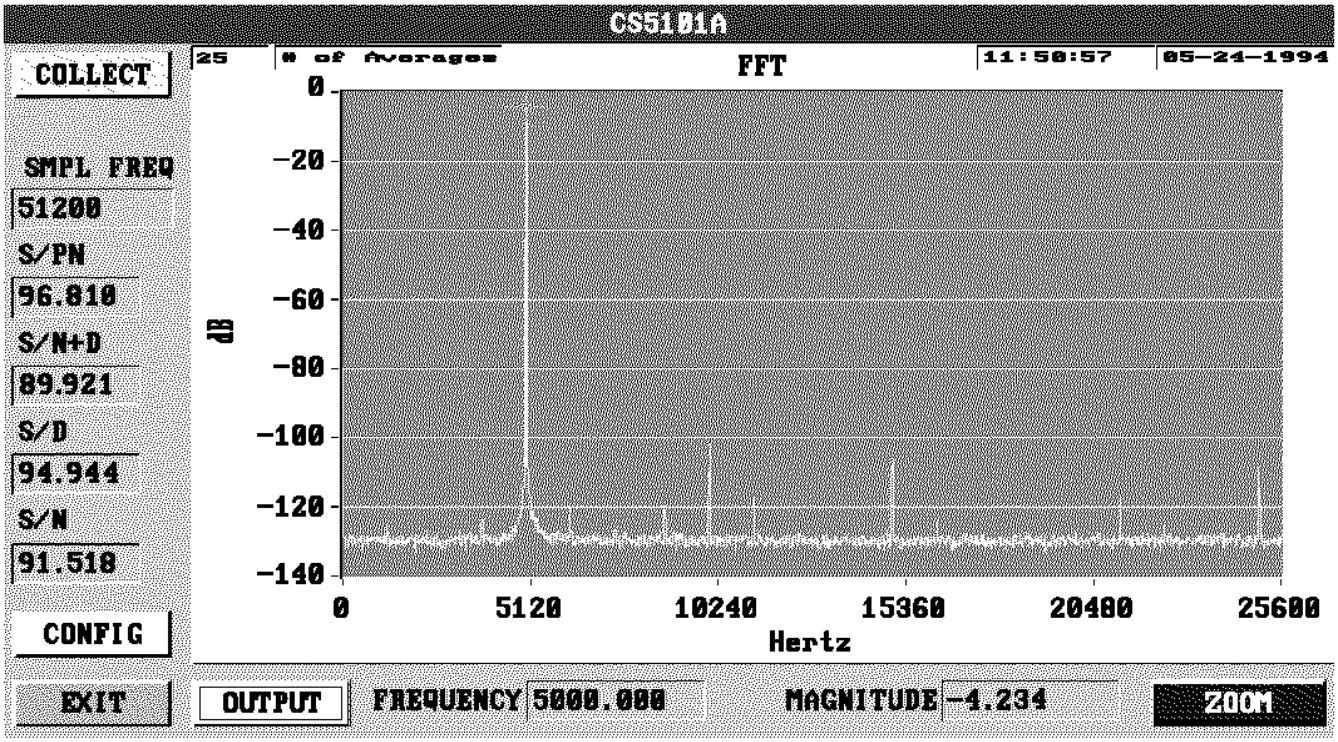

Figure 5.

Ideally, the signal to noise numbers in Figures 4 and 5 should match. However, the increased number of samples in Figure 5 has revealed new information. Notice that the base of the fundamental signal in Figure 5 is slightly smeared. This suggests jitter in either the signal source or sample clock. Also notice how the decrease in bin width from 50Hz to 6.25Hz reduced the spot noise floor by 9dB from -120dB to -129dB. Each doubling of the sample size yields a 3dB reduction in spot noise. Now more coherent noise sources are noticeable and knowledge of the frequency content can aid in isolating the source and improving performance. These noise sources were below the noise floor in Figure 4 and unnoticeable.

Increasing the number of samples from 1024 to 8192 doesn't reduce the uncertainty, so 25 FFTs are averaged for Figure 5. The additional information contained in the larger sample size goes toward higher frequency resolution. The number of averages used depends upon the amount of uncertainty acceptable and time available.

An analog to digital converter can also be tested with a DC signal. For this test, exit the "FREQUENCY DOMAIN" test and select "HISTOGRAM" test from the "TEST" menu bar. Histograms are used in the static testing of DC input signals. Here the input signal stays constant, and an ideal analog to digital converter would output only one code. Deviations from the ideal output are used to measure system performance.

Figure 6 is a Histogram of a CS5101A with its input grounded. The MEAN suggests that the analog to digital converter has an offset of -0.69 LSB. For a reference of 4.5 volts, and operating in bipolar mode, the offset translates to -94.8 microvolts. The standard deviation (STD DEV) is a measure of rms noise. Figure 6 has an STD DEV of 0.49 LSB which translates to 67.3 microvolts of rms noise. From Figure 4, the -120dB noise floor translates to 72 microvolts rms of noise. The STD DEV from the histogram test in Figure 6 indicates that the system rms noise increases by 4.7 microvolts when a signal source is included with the analog to digital converter.

The information presented in Figure 6 is again calculated from sampled data. Thus, there is uncertainty associated with each calculated value. This uncertainty is reduced by increasing the sample size of data. The sample size for the histogram in Figure 6 is 8192.

SUMMARY:

The CDBCAPTURE evaluation system is a valuable computer-aided engineering tool which assists in product development and evaluation. The CDBCAPTURE can quantify component and system performance. Histograms are available to measure the DC accuracy. From the histogram's statistics, the offset, gain error, and noise values can be estimated. FFTs are used with a sinusoidal input signal to measure dynamic performance. The FFT statistics estimate linearity and noise. Quantifying performance aids in system integration. This information can be used to identify noise sources and isolate performance issues to individual components. The result is a quicker time to market and reduced development costs.

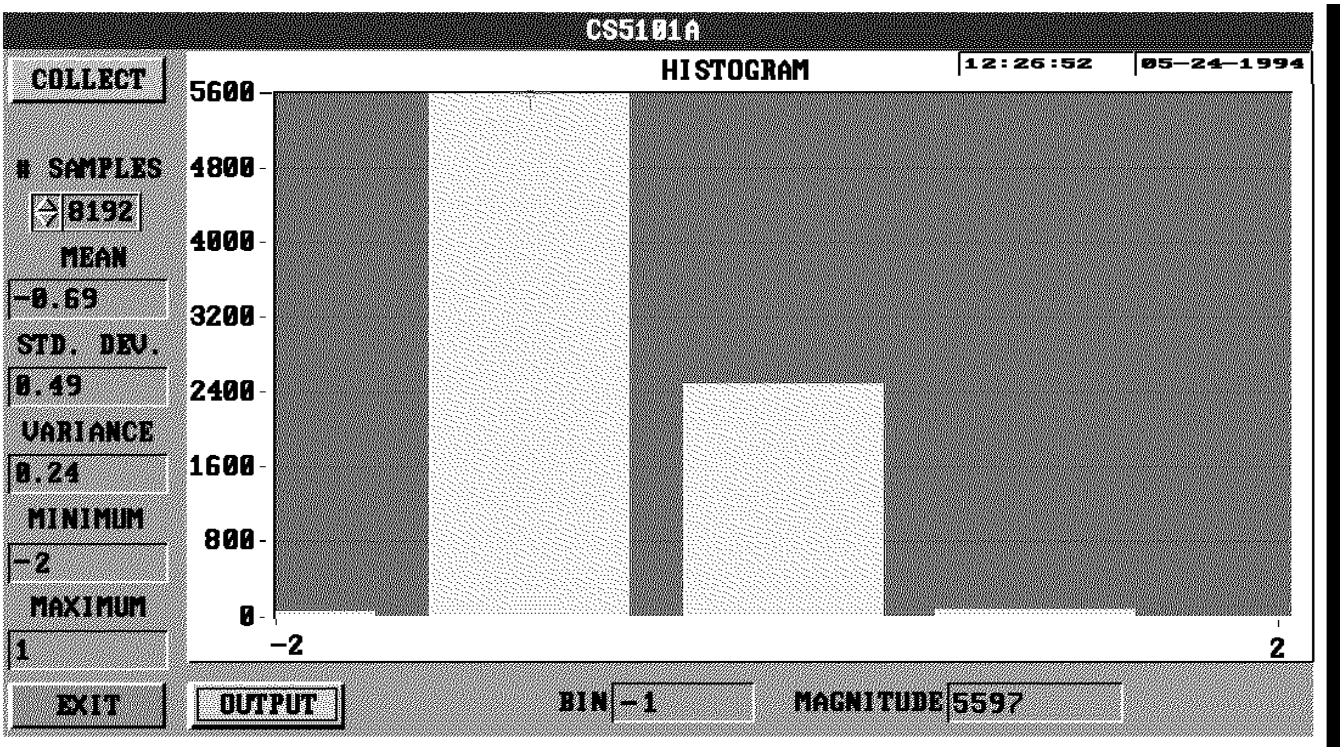
CS5101A
COLLECT
HISTOGRAM
12:26:52
05-24-1994
SAMPLES
8192
MEAN
-0.69
STD. DEV.
0.49
VARIANCE
0.24
MINIMUM
-2
MAXIMUM
1
5600
4800
4000
3200
2400
1600
800
0
-2
2
EXIT
OUTPUT
BIN -1
MAGNITUDE 5597

Figure 6.

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