

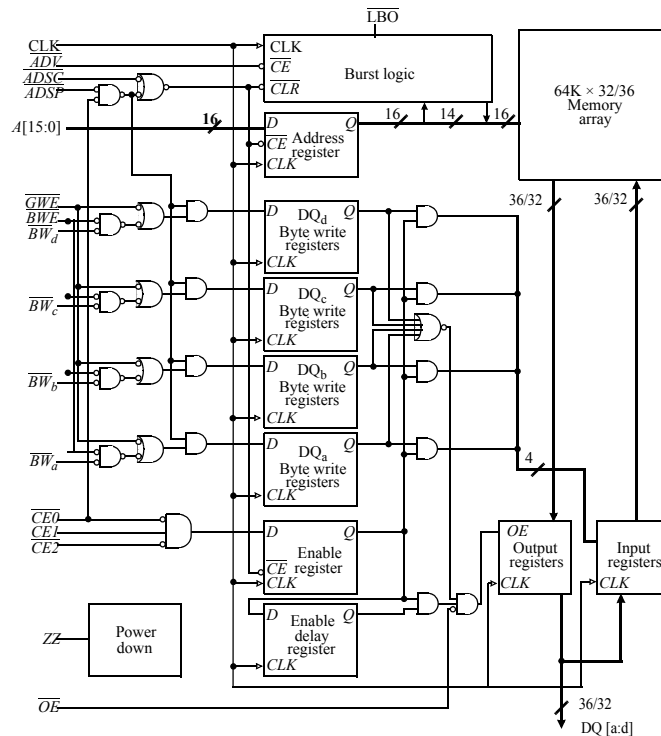


3.3V 64K X 32/36 pipeline burst synchronous SRAM

Features

- Organization: 65,536 words × 32 or 36 bits
- Fast clock speeds to 200 MHz
- Fast clock to data access: 3.0/3.5/4.0 ns
- Fast OE access time: 3.0/3.5/4.0 ns
- Fully synchronous register-to-register operation
- Single-cycle deselect
- Asynchronous output enable control
- Available in 100-pin TQFP package
- Linear or interleaved burst control
- Individual byte write and global write
- Snooze mode for reduced power-standby
- Common data inputs and data outputs
- Multiple chip enables for easy expansion
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V<sub>DDQ</sub>

Logic block diagram



Selection guide

	-200	-166	-133	Units
Minimum cycle time	5	6	7.5	ns
Maximum clock frequency	200	166	133	MHz
Maximum clock access time	3.0	3.5	4	ns
Maximum operating current	375	350	325	mA
Maximum standby current	130	100	90	mA
Maximum CMOS standby current (DC)	30	30	30	mA



**2 Mb Synchronous SRAM products list<sup>1,2</sup>**

Org	Part Number	Mode	Speed
128KX18	AS7C33128PFS18B	PL-SCD	200/166/133 MHz
64KX32	AS7C3364PFS32B	PL-SCD	200/166/133 MHz
64KX36	AS7C3364PFS36B	PL-SCD	200/166/133 MHz
128KX18	AS7C33128PFD18B	PL-DCD	200/166/133 MHz
64KX32	AS7C3364PFD32B	PL-DCD	200/166/133 MHz
64KX36	AS7C3364PFD36B	PL-DCD	200/166/133 MHz
128KX18	AS7C33128FT18B	FT	6.5/7.5/8.0/10 ns
64KX32	AS7C3364FT32B	FT	6.5/7.5/8.0/10 ns
64KX36	AS7C3364FT36B	FT	6.5/7.5/8.0/10 ns

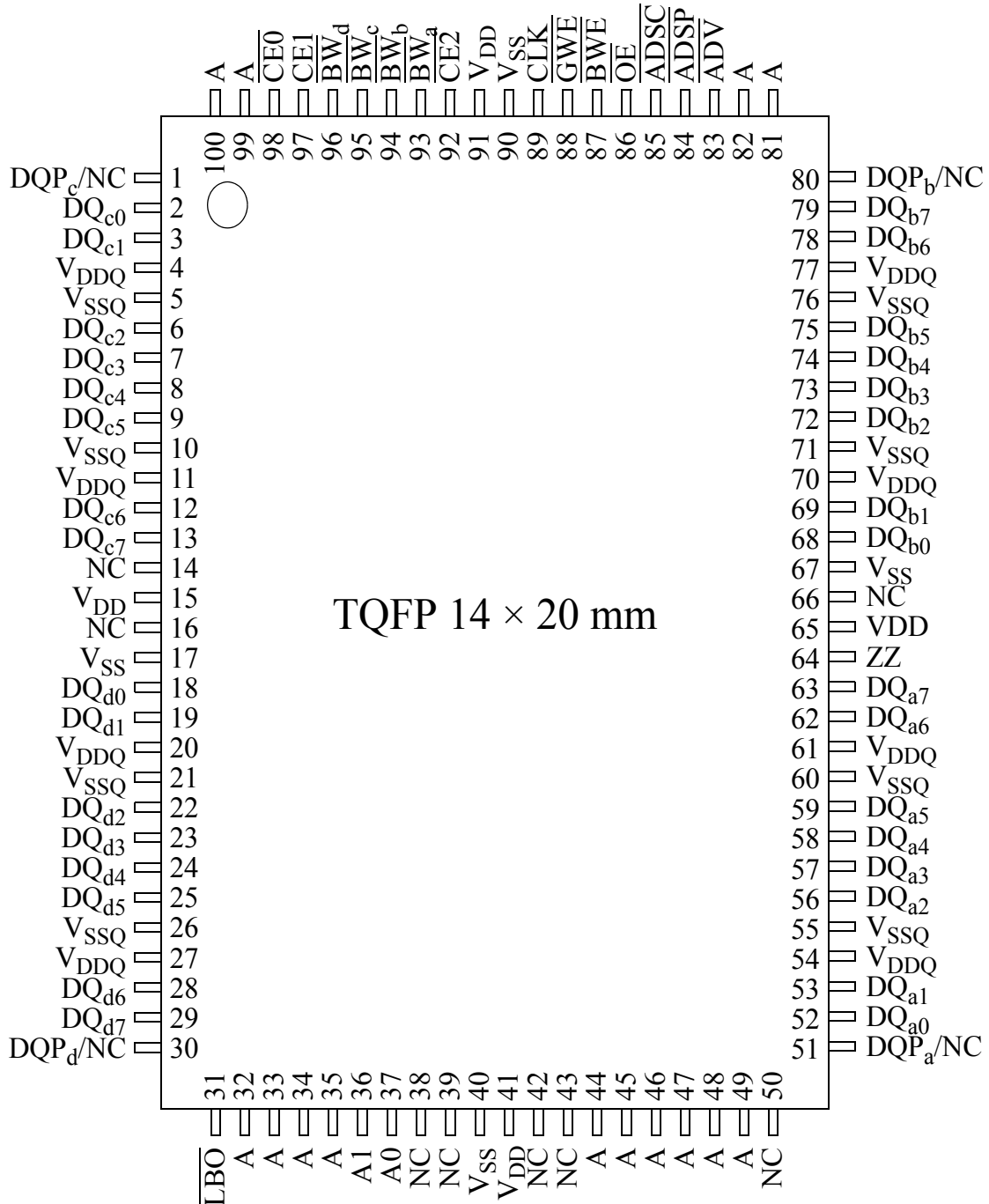
1 Core Power Supply: VDD = 3.3V ± 0.165V

2 I/O Supply Voltage: VDDQ = 3.3V ± 0.165V for 3.3V I/O  
VDDQ = 2.5V ± 0.125V for 2.5V I/O

- PL-SCD : Pipelined Burst Synchronous SRAM - Single Cycle Deselect
- PL-DCD : Pipelined Burst Synchronous SRAM - Double Cycle Deselect
- FT : Flow-through Burst Synchronous SRAM



Pin arrangement



Note: Pins 1,30,51,80 are NC for X32



## Functional description

The AS7C3364PFS32B and AS7C3364PFS36B are high-performance CMOS 2-Mbit synchronous Static Random Access Memory (SRAM) devices organized as 65,536 words × 32 or 36 bits, and incorporate a two-stage register-register pipeline for highest frequency on any given technology.

Timing for these devices is compatible with existing Pentium® synchronous cache specifications. This architecture is suited for ASIC, DSP and PowerPC™<sup>1</sup>-based systems in computing, datacom, instrumentation, and telecommunications systems.

Fast cycle times of 5.0/6.0/7.5 ns with clock access times ( $t_{CD}$ ) of 3.0/3.5/4.0 ns enable 200, 166 and 133 MHz bus frequencies. Three chip enable ( $\overline{CE}$ ) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ( $\overline{ADSC}$ ), or the processor address strobe ( $\overline{ADSP}$ ). The burst advance pin ( $\overline{ADV}$ ) allows subsequent internally generated burst addresses.

Read cycles are initiated with  $\overline{ADSP}$  (regardless of  $\overline{WE}$  and  $\overline{ADSC}$ ) using the new external address clocked into the on-chip address register when  $\overline{ADSP}$  is sampled Low, the chip enables are sampled active, and the output buffer is enabled with  $\overline{OE}$ . In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers and driven on the output pins on the next positive edge of CLK.  $\overline{ADV}$  is ignored on the clock edge that samples  $\overline{ADSP}$  asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when  $\overline{ADV}$  is sampled Low, and both address strobes are High. Burst mode is selectable with the  $\overline{LBO}$  input. With  $\overline{LBO}$  unconnected or driven High, burst operations use a Pentium® count sequence. With  $\overline{LBO}$  driven LOW, the device uses a linear count sequence suitable for PowerPC™ and many other applications.

Write cycles are performed by disabling the output buffers with  $\overline{OE}$  and asserting a write command. A global write enable  $\overline{GWE}$  writes all 32/36 bits regardless of the state of individual  $\overline{BW}[a:d]$  inputs. Alternately, when  $\overline{GWE}$  is High, one or more bytes may be written by asserting  $\overline{BWE}$  and the appropriate individual byte  $\overline{BWn}$  signal(s).

$\overline{BWn}$  is ignored on the clock edge that samples  $\overline{ADSP}$  Low, but is sampled on all subsequent clock edges. Output buffers are disabled when  $\overline{BWn}$  is sampled LOW (regardless of  $\overline{OE}$ ). Data is clocked into the data input register when  $\overline{BWn}$  is sampled Low. Address is incremented internally to the next burst address if  $\overline{BWn}$  and  $\overline{ADV}$  are sampled Low.

Read or write cycles may also be initiated with  $\overline{ADSC}$  instead of  $\overline{ADSP}$ . The differences between cycles initiated with  $\overline{ADSC}$  and  $\overline{ADSP}$  are as follows:

- $\overline{ADSP}$  must be sampled HIGH when  $\overline{ADSC}$  is sampled LOW to initiate a cycle with  $\overline{ADSC}$ .
- $\overline{WE}$  signals are sampled on the clock edge that samples  $\overline{ADSC}$  LOW (and  $\overline{ADSP}$  High).
- Master chip enable  $\overline{CE0}$  blocks  $\overline{ADSP}$ , but not  $\overline{ADSC}$ .

AS7C3364PFS32B and AS7C3364PFS36B family operates from a core 3.3V power supply. I/Os use a separate power supply that can operate at 2.5V or 3.3V. These devices are available in a 100-pin 14 × 20 mm TQFP package.

## TQFP capacitance

Parameter	Symbol	Test conditions	Min	Max	Unit
Input capacitance	$C_{IN}^*$	$V_{IN} = 0V$	-	5	pF
I/O capacitance	$C_{I/O}^*$	$V_{OUT} = 0V$	-	7	pF

\* Guaranteed not tested

## TQFP thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient) <sup>1</sup>	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1-layer	$\theta_{JA}$	40	°C/W
		4-layer	$\theta_{JA}$	22	°C/W
Thermal resistance (junction to top of case) <sup>1</sup>			$\theta_{JC}$	8	°C/W

<sup>1</sup> This parameter is sampled

<sup>1</sup> PowerPC™ is a trademark International Business Machines Corporation.



## Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ , $ZZ$ , $\overline{LBO}$ are synchronous to this clock.
A,A0,A1	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the Synchronous Truth Table for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active Low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE0}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe processor. Asserted LOW to load a new bus address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe controller. Asserted LOW to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted LOW to continue burst read/write.
$\overline{GWE}$	I	SYNC	Global write enable. Asserted LOW to write all 32/36 bits. When High, $\overline{BWE}$ and $\overline{BW[a:d]}$ control write enable.
$\overline{BWE}$	I	SYNC	Byte write enable. Asserted LOW with $\overline{GWE} = \text{HIGH}$ to enable effect of $\overline{BW[a:d]}$ inputs.
$\overline{BW[a,b,c,d]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE} = \text{HIGH}$ and $\overline{BWE} = \text{Low}$ . If any of $\overline{BW[a:d]}$ is active with $\overline{GWE} = \text{HIGH}$ and $\overline{BWE} = \text{LOW}$ the cycle is a write cycle. If all $\overline{BW[a:d]}$ are inactive the cycle is a read cycle.
$\overline{OE}$	I	ASYNCR	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is in read mode.
$\overline{LBO}$	I	STATIC	Selects Burst mode. When tied to $V_{DD}$ or left floating, device follows Interleaved Burst order. When driven Low, device follows linear Burst order. <i>This signal is internally pulled High.</i>
ZZ	I	ASYNCR	Snooze. Places device in low power mode; data is retained. Connect to GND if unused.
NC	-	-	No connect

## Snooze Mode

SNOOZE MODE is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of SNOOZE MODE is dictated by the length of time the  $ZZ$  is in a High state.

The  $ZZ$  pin is an asynchronous, active high input that causes the device to enter SNOOZE MODE.

When the  $ZZ$  pin becomes a logic High,  $I_{SB2}$  is guaranteed after the time  $t_{ZZ1}$  is met. After entering SNOOZE MODE, all inputs except  $ZZ$  is disabled and all outputs go to High-Z. Any operation pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during  $t_{PUS}$ , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SNOOZE MODE.



### Write enable truth table (per byte)

Function	$\overline{\text{GWE}}$	$\overline{\text{BWE}}$	$\overline{\text{BWa}}$	$\overline{\text{BWb}}$	$\overline{\text{BWc}}$	$\overline{\text{BWd}}$
Write All Bytes	L	X	X	X	X	X
	H	L	L	L	L	L
Write Byte a	H	L	L	H	H	H
Write Byte c and d	H	L	H	H	L	L
Read	H	H	X	X	X	X
	H	L	H	H	H	H

Key: X = don't care, L = low, H = high, n = a, b, c, d;  $\overline{\text{BWE}}$ ,  $\overline{\text{BWn}}$  = internal write signal.

### Asynchronous Truth Table

Operation	ZZ	$\overline{\text{OE}}$	I/O Status
Snooze mode	H	X	High-Z
Read	L	L	Dout
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care"
2. ZZ pin is pulled down internally
3. For write cycles that follows read cycles, the output buffers must be disabled with  $\overline{\text{OE}}$ , otherwise data bus contention will occur.
4. Snooze mode means power down state of which stand-by current does not depend on cycle times
5. Deselected means power down state of which stand-by current depends on cycle times

### Burst sequence table

Interleaved burst address ( $\overline{\text{LBO}} = 1$ )					Linear burst address ( $\overline{\text{LBO}} = 0$ )				
	A1 A0	A1 A0	A1 A0	A1 A0		A1 A0	A1 A0	A1 A0	A1 A0
1 <sup>st</sup> Address	0 0	0 1	1 0	1 1	1 <sup>st</sup> Address	0 0	0 1	1 0	1 1
2 <sup>nd</sup> Address	0 1	0 0	1 1	1 0	2 <sup>nd</sup> Address	0 1	1 0	1 1	0 0
3 <sup>rd</sup> Address	1 0	1 1	0 0	0 1	3 <sup>rd</sup> Address	1 0	1 1	0 0	0 1
4 <sup>th</sup> Address	1 1	1 0	0 1	0 0	4 <sup>th</sup> Address	1 1	1 0	0 1	1 0



Synchronous truth table<sup>[4]</sup>

$\overline{CE0}^1$	CE1	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}^{[2]}$	$\overline{OE}$	Address accessed	CLK	Operation	DQ
H	X	X	X	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	L	X	L	X	X	X	X	NA	L to H	Deselect	Hi-Z
L	L	X	H	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	X	H	L	X	X	X	X	NA	L to H	Deselect	Hi-Z
L	X	H	H	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	H	L	L	X	X	X	L	External	L to H	Begin read	Q
L	H	L	L	X	X	X	H	External	L to H	Begin read	Hi-Z
L	H	L	H	L	X	H	L	External	L to H	Begin read	Q
L	H	L	H	L	X	H	H	External	L to H	Begin read	Hi-Z
X	X	X	H	H	L	H	L	Next	L to H	Continue read	Q
X	X	X	H	H	L	H	H	Next	L to H	Continue read	Hi-Z
X	X	X	H	H	H	H	L	Current	L to H	Suspend read	Q
X	X	X	H	H	H	H	H	Current	L to H	Suspend read	Hi-Z
H	X	X	X	H	L	H	L	Next	L to H	Continue read	Q
H	X	X	X	H	L	H	H	Next	L to H	Continue read	Hi-Z
H	X	X	X	H	H	H	L	Current	L to H	Suspend read	Q
H	X	X	X	H	H	H	H	Current	L to H	Suspend read	Hi-Z
L	H	L	H	L	X	L	X	External	L to H	Begin write	D <sup>3</sup>
X	X	X	H	H	L	L	X	Next	L to H	Continue write	D
H	X	X	X	H	L	L	X	Next	L to H	Continue write	D
X	X	X	H	H	H	L	X	Current	L to H	Suspend write	D
H	X	X	X	H	H	L	X	Current	L to H	Suspend write	D

1 X = don't care, L = low, H = high

2 For  $\overline{WRITE}$ , L means any one or more byte write enable signals ( $\overline{BWA}$ ,  $\overline{BWb}$ ,  $\overline{BWC}$  or  $\overline{BWD}$ ) and  $\overline{BWE}$  are LOW or  $\overline{GWE}$  is LOW.  $\overline{WRITE}$  = HIGH for all  $\overline{BWx}$ ,  $\overline{BWE}$ ,  $\overline{GWE}$  HIGH. See "Write enable truth table (per byte)," on page 6 for more information.

3 For write operation following a READ,  $\overline{OE}$  must be high before the input data set up time and held high throughout the input hold time

4 ZZ pin is always Low.



### Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	$V_{DD}, V_{DDQ}$	-0.5	+4.6	V
Input voltage relative to GND (input pins)	$V_{IN}$	-0.5	$V_{DD} + 0.5$	V
Input voltage relative to GND (I/O pins)	$V_{IN}$	-0.5	$V_{DDQ} + 0.5$	V
Power dissipation	$P_d$	-	1.8	W
Short circuit output current	$I_{OUT}$	-	20	mA
Storage temperature	$T_{stg}$	-65	+150	°C
Temperature under bias	$T_{bias}$	-65	+135	°C

Stresses greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

### Recommended operating conditions at 3.3V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	$V_{DD}$	3.135	3.3	3.465	V
Supply voltage for I/O	$V_{DDQ}$	3.135	3.3	3.465	V
Ground supply	$V_{SS}$	0	0	0	V

### Recommended operating conditions at 2.5V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	$V_{DD}$	3.135	3.3	3.465	V
Supply voltage for I/O	$V_{DDQ}$	2.375	2.5	2.625	V
Ground supply	$V_{SS}$	0	0	0	V





### DC electrical characteristics for 3.3V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current <sup>†</sup>	I <sub>LI</sub>	V <sub>DD</sub> = Max, 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-2	2	μA
Output leakage current	I <sub>LO</sub>	OE ≥ V <sub>IH</sub> , V <sub>DD</sub> = Max, 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>	-2	2	μA
Input high (logic 1) voltage	V <sub>IH</sub>	Address and control pins	2*	V <sub>DD</sub> +0.3	V
		I/O pins	2*	V <sub>DDQ</sub> +0.3	
Input low (logic 0) voltage	V <sub>IL</sub>	Address and control pins	-0.3**	0.8	V
		I/O pins	-0.5**	0.8	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA, V <sub>DDQ</sub> = 3.135V	2.4	-	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA, V <sub>DDQ</sub> = 3.465V	-	0.4	V

### DC electrical characteristics for 2.5V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current <sup>†</sup>	I <sub>LI</sub>	V <sub>DD</sub> = Max, 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-2	2	μA
Output leakage current	I <sub>LO</sub>	OE ≥ V <sub>IH</sub> , V <sub>DD</sub> = Max, 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>	-2	2	μA
Input high (logic 1) voltage	V <sub>IH</sub>	Address and control pins	1.7*	V <sub>DD</sub> +0.3	V
		I/O pins	1.7*	V <sub>DDQ</sub> +0.3	V
Input low (logic 0) voltage	V <sub>IL</sub>	Address and control pins	-0.3**	0.7	V
		I/O pins	-0.3**	0.7	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA, V <sub>DDQ</sub> = 2.375V	1.7	-	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA, V <sub>DDQ</sub> = 2.625V	-	0.7	V

<sup>†</sup> LBO and ZZ pins have an internal pull-up or pull-down, and input leakage = ±10 μA.

\*V<sub>IH</sub> max < V<sub>DD</sub> + 1.5V for pulse width less than 0.2 X t<sub>CYC</sub>

\*\*V<sub>IL</sub> min = -1.5 for pulse width less than 0.2 X t<sub>CYC</sub>

### I<sub>DD</sub> operating conditions and maximum limits

Parameter	Sym	Conditions	-200	-166	-133	Unit
Operating power supply current <sup>1</sup>	I <sub>CC</sub>	$\overline{CE0} \leq V_{IL}$ , CE1 ≥ V <sub>IH</sub> , $\overline{CE2} \leq V_{IL}$ , f = f <sub>Max</sub> , I <sub>OUT</sub> = 0 mA, ZZ ≤ V <sub>IL</sub>	375	350	325	mA
Standby power supply current	I <sub>SB</sub>	All V <sub>IN</sub> ≤ 0.2V or ≥ V <sub>DD</sub> - 0.2V, Deselected, f = f <sub>Max</sub> , ZZ ≤ V <sub>IL</sub>	130	100	90	mA
	I <sub>SB1</sub>	Deselected, f = 0, ZZ ≤ 0.2V, all V <sub>IN</sub> ≤ 0.2V or ≥ V <sub>DD</sub> - 0.2V	30	30	30	
	I <sub>SB2</sub>	Deselected, f = f <sub>Max</sub> , ZZ ≥ V <sub>DD</sub> - 0.2V, all V <sub>IN</sub> ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub>	30	30	30	

<sup>1</sup> I<sub>CC</sub> given with no output loading. I<sub>CC</sub> increases with faster cycle times and greater output loading.



### Timing characteristics over operating range

Parameter	Sym	-200		-166		-133		Unit	Notes <sup>1</sup>
		Min	Max	Min	Max	Min	Max		
Clock frequency	$f_{Max}$	–	200	–	166	–	133	MHz	
Cycle time	$t_{CYC}$	5	–	6	–	7.5	–	ns	
Clock access time	$t_{CD}$	–	3.0	–	3.5	–	4.0	ns	
Output enable LOW to data valid	$t_{OE}$	–	3.0	–	3.5	–	4.0	ns	
Clock HIGH to output Low Z	$t_{LZC}$	0	–	0	–	0	–	ns	2,3,4
Data output invalid from clock HIGH	$t_{OH}$	1.5	–	1.5	–	1.5	–	ns	2
Output enable LOW to output Low Z	$t_{LZOE}$	0	–	0	–	0	–	ns	2,3,4
Output enable HIGH to output High Z	$t_{HZOE}$	–	3.0	–	3.5	–	4.0	ns	2,3,4
Clock HIGH to output High Z	$t_{HZC}$	–	3.0	–	3.5	–	4.0	ns	2,3,4
Output enable HIGH to invalid output	$t_{OHOE}$	0	–	0	–	0	–	ns	
Clock HIGH pulse width	$t_{CH}$	2.0	–	2.4	–	2.5	–	ns	5
Clock LOW pulse width	$t_{CL}$	2.3	–	2.4	–	2.5	–	ns	5
Address setup to clock HIGH	$t_{AS}$	1.4	–	1.5	–	1.5	–	ns	6
Data setup to clock HIGH	$t_{DS}$	1.4	–	1.5	–	1.5	–	ns	6
Write setup to clock HIGH	$t_{WS}$	1.4	–	1.5	–	1.5	–	ns	6,7
Chip select setup to clock HIGH	$t_{CSS}$	1.4	–	1.5	–	1.5	–	ns	6,8
Address hold from clock HIGH	$t_{AH}$	0.4	–	0.5	–	0.5	–	ns	6
Data hold from clock HIGH	$t_{DH}$	0.4	–	0.5	–	0.5	–	ns	6
Write hold from clock HIGH	$t_{WH}$	0.4	–	0.5	–	0.5	–	ns	6,7
Chip select hold from clock HIGH	$t_{CSH}$	0.4	–	0.5	–	0.5	–	ns	6,8
$\overline{ADV}$ setup to clock HIGH	$t_{ADVS}$	1.4	–	1.5	–	1.5	–	ns	6
$\overline{ADSP}$ setup to clock HIGH	$t_{ADSPS}$	1.4	–	1.5	–	1.5	–	ns	6
$\overline{ADSC}$ setup to clock HIGH	$t_{ADSCS}$	1.4	–	1.5	–	1.5	–	ns	6
$\overline{ADV}$ hold from clock HIGH	$t_{ADVH}$	0.4	–	0.5	–	0.5	–	ns	6
$\overline{ADSP}$ hold from clock HIGH	$t_{ADSPH}$	0.4	–	0.5	–	0.5	–	ns	6
$\overline{ADSC}$ hold from clock HIGH	$t_{ADSCH}$	0.4	–	0.5	–	0.5	–	ns	6

<sup>1</sup> See “Notes” on page 16.

### Snooze Mode Electrical Characteristics

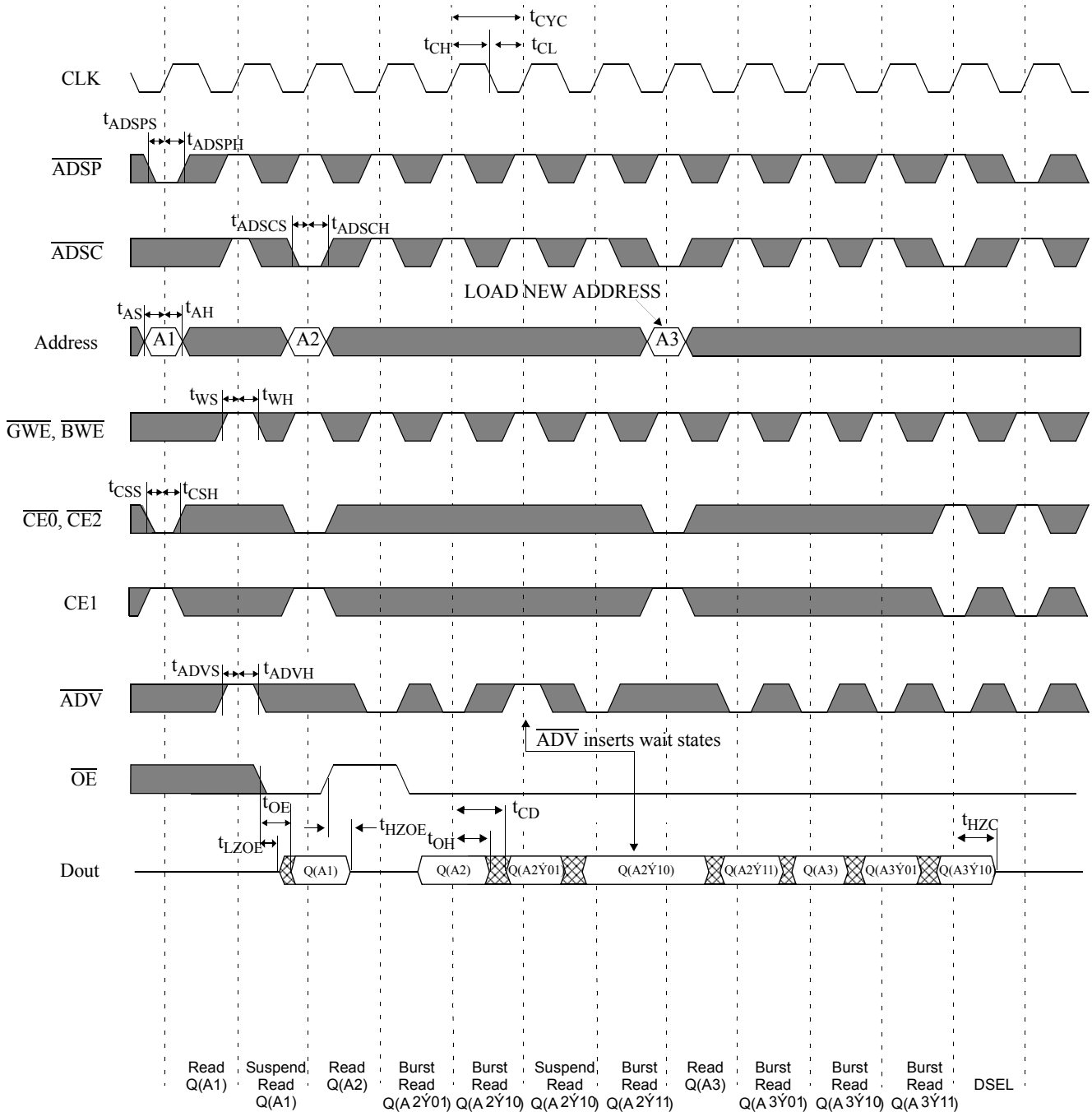
Description	Conditions	Symbol	Min	Max	Units
Current during Snooze Mode	$ZZ \geq V_{IH}$	$I_{SB2}$		30	mA
ZZ active to input ignored		$t_{PDS}$	2		cycle
ZZ inactive to input sampled		$t_{PUS}$	2		cycle
ZZ active to SNOOZE current		$t_{ZZI}$		2	cycle
ZZ inactive to exit SNOOZE current		$t_{RZZI}$	0		



Key to switching waveforms

Rising input   
 Falling input   
 don't care   
 Undefined

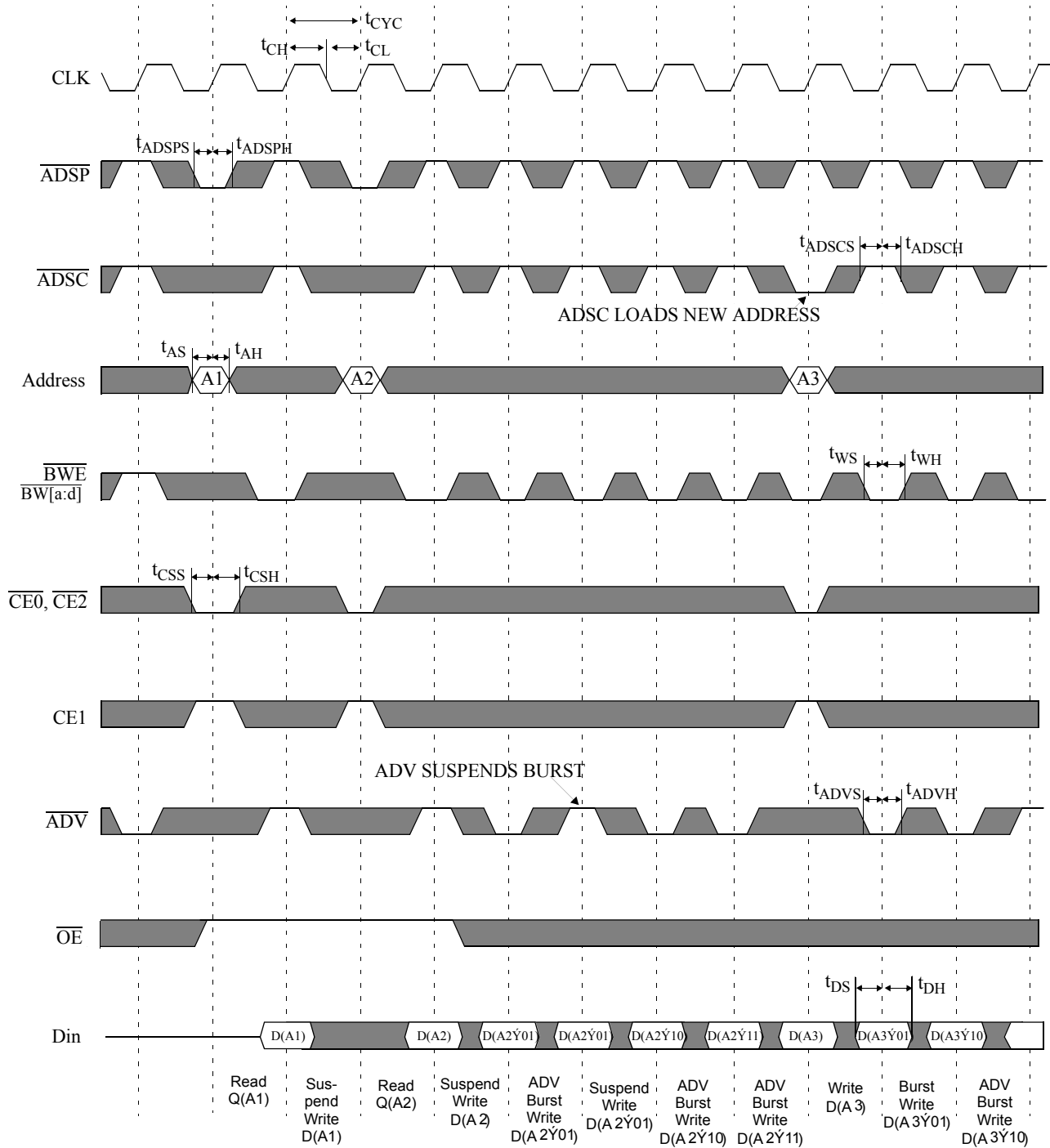
Timing waveform of read cycle



Note:  $\dot{Y}$  = XOR when  $\overline{LB0}$  = high/no connect;  $\dot{Y}$  = ADD when  $\overline{LB0}$  = low.  $\overline{BW}[a:d]$  is don't care.



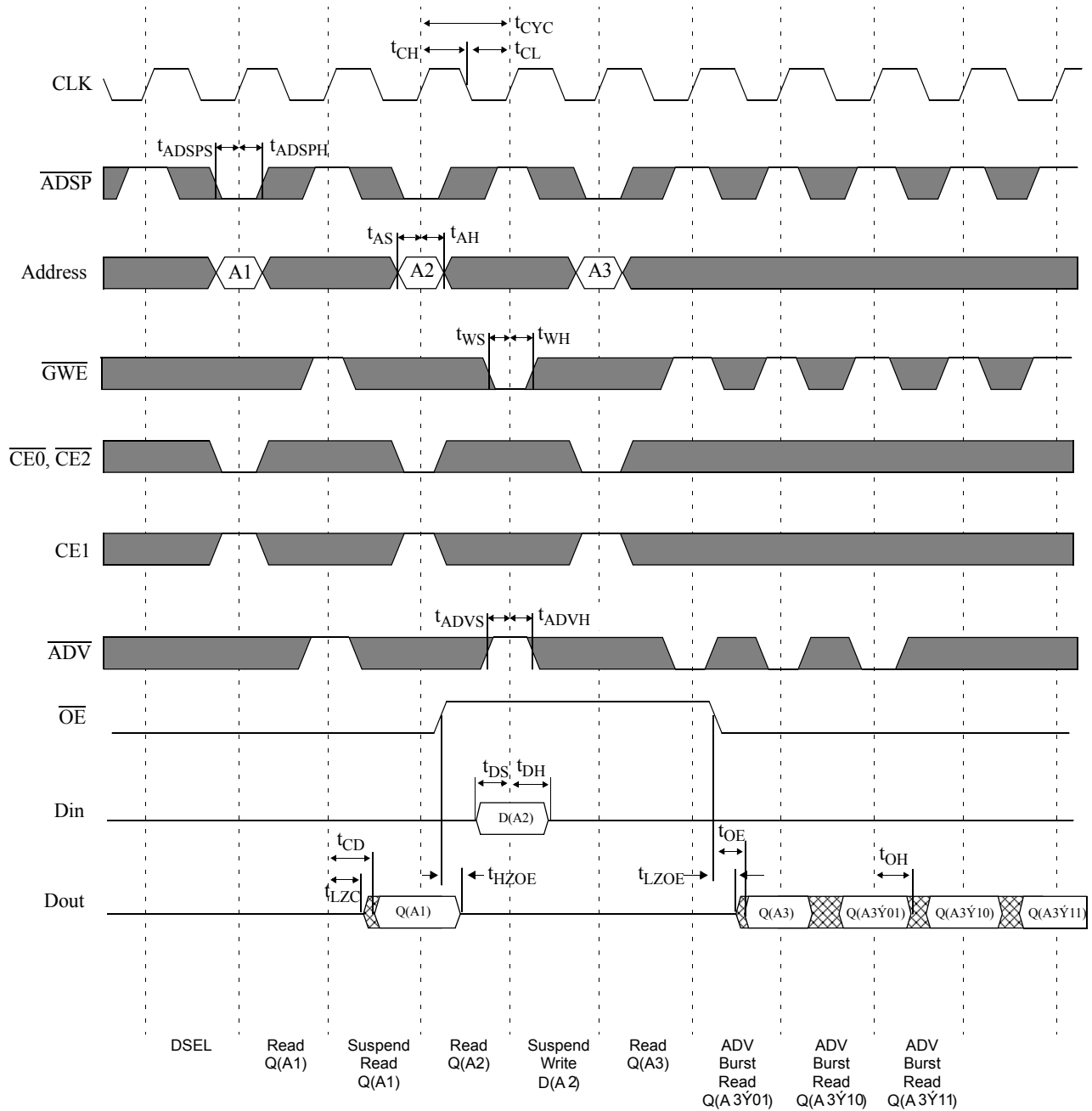
Timing waveform of write cycle



Note:  $\dot{Y}$  = XOR when  $\overline{LBO}$  = high/no connect;  $\dot{Y}$  = ADD when  $\overline{LBO}$  = low.



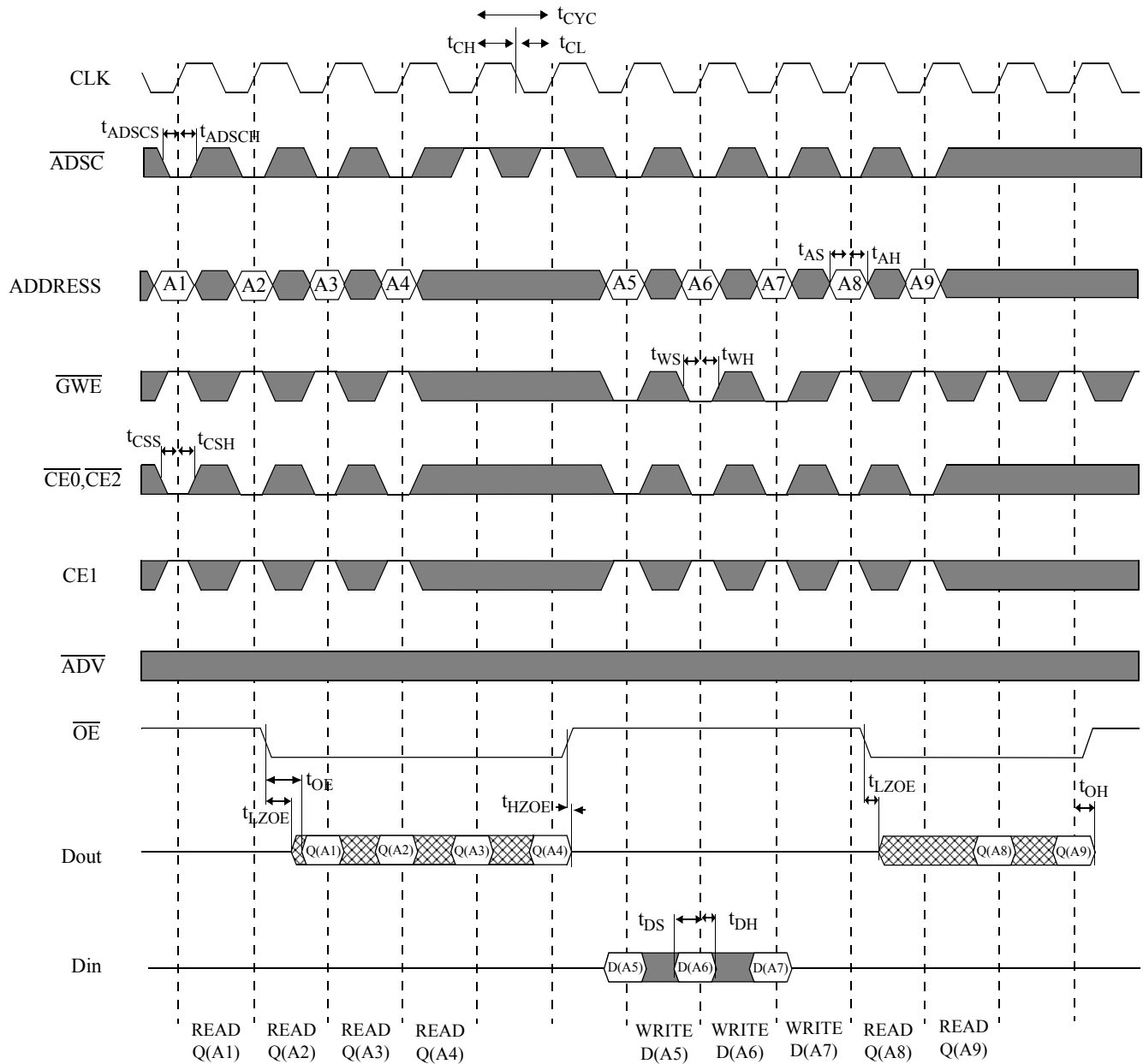
Timing waveform of read/write cycle (ADSP Controlled; ADSC High)



Note:  $\dot{Y}$  = XOR when  $\overline{LB0}$  = high/no connect;  $\dot{Y}$  = ADD when  $\overline{LB0}$  = low.

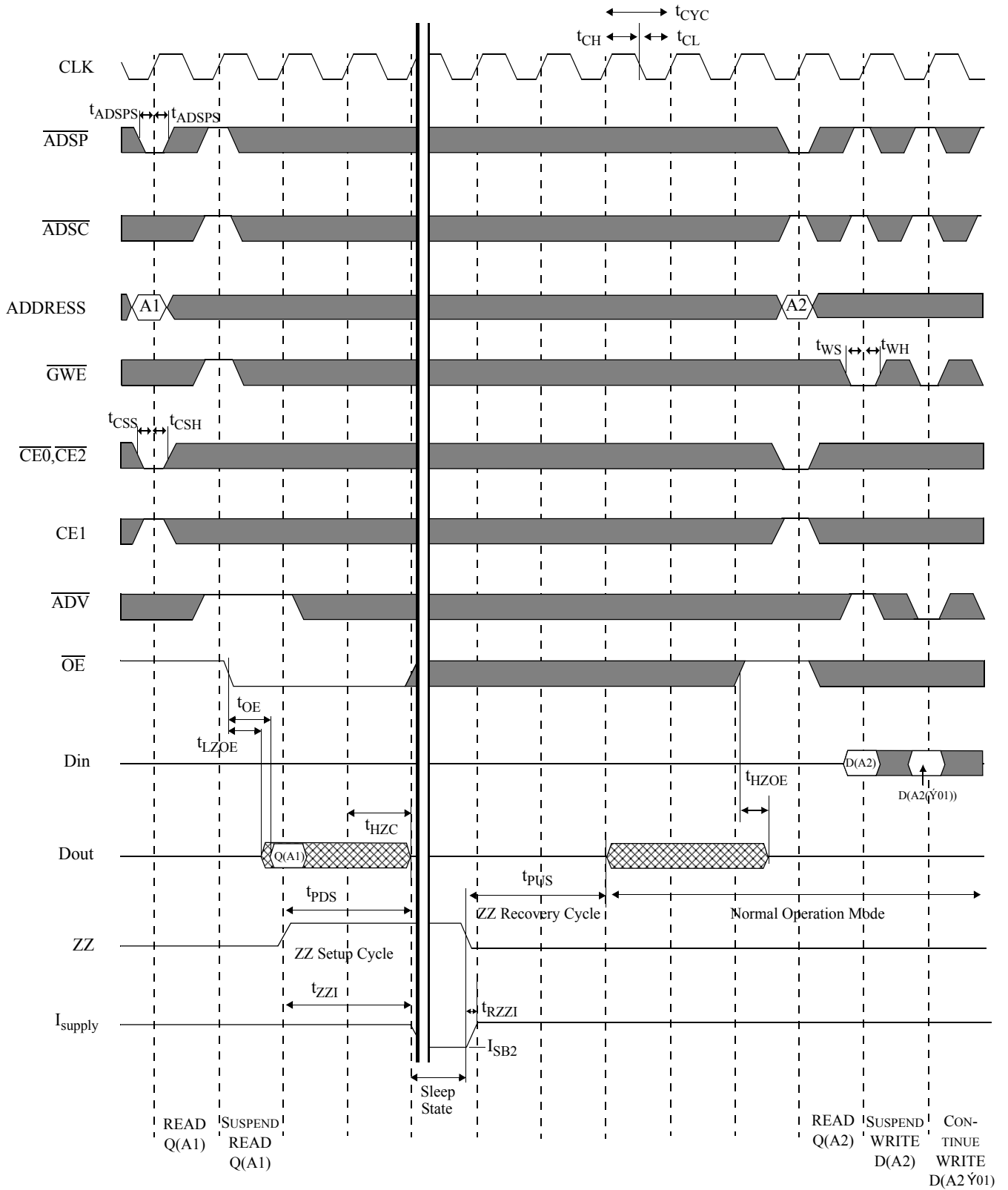


Timing waveform of read/write cycle ( $\overline{\text{ADSC}}$  controlled,  $\overline{\text{ADSP}} = \text{HIGH}$ )





Timing waveform of power down cycle





## AC test conditions

- Output load: see Figure B, except for  $t_{LZC}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ ,  $t_{HZC}$ , see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

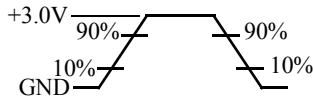


Figure A: Input waveform

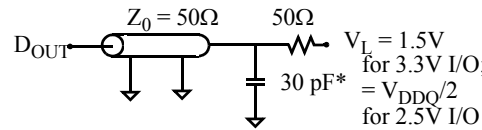


Figure B: Output load (A)

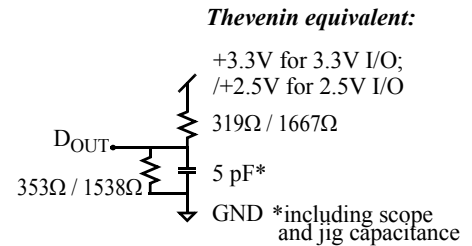


Figure C: Output load (B)

### Notes

- 1 For test conditions, see *AC Test Conditions*, Figures A, B, C.
- 2 This parameter measured with output load condition in Figure C.
- 3 This parameter is sampled, but not 100% tested.
- 4  $t_{HZOE}$  is less than  $t_{LZOE}$ ; and  $t_{HZC}$  is less than  $t_{LZC}$  at any given temperature and voltage.
- 5  $t_{CH}$  measured as HIGH above  $V_{IH}$  and  $t_{CL}$  measured as LOW below  $V_{IL}$ .
- 6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
- 7 Write refers to  $\overline{GWE}$ ,  $\overline{BWE}$ ,  $\overline{BW[a:d]}$ .
- 8 Chip select refers to  $\overline{CE0}$ ,  $CE1$ ,  $\overline{CE2}$ .

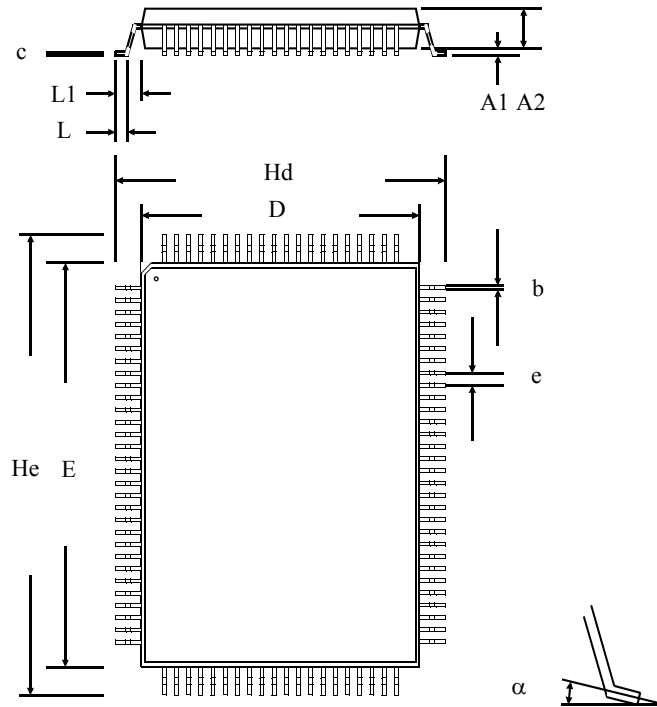




**Package Dimensions**

**100-pin quad flat pack (TQFP)**

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.85	16.15
He	21.80	22.20
L	0.45	0.75
L1	1.00 nominal	
$\alpha$	0°	7°
Dimensions in millimeters		





**Ordering information**

Package	Width	-200	-166	-133
TQFP	x32	AS7C3364PFS32B-200TQC	AS7C3364PFS32B-166TQC	AS7C3364PFS32B-133TQC
TQFP	x32	AS7C3364PFS32B-200TQI	AS7C3364PFS32B-166TQI	AS7C3364PFS32B-133TQI
TQFP	x36	AS7C3364PFS36B-200TQC	AS7C3364PFS36B-166TQC	AS7C3364PFS36B-133TQC
TQFP	x36	AS7C3364PFS36B-200TQI	AS7C3364PFS36B-166TQI	AS7C3364PFS36B-133TQI

Note

Add suffix 'N' to the above part number for lead free parts (Ex AS7C3364PFS32B-166TQCN)

**Part numbering guide**

AS7C	33	64	PF	S	32/36	B	-XXX	TQ	C/I	X
1	2	3	4	5	6	7	8	9	10	11

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 33 = 3.3V
3. Organization: 64 = 64K
4. Pipeline mode
5. Deselect: S = Single cycle deselect
6. Organization: 32 = x32; 36 = x36
7. Production version: B = Product revision
8. Clock speed (MHz)
9. Package type: TQ = TQFP
10. Operating temperature: C=Commercial (0° C to 70° C); I=Industrial (-40° C to 85° C)
11. N=Lead Free Part



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