

Data Sheet

### **Description**

The AS91L1006BU is a one to 6-port JTAG gateway. It partitions a single JTAG chain into six separate chains. These separate chains can be optionally configured to operate as a single chain.

The AS91L1006BU device is used to provide enhanced capabilities to the standard IEEE1149.1. It enables the IEEE1149.1 interface to be used in a true Multi-Drop environment without any additional signals. This Multi-Drop capability enables the standard IEEE1149.1 interface to be used not just for stand alone PCB (Printed Circuit Board) testing, but also for complete system testing including all PCBs within a system back plane environment.

The AS91L1006BU provides the capability of partitioning the PCB, into multiple smaller IEEE1149.1 scan chains totally under software control. Partitioning the IEEE1149.1 chains on the PCB has several benefits which include easier fault diagnostics capabilities as a fault on one of the IEEE1149.1 Local Scan Ports (LSPs) does not render the PCB untestable, faster flash programming on the PCBs, and removal of IEEE1149.1 signal loading issues.

All of the protocols required for addressing the AS91L1006BU device via the Multi-Drop capability and the protocols for configuring which of the six IEEE1149.1 LSPs on the AS91L1006BU are to be used, is handled via 3<sup>rd</sup> party ATPG tools from vendors like Asset-Intertech and JTAG Technologies. In a Multi-Drop environment it is also possible to perform interconnect tests between multiple PCBs within a system thus extending the interconnect tests to the back plane itself.

#### **Key Features**

- Device Multi-Drop addressable via the IEEE 1149.1 protocol
- Support for 6 local scan chains addressable via the IEEE 1149.1 interface
- Support for Pass-Through™
- Support for the IEEE 1149.1 USERCODE instruction
- Support for Status instruction enabling nonintrusive monitoring of the system card
- Local Scan Port (LSP) enable signal provides the ability to use non IEEE 1149.1 compliant devices that require JTAG enable signal

- Provides the ability to initiate Self-Test on a remote PCB via a standard IEEE 1149.1 command
- Support for JTAG Technologies AutoWR™ feature
- Pinout and feature set compatible (complete second source) with the Firecron JTS06BU device
- Available in a 100-pin LQFP or a 100-pin FPBGA lead free package

### **Device Block Diagram**



Figure 1 - AS91L1006BU Device Block Diagram



### AS91L1006BU Gateway Functional Description

The basic structure of the AS91L1006BU device is shown in Figure-1. The core of the device is the 16-state IEEE1149.1 TAP controller state machine. All accesses to the internal registers of the AS91L1006BU device are controlled via this state machine during normal operation as per the IEEE1149.1 standard. The address selection logic enables the AS91L1006BU to operate in a Multi-Drop environment within system backplane.

The address selection logic compares the scanned address to the slot address value presented on the I/O of the AS91L1006BU device. The LSP park/unpark logic provides control through instructions scanned in under the IEEE1149.1 protocol, to select, which LSP will be placed into the active, scan chain. The passthrough and LSP connection logic selects the signal paths for the LSP IEEE1149.1 signals. The

device also supports a Pass-Through mode which enables the primary IEEE1149.1 signals to be routed to any of the LSPs. This signal routing is selectable via I/O pins on the AS91L1006BU device.

Figure-2 shows the device selection state machine. The AS91L1006BU will perform an address compare on the slot address presented at its I/O and the value scanned in via the IEEE1149.1. If the value matches then the AS91L1006BU becomes selected and is ready for normal access via IEEE1149.1 commands. If the address does not match then the device will proceed to the unselected mode, where it will remain until the AS91L1006BU is issued a GOTOWAIT instruction or a reset occurs via TRST or the LSP RESET pin.



**Selection Logic State machine** 

Park/Unpark State Machine

The LSP Park/Unpark State Machine controls the insertion of the LSPs into the current active scan chain. The ability to park the LSP in certain IEEE1149.1 states, enable the AS91L1006BU to perform several functions including backplane interconnect testing and IC BIST.

#### AS91L1006BU Detailed Mode of Operation

#### Addressing the AS91L1006BU device

After a Test-Logic-Reset or power-up, the AS91L1006BU device will be in its Wait-for-Selection state with its TDO pin tri-stated, thus avoiding contention in a Multi-Drop environment. The AS91L1006BU device will respond to a device-select sequence for a particular address that is auto generated by third party test tools with respect to the address that is pre-loaded on its S(5..0). Once this sequence has been completed, the AS91L1006BU device will respond to normal IEEE 1149.1 instructions. Note that addresses 60-63 have been reserved and the AS91L1006BU device will not respond if the user selects these addresses.

The AS91L1006BU device should be in the Wait-for-Selection mode, which can be entered into by issuing an asynchronous reset (through the deassertion of TRST) or by issuing a synchronous reset (through the assertion of TMS for five cycles of TCK). After the device has been selected, it can be issued a GOTOWAIT instruction.

The internal IEEE1149.1 state machine of the AS91L1006BU device is taken to the Shift-IR phase and the required Device-ID is shifted into the Instruction register. As the IEEE1149.1 state machine passes through the Update-IR phase, the address is matched to the value on the S(5-0) pins on the AS91L1006BU device; if the values match, then the AS91L1006BU device is selected and is ready to receive any normal IEEE1149.1 command.

| S(5-0) value              | IR (7 – 0) value |
|---------------------------|------------------|
| < 3A hex or 60<br>decimal | XXVVVVV          |

Table 1 - AS91L1006BU

**Device Selection Table** 

# Table 2 - AS91L1006BU Multi Cast Group Selection Table

| Selection<br>Mode         | Binary<br>Address       | Function  |
|---------------------------|-------------------------|---|
| Single<br>Address<br>Mode | XX000000 to<br>XX111010 | Single AS91L1006BU<br>selected the TDO of<br>the device will be<br>active   |
| Broad<br>Cast Mode        | XX111011                | All accessible<br>AS91L1006BU<br>devices are selected<br>for operation. TDO on<br>all devices will be in<br>HighZ |
| Multi-Cast<br>Group 0     | XX111100                | Access all<br>AS91L1006BU<br>devices that have<br>been placed in GRP0<br>by their MCGR<br>contents                |
| Multi-Cast<br>Group 1     | XX111101                | Access all<br>AS91L1006BU<br>devices that have<br>been placed in GRP1<br>by their MCGR<br>contents                |
| Multi-Cast<br>Group 2     | XX111110                | Access all<br>AS91L1006BU<br>devices that have<br>been placed in GRP2<br>by their MCGR<br>contents                |
| Multi-Cast<br>Group 3     | XX111111                | Access all<br>AS91L1006BU<br>devices that have<br>been placed in GRP3<br>by their MCGR<br>contents                |

#### Table 3 - AS91L1006BU Device Register Description

| Register<br>Name                     | Description  |
|--------------------------------------|--|
| Instruction<br>Register              | AS91L1006BU device<br>addressing and instruction-<br>decode<br>IEEE Std. 1149.1 required<br>register |
| Boundary-<br>Scan<br>Register        | IEEE Std. 1149.1 required register   |
| Bypass<br>Register                   | IEEE Std. 1149.1 required register   |
| Device<br>Identification<br>Register | IEEE Std. 1149.1 optional<br>register  |
| User Code<br>Register                | IEEE Std. 1149.1 optional<br>register  |
| Status<br>Register                   | AS91L1006BU device non<br>intrusive 8-bit register pre load<br>able from the I/O pins                |
| Self Test<br>Register                | AS91L1006BU device specific<br>single bit register for initiating<br>self testing on a PCB           |
| Mode<br>Register                     | AS91L1006BU device local-port<br>configuration and control bits                                      |
| Auto Write<br>Register               | AS91L1006BU device Auto<br>Write feature enable register   |
| LSP Async<br>Reset<br>Register       | AS91L1006BU device Async<br>reset register for the LSPs  |

| Instructions    | Hex Op-<br>Code | Binary Op-<br>Code | Data Register   |
|-----------------|-----------------|--------------------|---|
| BYPASS          | FF              | 11111111           | Bypass Register   |
| EXTEST          | 00              | 00000000           | Boundary-Scan Register  |
| SAMPLE/PRELOAD  | 81              | 10000001           | Boundary-Scan Register  |
| IDCODE          | AA              | 10101010           | Device Identification Register  |
| UNPARK          | E7              | 11100111           | Device Identification Register  |
| PARKTLR         | C5              | 11000101           | Device Identification Register  |
| PARKRTI         | 84              | 10000100           | Device Identification Register  |
| PARKPAUSE       | C6              | 11000110           | Device Identification Register  |
| GOTOWAIT*       | C3              | 11000011           | Device Identification Register  |
| MODESELECT      | 8E              | 10001110           | Mode Register   |
| MCGRSELECT      | 03              | 00000011           | Multi-Cast Group Register.  |
| SOFTRESET       | 88              | 10001000           | Device Identification Register  |
| USERCODE        | 97              | 10010111           | User Programmable 32 Bit Identification Register                          |
| AUTOWR          | 98              | 10011000           | Auto Write Feature Enable Register  |
| STEST_PCB       | 99              | 10011001           | Single bit low pulse, used to initiate function on PCB<br>(SELF_TEST pin) |
| STATUS_BYTE     | 9A              | 10011010           | User programmable status byte (USER_STATUS_DATA pins)                     |
| LSP_ASYNC_RESET | 9B              | 10011011           | Toggles LSP TRST while maintaining the AS91L1006BU in the selected state. |
| Other Undefined | TBD             | TBD                | Device Identification Register  |

Table 4 - AS91L1006BU Device Instruction Register OpCodes

 ${
m cl}$  Note: All instructions act on a single selected AS91L1006BU device only.

\* This instruction causes the AS91L1006BU to become unselected and revert to the Wait-for-Selection state.

### AS91L1006BU device Register descriptions

#### **Bypass Register**

It is a mandatory single bit register that can be connected between PRIM\_TDI and PRIM\_TDO of the AS91L1006BU device.

#### **Multi-Cast Group Register**

This 2-bit data register enables the host system to place the AS91L1006BU into one of four distinct addressable groups.

| MCGR Register Bits<br>[10] | Binary Selection Address | MCGR GROUP |
|----------------------------|--------------------------|------------|
| 00                         | XX111100                 | GRP0       |
| 01                         | XX111101                 | GRP1       |
| 10                         | XX111110                 | GRP2       |
| 11                         | XX111111                 | GRP3       |

#### Table 5 - Multicast Group Register Mapping

Note: The MCGR is reset to 00 upon receiving TRST or the entering of the Test-Logic-Reset state.

#### **IDCODE Register**

It is an optional 32-bit register that can be connected between PRIM\_TDI and PRIM\_TDO of the AS91L1006BU device. The contents of the IDCODE register will be loaded with the following data when the AS91L1006BU enters Test-Logic-Reset or passes through Capture-IR:

"00000000000000001000001101101111"

Bits 0 to 11 indicate ALSC Jedec ID value of: "001101101111"

Bits 12 to 27 indicate the part number of the device: "000000000010000"

Bits 28 to 31 indicate the revision of the device: "0000"

#### **USERCODE Register**

The USERCODE is an 8-bit register that can be addressed via standard IEEE1149.1 commands, which are automatically generated by third party test tools. AS91L1006BU returns all zeroes if read from this registerUSERUSER and does have the ability to write into this register.

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\* The AS91L1006BU is a complete second source and pin for pin replacement of the Firecron JTS06BU device.

#### SELF\_TEST Register

The AS91L1006BU device supports a single output pin that can be controlled via the IEEE1149.1 interface. When the instruction is loaded into the AS91L1006BU instruction register, a single bit data register is connected which is always reset to logic zero when the TAP state machine enters Capture-DR. This will cause the SELF\_TEST pin to pulse low for one cycle of TCK, during the Update-DR phase. This low going pulse can be used to initiate self-tests on PCB's in a rack via the JTAG interface.

#### LSP\_ASYNC\_RST Register

The AS91L1006BU device supports async reset tests on the devices connected to the LSPs. The standard method of performing these tests by utilizing the primary TRST pin cannot be used as it will cause the AS91L1006BU to deselect and its internal registers to be reset. In order to enable async reset tests on LSPs, the test tool should instruct the device to toggle the LSP reset pins while maintaining the set up information in the AS91L1006BU. When the instruction is loaded into the AS91L1006BU instruction register, a single bit data register is connected as the data register which is always reset to logic zero when the TAP state machine enters Capture-DR. This will cause the LSP TRST pins to pulse low for one TCK cycle, during the Update-DR phase.

#### **AUTOWR Register**

This is a 6-bit register that controls the passthrough of the JTAG Technologies AutoWR<sup>™</sup> signal to any LSP. The register is reset to all zeros when entering the Test-Logic-Reset state.

# ☑ Note: The MCGR is reset to 00 upon receiving TRST or the entering of the Test-Logic-Reset state

| AutoWr<br>Register<br>(Bit 2 –<br>Bit 0) | LSP 3<br>AutoWr<br>Signal | LSP 2<br>AutoWr<br>Signal | LSP 1<br>AutoWr<br>Signal | AutoWr<br>Register<br>(Bit 5 – Bit<br>3) | LSP 6<br>AutoWr<br>Signal | LSP 5<br>AutoWr<br>Signal | LSP 4<br>AutoWr<br>Signal |
|--|---------------------------|---------------------------|---------------------------|--|---------------------------|---------------------------|---------------------------|
| 000                                      | High Z                    | High Z                    | High Z                    | 000                                      | High Z                    | High Z                    | High Z                    |
| 001                                      | High Z                    | High Z                    | Active                    | 001                                      | High Z                    | High Z                    | Active                    |
| 011                                      | High Z                    | Active                    | Active                    | 011                                      | High Z                    | Active                    | Active                    |
| 100                                      | Active                    | High Z                    | High Z                    | 100                                      | Active                    | High Z                    | High Z                    |
| 101                                      | Active                    | High Z                    | Active                    | 101                                      | Active                    | High Z                    | Active                    |
| 110                                      | Active                    | Active                    | High Z                    | 110                                      | Active                    | Active                    | High Z                    |
| 111                                      | Active                    | Active                    | Active                    | 111                                      | Active                    | Active                    | Active                    |

| Table 6 - | AUTOWR | Register | Mapping |
|-----------|--------|----------|---------|
|-----------|--------|----------|---------|

#### MODE\_SELECT Register

The Mode\_Select register allows the LSP of the AS91L1006BU to be connected in various different configurations. A LSP is selected for connection within the scan chain by the contents of the Mode\_Select register.

If the LSP is not parked in a stable state, i.e.: Pause-DR, Pause-IR, Run-Test-Idle or Test-Logic-Reset, it will be connected into the active scan chain. If all LSPs are parked in a stable state, then the AS91L1006BU will perform a bypass of the 6-LSP chain section. In this way if both sections are in the bypass mode then the AS91L1006BU is performing a loopback of TDI->Register->TDO to the host device.

| Mode_Select<br>Register (Bit 15<br>-> Bit 8) | LSP Configuration (If Port<br>Unparked)                           |  | Mode_Select<br>Register (Bit 7 -><br>Bit 0) | LSP Configuration (If Port<br>Unparked)                 |
|--|---|--|---|---|
| XXX0X000                                     | TDI ->Register->LSP_Data  |  | XXX0X000                                    | LSP_Data ->TDO  |
| XXX0X001                                     | TDI ->Register->LSP1->PAD-><br>LSP_Data                           |  | XXX0X001                                    | LSP_Data ->LSP4->PAD-<br>>TDO                           |
| XXX0X010                                     | TDI ->Register->LSP2->PAD-><br>LSP_Data                           |  | XXX0X010                                    | LSP_Data ->LSP5->PAD-<br>>TDO                           |
| XXX0X011                                     | TDI ->Register->LSP1->PAD-<br>>LSP2->PAD-> LSP_Data               |  | XXX0X011                                    | LSP_Data ->LSP4->PAD-<br>>LSP5->PAD->TDO                |
| XXX0X100                                     | TDI ->Register->LSP3->PAD-><br>LSP_Data                           |  | XXX0X100                                    | LSP_Data ->LSP6->PAD-<br>>TDO                           |
| XXX0X101                                     | TDI ->Register->LSP1->PAD-<br>>LSP3->PAD-> LSP_Data               |  | XXX0X101                                    | LSP_Data ->LSP4->PAD-<br>>LSP6->PAD->TDO                |
| XXX0X110                                     | TDI ->Register->LSP2->PAD-<br>>LSP3->PAD-> LSP_Data               |  | XXX0X110                                    | LSP_Data ->LSP5->PAD-<br>>LSP6->PAD->TDO                |
| XXX0X111                                     | TDI ->Register->LSP1->PAD-<br>>LSP2->PAD->LSP3->PAD-><br>LSP_Data |  | XXX0X111                                    | LSP_Data ->LSP4->PAD-<br>>LSP5->PAD->LSP6->PAD-<br>>TDO |

#### Table 7 - Mode Select Register Mapping

**X** = Don't care

**Register** = AS91L1006BU device instruction register or any of the AS91L1006BU device test data registers.

**PAD** = Insertion of a 1-bit register for data synchronization.

Upon entering Test-Logic-Reset, the register bits will be loaded with "0000000".



### Pass Through Support within the AS91L1006BU Device

The AS91L1006BU device supports a Pass-Through mode where the primary or master IEEE1149.1 JTAG signals can be routed to any one of the LSPs. When this mode is activated, the "Debug Enable" signal for that LSP will go active, which can be used to place a processor such as the MPC8260 into BDM (Background Debug mode), if required. If no processors are present in the LSP, the Pass-Through mode can be used to assist in the generation of the test vectors or memory tests for the devices that are linked into

the selected LSP. The pass-through feature has the effect of simplifying the test vector generation for the LSP, as it also has the effect of removing the AS91L1006BU device from the test vector generation process.

The pass-through mode can be used in FPGA or PLD programming applications, where a direct path between the primary and a specific LSP is desired.

| PASS_THRU_Enable | PASS_THRU_SEL(2) | PASS_THRU_SEL(1) | PASS_THRU_SEL(0) | Active LSP          |
|------------------|------------------|------------------|------------------|---------------------|
| High             | Х                | Х                | Х                | Normal<br>Operation |
| Low              | Low              | Low              | Low              | LSP1                |
| Low              | Low              | Low              | High             | LSP2                |
| Low              | Low              | High             | Low              | LSP3                |
| Low              | Low              | High             | High             | LSP4                |
| Low              | High             | Low              | Low              | LSP5                |
| Low              | High             | Low              | High             | LSP6                |

Table 8 - Pass through mode in AS91L1006BU

Note: When PASS\_THRU\_ENABLE is deasserted (logic "1"), then the LSPs are under control of the AS91L1006BU device logic.

# **Signal Description**

|           | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION  | Stable state after port/reset                            |
|-----------|-------------|-----------------------|------------------------|--|--|
| LSP1_TCK  | OUT         | 31                    | H4                     | IEEE1149.1 Test Clock on LSP 1<br>when PASS_THRU_ENABLE is<br>HIGH.  | Buffered version<br>of signal present<br>on primary TCK  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 000.<br>This pin is tri-stated for all other<br>combinations. |  |
| LSP1_TMS  | OUT         | 32                    | J4                     | IEEE1149.1 Test Mode Select on<br>LSP 1 when PASS_THRU_ENABLE<br>is HIGH.  | Logic '1'  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 000.<br>This pin is tri-stated for all other<br>combinations. |  |
| LSP1_TDO  | OUT         | 35                    | H5                     | IEEE1149.1 Test Data Out on LSP 1<br>when PASS_THRU_ENABLE is<br>HIGH.   | Logic '1'  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 000.<br>This pin is tri-stated for all other<br>combinations. |  |
| LSP1_TDI  | IN          | 33                    | K4                     | IEEE1149.1 Test Data In on LSP 1<br>when PASS_THRU_ENABLE is<br>HIGH.  |  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 000.  |  |
| LSP1_TRST | OUT         | 29                    | K3                     | IEEE1149.1 Test Reset on LSP 1<br>when PASS_THRU_ENABLE is<br>HIGH.  | Buffered version<br>of signal present<br>on primary TRST |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 000.  |  |

| PIN NAME    | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION   | Stable state<br>after port/reset                        |
|-------------|-------------|-----------------------|------------------------|---|---|
| LSP1_AutoWR | OUT         | 30                    | J3                     | Flash, Memory Auto-Write on LSP 1<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and  | Logic '1'   |
|             |             |                       |                        | PASS_THRU_SEL[2:0] = 000;<br>PRIM_AutoWR is routed to output.<br>This pin is tri-stated for all other<br>combinations.  |   |
| LSP1_DE     | OUT         | 28                    | J2                     | Pass-Through Debug Enable Output<br>on Local Scan Port 1.<br>Active low output when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 000.<br>This pin is high for all other<br>combinations.                                 | Logic '1'   |
| LSP2_TCK    | OUT         | 41                    | J6                     | IEEE1149.1 Test Clock on LSP 2<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001.<br>This pin is tri-stated for all other<br>combinations.       | Buffered version<br>of signal present<br>on primary TCK |
| LSP2_TMS    | OUT         | 42                    | H6                     | IEEE1149.1 Test Mode Select on<br>LSP 2 when PASS_THRU_ENABLE<br>is HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001.<br>This pin is tri-stated for all other<br>combinations. | Logic '1'   |
| LSP2_TDO    | OUT         | 45                    | J7                     | IEEE1149.1 Test Data Out on LSP 2<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001.<br>This pin is tri-stated for all other<br>combinations.    | Logic '1'   |

| PIN NAME    | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION  | Stable state<br>after port/reset                         |
|-------------|-------------|-----------------------|------------------------|--|--|
| LSP2_TDI    | IN          | 44                    | K7                     | IEEE1149.1 Test Data In on LSP 2<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001.   |  |
| LSP2_TRST   | OUT         | 37                    | K5                     | IEEE1149.1 Test Reset on LSP 2<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001.   | Buffered version<br>of signal present<br>on primary TRST |
| LSP2_AutoWR | OUT         | 40                    | K6                     | Flash, Memory Auto-Write on LSP 2<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001;<br>PRIM_AutoWR is routed to output.<br>This pin is tri-stated for all other<br>combinations. | Logic '1'  |
| LSP2_DE     | OUT         | 36                    | J5                     | PASS_THRU Debug Enable Output<br>on LSP 2.<br>Active low output when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 001.<br>This pin is high for all other<br>combinations.   | Logic '1'  |
| LSP3_TCK    | OUT         | 49                    | K9                     | IEEE1149.1 Test Clock on LSP 3<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010.<br>This pin is tri-stated for all other<br>combinations.  | Buffered version<br>of signal present<br>on primary TCK  |

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| PIN NAME            | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION  | Stable state<br>after port/reset                         |
|---------------------|-------------|-----------------------|------------------------|--|--|
| LSP3_TMS            | OUT         | 50                    | K10                    | IEEE1149.1 Test Mode Select on<br>LSP 3 when PASS_THRU_ENABLE<br>is HIGH.  | Logic '1'  |
|                     |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010.<br>This pin is tri-stated for all other<br>combinations.                                     |  |
| LSP3_TDO            | OUT         | 53                    | H10                    | IEEE1149.1 Test Data Out on LSP 3<br>when PASS_THRU_ENABLE is<br>HIGH.   | Logic '1'  |
|                     |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010.<br>This pin is tri-stated for all other<br>combinations.                                     |  |
| LSP3_TDI            | IN          | 52                    | J10                    | IEEE1149.1 Test Data In on LSP 3<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when  |  |
|                     |             |                       |                        | PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010.  |  |
| LSP3_TRST           | OUT         | 47                    | J8                     | IEEE1149.1 Test Reset on LSP 3<br>when PASS_THRU_ENABLE is<br>HIGH.  | Buffered version<br>of signal present<br>on primary TRST |
|                     |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010.  |  |
| LSP3_LSP_<br>AutoWR | OUT         | 48                    | K8                     | Flash, Memory Auto-Write on LSP 3<br>when PASS_THRU_ENABLE is<br>HIGH.   | Logic '1'  |
|                     |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010;<br>PRIM_AutoWR is routed to output.<br>This pin is tri-stated for all other<br>combinations. |  |

| PIN NAME  | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION  | Stable state after port/reset                            |
|-----------|-------------|-----------------------|------------------------|--|--|
| LSP3_DE   | OUT         | 46                    | H7                     | PASS_THRU Debug Enable Output<br>on LSP 3.<br>Active low output when   | Logic '1'  |
|           |             |                       |                        | PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 010.<br>This pin is high for all other<br>combinations.   |  |
| LSP4_TCK  | OUT         | 79                    | A8                     | IEEE1149.1 Test Clock on LSP 4<br>when PASS_THRU_ENABLE is<br>HIGH.  | Buffered version<br>of signal present<br>on primary TCK  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011.<br>This pin is tri-stated for all other<br>combinations. |  |
| LSP4_TMS  | OUT         | 78                    | A9                     | IEEE1149.1 Test Mode Select on<br>LSP 4 when PASS_THRU_ENABLE<br>is HIGH.  | Logic '1'  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011.<br>This pin is tri-stated for all other<br>combinations. |  |
| LSP4_TDO  | OUT         | 76                    | B10                    | IEEE1149.1 Test Data Out on LSP 4<br>when PASS_THRU_ENABLE is<br>HIGH.   | Logic '1'  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011.<br>This pin is tri-stated for all other<br>combinations. |  |
| LSP4_TDI  | IN          | 77                    | B9                     | IEEE1149.1 Test Data In on LSP 4<br>when PASS_THRU_ENABLE is<br>HIGH.  |  |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011.  |  |
| LSP4_TRST | OUT         | 81                    | Α7                     | IEEE1149.1 Test Reset on LSP 4<br>when PASS_THRU_ENABLE is<br>HIGH.  | Buffered version<br>of signal present<br>on primary TRST |
|           |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011.  |  |

| PIN NAME    | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION   | Stable state<br>after port/reset                        |
|-------------|-------------|-----------------------|------------------------|---|---|
| LSP4_AutoWR | OUT         | 80                    | B8                     | Flash, Memory Auto-Write on LSP 4<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011;<br>PRIM_AutoWR is routed to output.<br>This pin is tri-stated for all other | Logic '1'   |
|             |             |                       |                        | combinations.   |   |
| LSP4_DE     | OUT         | 83                    | Β7                     | PASS_THRU Debug Enable Output<br>on LSP 4.<br>Active low output when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 011.<br>This pin is high for all other<br>combinations.  | Logic '1'   |
| LSP5_TCK    | OUT         | 70                    | D10                    | IEEE1149.1 Test Clock on LSP 5<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 100.<br>This pin is tri-stated for all other<br>combinations.                       | Buffered version<br>of signal present<br>on primary TCK |
| LSP5_TMS    | OUT         | 69                    | D9                     | IEEE1149.1 Test Mode Select on<br>LSP 5 when PASS_THRU_ENABLE<br>is HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 100.<br>This pin is tri-stated for all other<br>combinations.                 | Logic '1'   |
| LSP5_TDO    | OUT         | 67                    | E8                     | IEEE1149.1 Test Data Out on LSP 5<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 100.<br>This pin is tri-stated for all other<br>combinations.                    | Logic '1'   |

| PIN NAME    | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION  | Stable state<br>after port/reset                        |
|-------------|-------------|-----------------------|------------------------|--|---|
| LSP5_TDI    | IN          | 68                    | E7                     | IEEE1149.1 Test Data In on LSP 5<br>when PASS_THRU_ENABLE is<br>HIGH.<br>Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and  |   |
|             |             | 70                    | <u></u>                | PASS_THRU_SEL[2:0] = 100.  | Duffered version  |
| LSP5_1RS1   | OUT         | 72                    | C9                     | when PASS_THRU_ENABLE is<br>HIGH.  | of signal present<br>of primary TRST                    |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 100.  |   |
| LSP5_AutoWR | OUT         | 71                    | D8                     | Flash, Memory Auto-Write on LSP 5<br>when PASS_THRU_ENABLE is<br>HIGH.   | Logic '1'   |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 100;<br>PRIM_AutoWR is routed to output.<br>This pin is tri-stated for all other<br>combinations. |   |
| LSP5_DE     |             | 75                    | C10                    | PASS_THRU Debug Enable Output<br>on LSP 5.   | Logic '1'   |
|             |             |                       |                        | Active low output when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 100.<br>This pin is high for all other<br>combinations.   |   |
| LSP6_TCK    | OUT         | 61                    | F10                    | IEEE1149.1 Test Clock on LSP 6<br>when PASS_THRU_ENABLE is<br>HIGH.  | Buffered version<br>of signal present<br>on primary TCK |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101.<br>This pin is tri-stated for all other<br>combinations.                                     |   |

| PIN NAME    | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION   | Stable state after port/reset                            |
|-------------|-------------|-----------------------|------------------------|---|--|
| LSP6_TMS    | OUT         | 60                    | F9                     | IEEE1149.1 Test Mode Select on<br>LSP 6 when PASS_THRU_ENABLE<br>is HIGH.   | Logic '1'  |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101.<br>This pin is tri-stated for all other<br>combinations.                                    |  |
| LSP6_TDO    | OUT         | 57                    | G10                    | IEEE1149.1 Test Data Out on LSP 6<br>when PASS_THRU_ENABLE is<br>HIGH.  | Logic '1'  |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101.<br>This pin is tri-stated for all other<br>combinations.                                    |  |
| LSP6_TDI    | IN          | 58                    | G8                     | IEEE1149.1 Test Data In on LSP 6<br>when PASS_THRU_ENABLE is<br>HIGH.   |  |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101.   |  |
| LSP6_TRST   | OUT         | 64                    | E9                     | IEEE1149.1 Test Reset on LSP 5<br>when PASS_THRU_ENABLE is<br>HIGH.   | Buffered version<br>of signal present<br>on primary TRST |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101.   |  |
| LSP6_AutoWR | OUT         | 63                    | F7                     | Flash, Memory Auto-Write on LSP 6<br>when PASS_THRU_ENABLE is<br>HIGH.  | Logic '1'  |
|             |             |                       |                        | Pin is in Pass-Through mode when<br>PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101;<br>PRIM_AutoWR is routed to output.<br>This pin is tri-stated for all other<br>combinations |  |

| PIN NAME    | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP | PIN<br>NUMBER<br>FPBGA | DESCRIPTION   | Stable state<br>after port/reset |
|-------------|-------------|-----------------------|------------------------|---|----------------------------------|
| LSP6_DE     | OUT         | 65                    | E10                    | PASS_THRU Debug Enable Output<br>on LSP 6.  | Logic '1'                        |
|             |             |                       |                        | PASS_THRU_ENABLE = 0 and<br>PASS_THRU_SEL[2:0] = 101.<br>This pin is high for all other<br>combinations.  |                                  |
| PRIM_TCK    | IN          | 87                    | A6                     | IEEE1149.1 Primary Test Clock<br>Input.   |                                  |
| PRIM_TMS    | IN          | 21                    | G2                     | IEEE1149.1 Primary Test Mode<br>Select Input.   |                                  |
| PRIM_TDO    | OUT         | 20                    | G1                     | IEEE1149.1 Primary Test Data<br>Output. This pin is tri-stated when<br>AS91L1006BUis not selected.  | HighZ                            |
| PRIM_TDI    | IN          | 19                    | G3                     | IEEE1149.1 Primary Test Data Input  |                                  |
| PRIM_TRST   | IN          | 22                    | H2                     | IEEE1149.1 Primary Test Reset<br>Input.   |                                  |
|             |             |                       |                        | This active low asynchronous reset<br>input signal places AS91L1006U in<br>Wait-for-Selection state.  |                                  |
| PRIM_AutoWR | IN          | 16                    | F1                     | Primary Auto-Write Input controlled<br>by test equipment to shorten Flash<br>memory programming.  |                                  |
| S[5:0]      | IN          | 8,7,6,5,100,<br>99    | D2,D1,D3,C<br>2,B2,A2  | AS91L1006BU Slot Address[5:0]<br>Inputs.  |                                  |
|             |             |                       |                        | Used to set address at which<br>AS91L1006BU will respond; typically<br>set by hardwired connection on the<br>backplane.   |                                  |
| *TOE        | IN          | 88                    | B6                     | Test Output Enable Input.<br>Tri-states all LSPs, when asserted   |                                  |
| ISP RESET n | IN          | 14                    | F4                     | IOW.<br>I SP Reset Innut  | <u> </u>                         |
|             |             |                       |                        | Active low resets AS91L1006BU to<br>"Wait-for-Selection" state and pulses<br>all LSP TRST output pins to low.<br>This resets all devices with TRST<br>function; typically this signal would be<br>connected to a power-on-reset<br>function |                                  |

| PIN NAME                  | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP  | PIN<br>NUMBER<br>FPBGA                                       | DESCRIPTION  | Stable state after port/reset |
|---------------------------|-------------|--|--|--|-------------------------------|
| AS91L1006BU_<br>SELECTED  | OUT         | 25   | К1   | AS91L1006BU_Selected Output.<br>Active low when AS91L1006BU is<br>selected; typically used to control off<br>board buffering.  | Logic '1'                     |
| LSP_ENABLE                | OUT         | 24   | J1   | LSP Enabled Output.<br>Active low when AS91L1006BU is<br>selected; typically used to set<br>IEEE1149.1 compliance enable pins<br>on devices.   | Logic '1'                     |
| USER_STATUS<br>_BYTE[7:0] | IN          | 84, 85, 92,<br>93, 94, 96,<br>97, 98<br>(MSB-LSB)            | C7,C6,C5,C<br>4,B4,A4,B3,<br>A3(MSB-<br>LSB)                 | AS91L1006BU Status_Byte Inputs.<br>Used to provide status information of<br>the PCB under test back to the test<br>master via the IEEE1149.1 bus. Eight<br>signals levels can be monitored and<br>then reported via the IEEE1149.1 bus<br>in a non intrusive manner. |                               |
| SELF_TEST                 | OUT         | 27   | K2   | Provides a low going output pulse<br>under command from the<br>IEEE1149.1 bus, which can be used<br>to start self-test functions on a PCB.   | Logic '1'                     |
| PASS_THRU_<br>ENABLE      | IN          | 9  | E4   | PASS_THRU Enable Input.<br>Active high disables Pass-Through<br>mode.<br>Active low enables Pass-Through<br>mode.  |                               |
| PASS_THRU_<br>SEL12:0]    | IN          | 13,12,10<br>(MSB-LSB)  | E2,E1,E3<br>(MSB-LSB)  | PASS_THRU Select Inputs.<br>Used to select active routing of Pass-<br>Through ports enabled by active low<br>on PASS_THRU_ENABLE pin.<br>000 = LSP1<br>001 = LSP2<br>010 = LSP3<br>011 = LSP4<br>100 = LSP5<br>101 = LSP6  |                               |
| GND                       | POWER       | 38, 86, 11,<br>26, 43, 59,<br>74, 95, 2,<br>17, 54, 55<br>90 | D6, G5, C3,<br>D7, E5, F6,<br>G4,H8, H9,<br>J9,B1, A5,<br>F2 | Ground pins.   |                               |

|                  | PIN<br>TYPE | PIN<br>NUMBER<br>LQFP                        | PIN<br>NUMBER<br>FPBGA                        | DESCRIPTION  | Stable state<br>after port/reset |
|------------------|-------------|--|---|--|----------------------------------|
| VCC              | POWER       | 39, 91, 3,<br>18, 34, 51,<br>66,<br>82,23,56 | D5, G6, C8,<br>D4, E6, F5,<br>G7,<br>H3,G9,H1 | VCC pins.  |                                  |
| ASIC_TEST_<br>EN | IN          | 89   | B5  | Factory Test_Enable Input.<br>This pin should be left unconnected. |                                  |
| ASIC_TCK         | IN          | 62   | F8  | IEEE1149.1 ASIC Test Clock Input.                                  |                                  |
| ASIC_TMS         | IN          | 15   | F3  | IEEE1149.1 ASIC Test Mode Select.<br>Input                         |                                  |
| ASIC_TDO         | OUT         | 73   | A10   | IEEE1149.1 ASIC Test Clock Output.                                 |                                  |
| ASIC_TDI         | IN          | 4  | A1  | IEEE1149.1 ASIC Test Clock Input.                                  |                                  |
| No Connects      |             | 1  | C1  |  |                                  |

#### Table 9 - AS91L0006BU Signal Description

### **Absolute Maximum Ratings**

| Parameter                                      | Maximum Range        |
|--|----------------------|
| Supply Voltage (Vcc)                           | -0.3V to 5.5V        |
| DC Input Voltage (Vi)                          | -0.5V to Vcc +0.5V   |
| Max sink current when Vi = -0.5V               | -20mA                |
| Max source current when Vi = Vcc + 0.5V        | +20mA                |
| Max Junction Temperature with power applied Tj | +125 degrees C       |
| Max Storage temperature                        | -55 to +150 degree C |

#### Table 10 - Absolute Maximum Ratings

Note: Stress above the stated maximum values may cause irreparable damage to the device. Correct operation of the device at these values is not guaranteed.

### **Recommended Operating Conditions**

| Parameter            | Operating Range |  |
|----------------------|-----------------|--|
| Supply Voltage (Vcc) | 3.0V to 3.6V    |  |

| Input Voltage (Vi)                       | 0V to Vcc                             |
|--|---------------------------------------|
| Output Voltage (Vo)                      | 0V to Vcc                             |
| Operating Temperature (Ta)<br>Commercial | 0 C to 70 C                           |
| Industrial (Ta)                          | -40 deg C to +85 deg C, 3.00V to 3.6V |

Table 11 - Recommended Operating Conditions

### **AC Electrical Characteristics**



#### Figure 4 - AS91L1006BU AC Timing Diagram

| SYMBOL | Parameter                           | MIN | MAX | UNITS |
|--------|-------------------------------------|-----|-----|-------|
| Tcw    | TCK clock pulse width               | 100 | -   | ns    |
| Tch    | TCK pulse width high                | 50  | -   | ns    |
| Tcl    | TCK pulse width low                 | 50  | -   | ns    |
| Tsu    | TCK Setup time                      | 30  | -   | ns    |
| Th     | TCK Hold time                       | 40  | -   | ns    |
| Тое    | Neg Edge TCK to valid data enable   | 20  | -   | ns    |
| Тсо    | Neg Edge TCK to valid data          | 15  | -   | ns    |
| Tpd    | Pass through Mode Primary/Lsp Delay | -   | 10  | ns    |

Table 12 - AS91L1006BU AC Timing Information

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### **DC Electrical Characteristics**

| Symbol | Parameter                           | Мах          | Min   | Condition                            |
|--------|-------------------------------------|--------------|-------|--------------------------------------|
| VIH    | Minimum High Input<br>Voltage       | 5.25         | 2.0   |                                      |
| VIL    | Maximum Low Input<br>Voltage        | 0.8V         | -0.3V |                                      |
| Symbol | Parameter                           | Value        |       | Condition                            |
| VOH    | Minimum High Output<br>Voltage      | 2.4V         |       | loh=24mA or 8mA as defined<br>by pin |
| VOL    | Minimum LowOutput<br>Voltage        | 0.4V         |       | lol=24mA or 8mA as defined<br>by pin |
| loz    | Tristate output leakage             | -10 or 10 mA |       |                                      |
| lcc    | Maximum quiecennt<br>supply current | 2mA          |       |                                      |
| lccd   | Maximum dynamic<br>supply current   | 80mA         |       | TCK freq equal to 10 MHz             |

Table 13 - AS91L1006BU DC Electrical Characteristics

### **AC Timing Information**

| From         | То           | Туре       | Value |
|--------------|--------------|------------|-------|
| Prim_TCK     | Prim inputs  | Setup      | 6ns   |
| Prim_TCK     | Prim inputs  | Hold       | 1ns   |
| LSP[1:6]_TCK | LSP inputs   | Setup      | 6ns   |
| LSP[1:6]_TCK | LSP inputs   | Hold       | 0ns   |
| Prim inputs  | LSP outputs  | Comb Delay | 11ns  |
| LSP inputs   | Prim outputs | Comb Delay | 11ns  |
| Prim_TCK     | LSP_TCK      | Comb Delay | 10ns  |
| Prim_TCK     | Prim outputs | Delay      | 11ns  |
| LSP_TCK      | LSP outputs  | Delay      | 7ns   |
| Prim_TCK     |              | Freq       | 40MHz |

Table 14 - AS91L1006BU AC timing information

### **Packaging Information**

The AS91L1006BU is available in a 100-pin LQFP or a 100-pin FPBGA lead free package.





| Revisions |  |   |       |          |
|-----------|--|---|-------|----------|
| REV.      | DESCRIPTION  |   | ECN   | DATE     |
| A         | Initial document release.                              |   | 91253 | 12-04-01 |
| В         | Updated ball coplanarity limits from 0.20mm to 0.15mm. |   |       |          |
|           |  |   |       |          |
|           |  |   |       | C        |
|           | Î  | Ī |       | ⊃ 0.15 C |



| DIMENSIONS                  |  |  |  |  |
|-----------------------------|--|--|--|--|
| MIN. NOM.                   |  | MAX.   |  |  |
|                             |  |  |  |  |
| 0.30                        |  |  |  |  |
| 0.25                        |  | 1.10   |  |  |
| 0.50                        | 0.60   | 0.70   |  |  |
| 11.00 BSC                   |  |  |  |  |
| 9.00 BSC                    |  |  |  |  |
| 11.00 BSC                   |  |  |  |  |
| 9.00 BSC                    |  |  |  |  |
| 1.00                        |  |  |  |  |
| PACKAGE NUMBER FBGA0100-11F |  |  |  |  |
| MO-192 VAR. AAC-1           |  |  |  |  |
|                             | DIMENSIONS<br>MIN.<br><br>0.30<br>0.25<br>0.50<br> | MIN.         NOM.               0.30            0.25            0.50         0.60           11.00 BSC         9.00 BSC           11.00 BSC         9.00 BSC           11.00 FBGA0100-11F         MO-192 VAR. AAQ |  |  |



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### **Device Selector Guide and Ordering Information**





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| Part Number             | Description  |   |
|-------------------------|--|---|
| AS91L1006BU – 10L100-C  | JTAG 6-Port Gateway, 100-pin LQFP package, commercial                                  | now   |
| AS91L1006BU – 10L100-I  | 91L1006BU – 10L100-I JTAG 6-Port Gateway, 100-pin LQFP package, industrial             |   |
| AS91L1006BU – 10F100-C  | JTAG 6-Port Gateway 100-pin FPBGA package, commercial                                  | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 10F100-I  | JTAG 6-Port Gateway 100-pin FPBGA package, industrial                                  | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 40L100-C  | JTAG 6-Port Gateway, 100-pin LQFP package, commercial, High Frequency                  | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 40L100-CF | JTAG 6-Port Gateway, 100-pin LQFP<br>package, commercial, lead free, High<br>Frequency | now   |
| AS91L1006BU – 40L100-I  | JTAG 6-Port Gateway, 100-pin LQFP package, industrial, High Frequency                  | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 40L100-IF | JTAG 6-Port Gateway, 100-pin LQFP<br>package, industrial, lead free, High<br>Frequency | now   |
| AS91L1006BU – 40F100-C  | JTAG 6-Port Gateway 100-pin FPBGA, commercial, High Frequency                          | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 40F100-CG | JTAG 6-Port Gateway 100-pin FPBGA,<br>commercial, green package, High<br>Frequency     | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 40F100-I  | JTAG 6-Port Gateway 100-pin FPBGA,<br>industrial, High Frequency                       | Please Contact<br>Alliance<br>Semiconductor |
| AS91L1006BU – 40F100-IG | JTAG 6-Port Gateway 100-pin FPBGA,<br>industrial, green package, High Frequency        | Please Contact<br>Alliance<br>Semiconductor |

Table 15 - Valid Part Number Combinations

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| Device<br>Master | Description          | Package Options          |          |  |
|------------------|----------------------|--------------------------|----------|--|
| '<br>            |                      | FPBGA-100<br>(1mm pitch) | LQFP-100 |  |
| AS91L1001        | JTAG Test Controller | x                        | х        |  |
| AS91L1002        | JTAG Test Sequencer  | Х                        | Х        |  |
| AS91L1003U       | 3-Port Gateway       | Х                        | Х        |  |
| AS91L1006BU      | 6-Port Gateway       | Х                        | Х        |  |

Table 16 - JTAG Controller Product Family

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