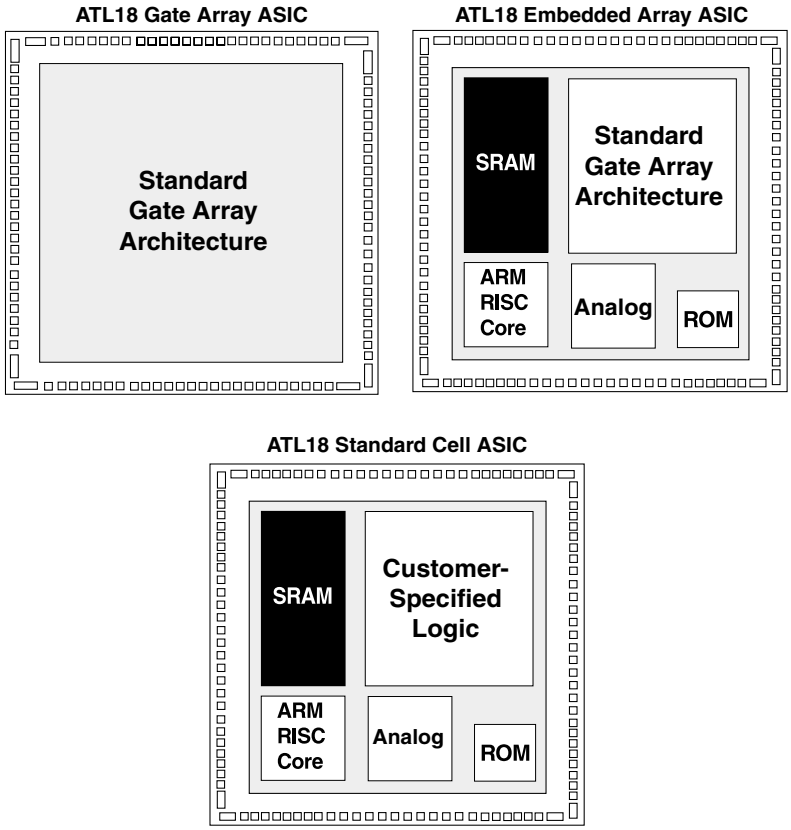
Features

- **Available in Gate Array, Embedded Array or Standard Cell**
- **High-speed, 75 ps Gate Delay, 2-input NAND, FO = 2 (nominal)**
- **Up to 13.7 Million Used Gates and 1516 Pins**
- **0.18µ Geometry in up to Six-level Metal**
- **System-level Integration Technology**
  - **Cores: ARM7TDMI™, ARM920T™ and ARM946E-S™ and MIPS64™ 5Kf™ RISC Microprocessors; AVR® RISC Microcontroller; Teak® and PalmDSPCore® Digital Signal Processors; 10/100 Ethernet MAC, USB, 1394, 1284, CAN and other Assorted Processor Peripherals**
  - **Analog Functions: DACs, ADCs, OPAMPs, Comparators, PLLs and PORs**
  - **Soft Macro Memory: Gate Array**
    SRAM — ROM — DPSRAM — FIFO
  - **Hard Macro Memory: Embedded Array or Standard Cell**
    SRAM — ROM — DPSRAM — FIFO — Stacked E^2 — Stacked Flash
  - **I/O Interfaces: CMOS, LVTTL, LVDS, PCI, USB; Output Currents up to 24 mA at 1.8V; 1.8V Native I/O, 2.5V Tolerant/Compliant I/O, 3.3V Tolerant/Compliant I/O, 5.0V Tolerant I/O**

Description

The ATL18 Series ASIC family is fabricated on a 0.18µ CMOS process with up to six levels of metal. This family features layouts with up to 13.7 million routable gates and 1516 pins. The high density and high pin count capabilities of the ATL18 family, coupled with the ability to embed microprocessor cores, DSP engines and memory on the same silicon, make the ATL18 series of ASICs an ideal choice for system-level integration.

Figure 1. ATL18 Technology



ASIC

ATL18 Series

Rev. 2005A–ASIC–06/02

Table 1. ATL18 Array Organization

Device Number	6LM Routable Gates[1]	Available Routing Sites[2]	Max Pad Count	Max I/O Count	Gate Speed[3]
ATL18/44	21,902	29,202	44	36	75 ps
ATL18/68	54,572	72,762	68	60	75 ps
ATL18/84	84,303	112,404	84	76	75 ps
ATL18/100	120,474	160,632	100	92	75 ps
ATL18/120	164,735	219,646	120	112	75 ps
ATL18/132	200,388	267,184	132	124	75 ps
ATL18/144	238,297	317,729	144	136	75 ps
ATL18/160	296,171	394,894	160	152	75 ps
ATL18/184	367,923	490,564	184	176	75 ps
ATL18/208	471,598	628,797	208	200	75 ps
ATL18/228	371,057	494,742	228	220	75 ps
ATL18/256	475,669	634,225	256	248	75 ps
ATL18/304	637,427	849,902	304	296	75 ps
ATL18/352	867,442	1,156,589	352	344	75 ps
ATL18/388	1,062,530	1,416,706	388	380	75 ps
ATL18/432	1,328,670	1,771,560	432	424	75 ps
ATL18/484	1,564,492	2,085,989	484	476	75 ps
ATL18/540	1,960,378	2,613,837	540	532	75 ps
ATL18/600	2,434,175	3,245,566	600	592	75 ps
ATL18/700	3,337,788	4,450,384	700	692	75 ps
ATL18/800	4,061,100	5,414,800	800	792	75 ps
ATL18/900	5,163,302	6,884,402	900	892	75 ps
ATL18/976	6,090,447	8,120,596	976	968	75 ps
ATL18/1132	7,597,266	10,129,688	1132	1124	75 ps
ATL18/1156	7,919,768	10,559,690	1156	1148	75 ps
ATL18/1312	10,235,584	13,647,445	1312	1304	75 ps
ATL18/1444	12,430,118	16,573,490	1444	1436	75 ps
ATL18/1516	13,715,871	18,287,828	1516	1508	75 ps

Notes: 1. One gate = NAND2
2. Routing site = 4 transistors
3. Nominal 2-input NAND gate, Fanout = 2 at 1.8V

Design

Atmel supports several major software systems for design with complete cell libraries, as well as utilities for netlist verification, test vector verification and accurate delay simulations.

Table 2. Design Systems Supported

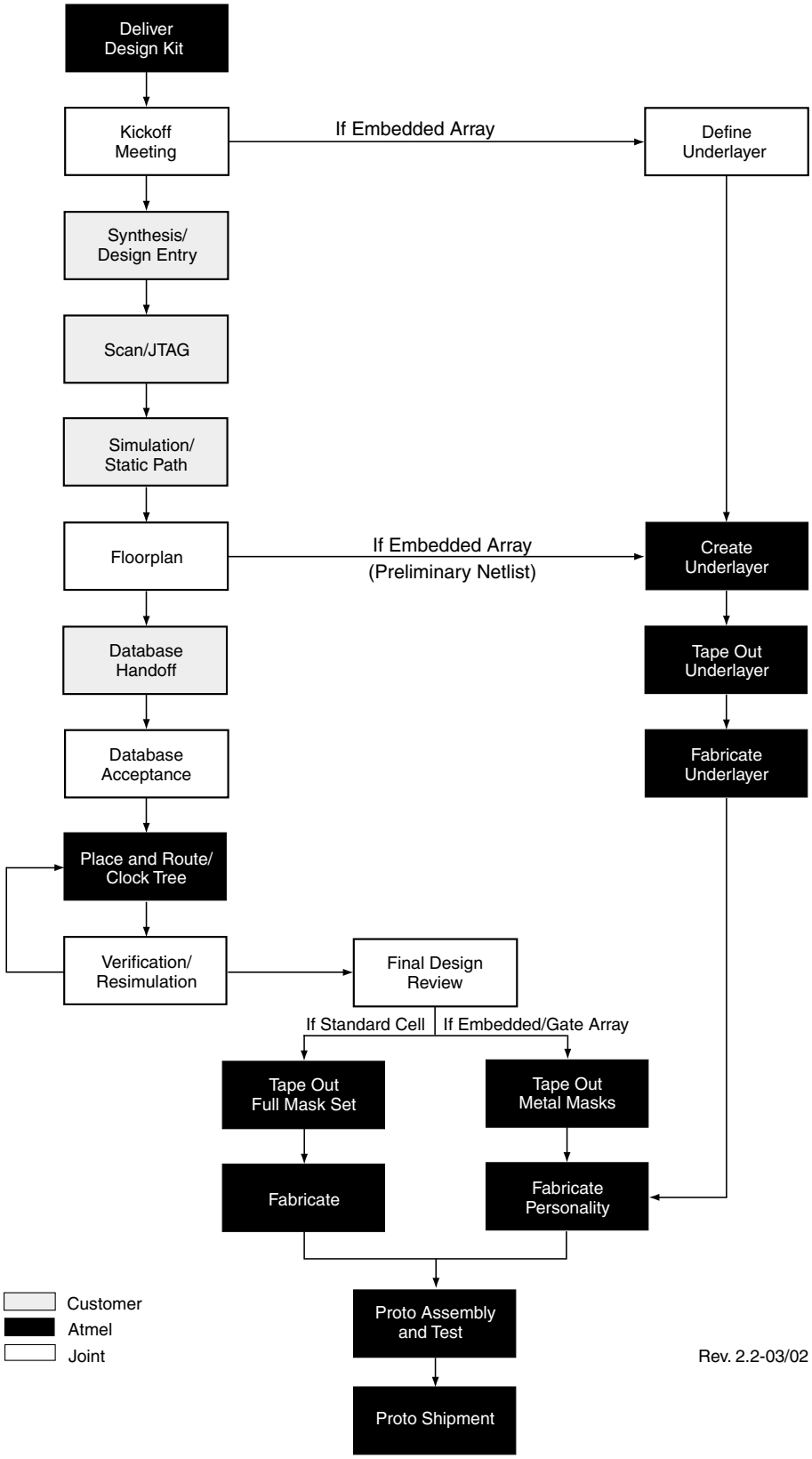
System	Tools	Version
Cadence® Design Systems, Inc.	Opus™ – Schematic and Layout	4.46
	NC Verilog™ – Verilog Simulator	3.3-s008
	Pearl™ – Static Path	4.3-s095
	Verilog-XL™ – Verilog Simulator	3.3-s006
	BuildGates™ – Synthesis (Ambit)	4.0-p003
Mentor Graphics®	ModelSim® – Verilog and VHDL (VITAL) Simulator	5.5e
	Leonardo Spectrum™ – Logic Synthesis	2001.1d
Synopsys™	Design Compiler™ – Synthesis	01.01-SP1
	DFT Compiler – 1-Pass Test Synthesis	01.08-SP1
	BSD Compiler – Boundary Scan Synthesis	01.08-SP1
	TetraMax® – Automatic Test Pattern Generation	01.08
	PrimeTime™ – Static Path	01.08-SP1
	VCS™ – Verilog Simulator	5.2
	Floorplan Manager™	01.08-SP1
Novas Software, Inc.	Debussy®	5.1
Silicon Perspective™	First Encounter®	v2001.2.3

Atmel's ASIC design flow is structured to allow the designer to consolidate the greatest number of system components onto the same silicon chip, using widely available third-party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage and process, and includes the effects of metal loading, interlevel capacitance, and edge rise and fall times. The design flow includes clock tree synthesis to customer-specified skew and latency goals. RC extraction is performed on the final design database and incorporated into the timing analysis.

The ASIC design flow, shown on page 4, provides a pictorial description of the typical interaction between Atmel's design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning and scan insertion activities. Leading-edge tools from vendors such as Synopsys and Cadence are fully supported in the Atmel design flow. In the case of an embedded array design, Atmel will conduct a design review with the customer to define the partition of the embedded array ASIC and to define the location of the memory blocks and/or cores so an underlayer layout model can be created. In the case of a standard cell design, Atmel will conduct a design review with the customer to define the partition of the standard cell ASIC and to define the location of the standard cell components so a full mask set layout can be created.

Following database acceptance, automated test pattern generation (ATPG) is performed, if required, on scan paths using Synopsys tools; the design is routed; and post-route RC data is extracted. After post-route verification and a final design review, the design is taped out for fabrication.

Figure 2. Design Flow



Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 3.3V or 2.5V compliant or 5.0V tolerant buffers, an appropriate number of pad sites must be reserved for the VDD3 or VDD2 pins, which are used to distribute 3.3V or 2.5V power to the compliant buffers.

Design Options

Logic Synthesis

Atmel can accept RTL designs in Verilog or VHDL formats. Atmel fully supports Synopsys for Verilog or VHDL simulation as well as synthesis.

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors into Atmel ASICs. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated as a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors into Atmel ASICs. There are four primary reasons to convert from an FPGA/PLD to an ASIC:

- Conversion of high-volume devices for a single or combined design is cost effective.
- Performance can often be optimized for speed or low power consumption.
- Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements.
- In situations where an FPGA/PLD was used for fast cycle time prototyping, an ASIC may provide a lower cost answer for long-term volume production.

Macro Cores

AVR 8-bit RISC Microcontroller Core

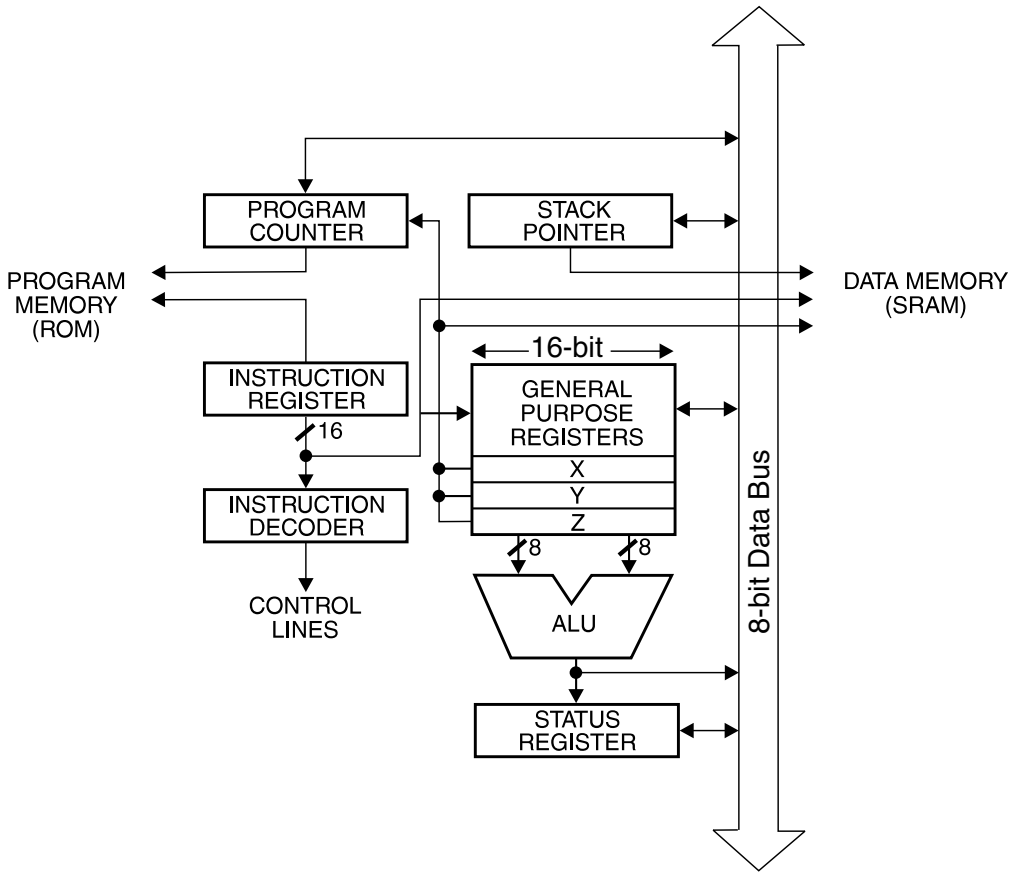
The AVR RISC microcontroller is a true 8-bit RISC architecture, ideally suited for embedded control applications. The AVR is offered as a gate level, synthesizable macro core in the ATL18 family.

The AVR supports a powerful set of 120 instructions. The AVR prefetches an instruction during a prior instruction execution, enabling the execution of one instruction per clock cycle.

The Fast Access RISC register file consists of 32 general-purpose working registers. These 32 registers eliminate the data transfer delay in the traditional program code intensive accumulator architectures.

The AVR can incorporate up to 64K x 16 program memory (ROM) and 64K x 8 data memory (SRAM). Among the peripheral options offered are: UART, 8-bit timer/counter, 16-bit timer/counter, programmable watchdog timer and SPI. Support for JTAG on-chip debugging has recently been added.

Figure 3. AVR 8-bit RISC Microcontroller Core



ARM7TDMI 32-bit RISC Microprocessor Core

The ARM7TDMI is a powerful 32-bit processor offered as a hard macro core in the ATL18 family.

The ARM7TDMI is a member of the ARM family of general purpose 32-bit microprocessors, which offer high performance with very low power consumption. Additionally, the ARM7T offers users a “thumb” mode (for higher code density using 16-bit instructions).

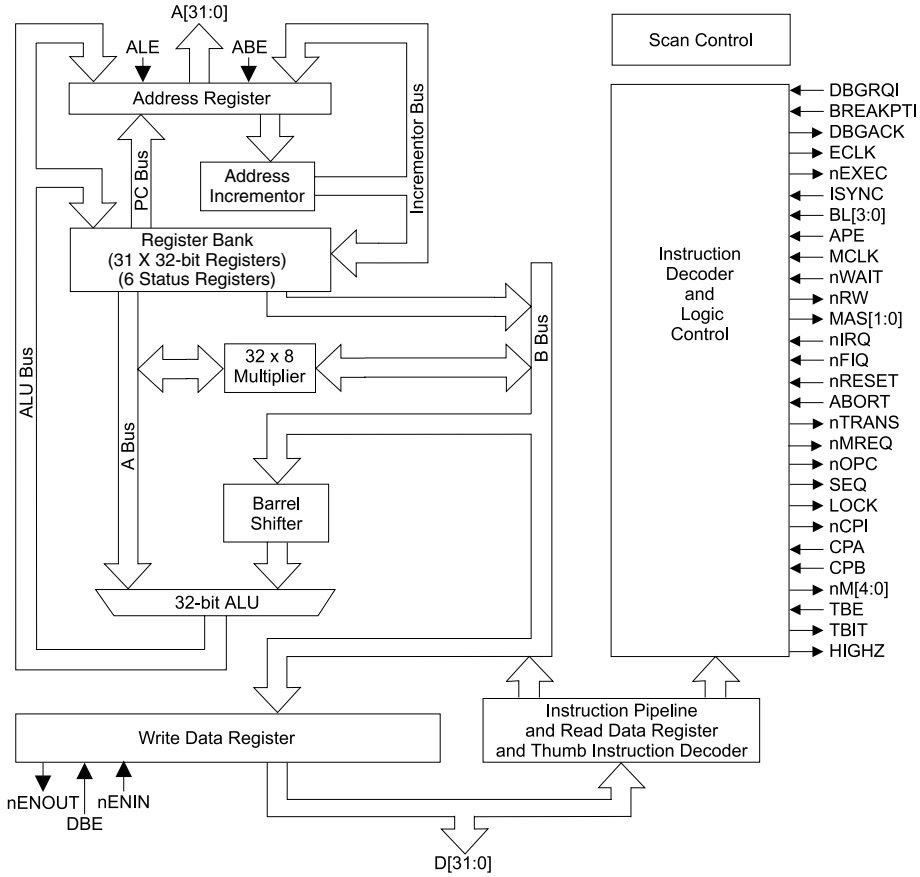
The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and an impressive real-time interrupt response from a small and cost-effective chip.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM memory interface has been designed to allow the performance potential to be realized without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard SRAMs.

The ARM7TDMI core interfaces to several optional peripheral macros. Among the peripheral options offered are real-time clock, peripheral data controller, USART, external bus interface, interrupt controller, timer counter and watchdog timer.

Figure 4. ARM7TDMI 32-bit RISC Microprocessor Core



ARM920T 32-bit RISC Microprocessor Core

The ARM920T extends the capabilities of the popular ARM7TDMI, while maintaining code compatibility and Thumb instruction compression. Enhancements include Harvard architecture and a memory management unit with virtual addressing support (allowing the use of advanced platform operating systems such as Windows CE™, Linux™, Symbian OS™ and VxWorks™). 16 Kbyte data and instruction caches are included.

ARM946E-S 32-bit RISC Microprocessor Core

The ARM946E-S is a synthesizable version of the ARM9E-S core, with similar features to the ARM920T. The ARM9E-S instruction set adds saturation logic to enhance DSP implementation, as well as double-word data moves. Additional DSP features include a single cycle 16 x 32 Multiply Accumulate (MAC) Unit. A memory protection unit is provided, but without full virtual memory support. As a result, the ARM946E-S is more suited to deeply embedded tasks that do not require extended-platform OS support. Cache sizes can be tailored to the application, resulting in a (potentially) smaller die size compared to the ARM920T.

MIPS64 5Kf 64-bit RISC Microprocessor Core

The MIPS64 5Kf is a synthesizable MIPS64 5K family core that provides 64-bit address and data paths along with an onboard IEEE 754-compliant Floating Point Unit. A built-in memory management unit with virtual addressing support allows the use of platform operating systems such as Windows CE and others. Also provided are configurable instruction and data caches, as well as a multiply divide unit capable of single cycle 32 x 16 Multiply Accumulate (MAC) operations.

Teak® and PalmDSPCore® Digital Signal Processing Cores

The Teak and Palm are synthesizable dual-MAC DSP cores from DSP Group, Inc. The Teak is a fixed-point 16-bit DSP, whereas the Palm can be configured for 16-bit, 20-bit or 24-bit fixed-point math. Both cores are optimized for high MIPs per mW, with performance targeted to handling filtering, voice compression/decompression and modem functions for portable and wireless applications such as 3G digital cellular. Hardware support is also provided for implementing Viterbi forward error correction.

The Teak and Palm cores both have a comprehensive suite of development tools that are easy to learn and are intended to support rapid code development. A C compiler that supports in-line assembly language and provides language extensions to enhance C code optimization is provided. An assembler and linker are also provided. Both emulation (using test silicon) and source-level simulation of C and assembly language enhance software verification.

ATL18 Series Cell Library

Atmel's ATL18 Series ASICs make use of an extensive library of cell structures, including logic cells, buffers and inverters, multiplexers, decoders and I/O options. Soft macros are also available.

These cells are characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test silicon. Characterization is performed over the rated temperature and voltage ranges to ensure simulation accuracy.

Absolute Maximum Ratings*

Parameter	Category	Rating
Operating Ambient Temperature		–55°C to +125°C
Storage Temperature		–65°C to +150°C
Maximum Input Voltage	base L25V L25, L33 L33V	V_{DD} + 0.5V 3.6V V_{HV} + 0.5V 5.5V
Maximum Operating Voltage (V_{DD})		2.0V
Maximum Operating Voltage (V_{HV})	L25, L25V L33, L33V	2.7V 3.6V

Note: * Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Characteristics

Symbol	Parameter	Category	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All			–55	–	125	°C
V_{DD}	V_{DD} Supply Voltage	All			1.6	1.8	2.0	V
V_{HV}	V_{HV} Supply Voltage	L25, L25V			2.3	2.5	2.7	V
		L33, L33V			3.0	3.3	3.6	
I_{IH}	High-level Input Current	Base	CMOS	$V_{IN} = V_{DD}$ (max)	–	–	5	µA
		L25V		V_{IN} = 3.6V				
		L25, L33		$V_{IN} = V_{HV}$ (max)				
		L33V		V_{IN} = 5.5V				
I_{IL}	Low-level Input Current	All	CMOS	$V_{IN} = V_{SS}$	–5	–	–	µA
I_{OZ}	High-impedance Output Current	Base	All	$V_{OUT} = V_{DD}$ (max)	–	–	5	µA
		L25V	All	V_{OUT} = 3.6V	–		5	
		L25, L33	All	$V_{OUT} = V_{HV}$ (max)	–		5	
		L33V	All	V_{OUT} = 5.5V	–		5	
		All	All	$V_{OUT} = V_{SS}$	–5		–	

Table 3. DC Characteristics (Continued)

Symbol	Parameter	Category	Buffer	Test Condition	Min	Typ	Max	Units
I_{OS}	Output Short-circuit Current	Base	PO11*	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)	–	12	–	mA
				$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)	–	–11	–	
		L25, L25V, L33, L33V	PO11L25V*	$V_{OUT} = V_{HV}$ (max), $V_{DD} = V_{HV}$ (max)	–	10	–	mA
				$V_{OUT} = V_{SS}$, $V_{DD} = V_{HV}$ (max)	–	–9	–	
V_{OH}	High-level Output Voltage	Base	PO11*	I_{OH} = 2 mA	0.75 V_{DD}	–	–	V
		L25, L25V	PO11L25*	I_{OH} = 2 mA	0.75 V_{HV}	–	–	
		L33, L33V	PO11L33*	I_{OH} = 2 mA	0.75 V_{HV}	–	–	
V_{OL}	Low-Level Output Voltage	Base	PO11*	I_{OL} = 2 mA	–	–	0.25V_{DD}	V
		L25, L25V	PO11L25*	I_{OL} = 2 mA	–	–	0.25V_{HV}	
		L33, L33V	PO11L33*	I_{OL} = 2 mA	–	–	0.25V_{HV}	
V_{IH}	High-level Input Voltage	Base	CMOS		0.65V_{DD}	–	–	V
		PCI			0.475V_{HV} (3.3.)			
		L25, L25V, L33, L33V			0.65V_{HV}			
V_{IL}	Low-level Input Voltage	Base	CMOS		–	–	0.35V_{DD}	V
		PCI					0.325V_{HV} (3.3)	
		L25, L25V, L33, L33V					0.35V_{HV}	
V_{HYS}	Hysteresis	Base	Schmitt	V_{DD} = 1.8V	–	0.31	–	V
		L25, L25V		V_{HV} = 2.5V		0.44		
		L33, L33V		V_{HV} = 3.3V		0.46		
C	Capacitance		Input or Output	3.3V	–	6.6	–	pF

Note: * Named buffer is given as an example only. All buffers in the category have these ratings.

I/O Buffer Cell Library

Buffer Interface Categories

ATL18 I/O buffers are designed to operate in specific interface environments. Buffers are assigned to one of several “interface categories” that define this environment with a specific supply voltage and interface voltage level. Tables 4 and 5 define all supported interface categories.

When selecting an I/O buffer for use in combination (as a bidirectional buffer), note that the input and output buffers selected must conform to the compatibility rules defined in Tables 4 and 5.

Table 4. Input Buffer Categories

Interface Category	Example Name	V_{HV}	V_{OUT} (Keeper/Pullup)	V_{IN}(H) Nominal	V_{IN}(H) Max	PO Compatibility	Char. Groups
Base	PIC	–	1.8	1.8	1.8	Base	1818_io
L25	PICKL25	2.5	2.5	2.5	2.5	L25	1825_iox
L25V	PICL25V	2.5	2.5	2.5	3.3	L25V	1825_iox
L33	PICKL33	3.3	3.3	3.3	3.3	L33	1833_iox
L33V	PICL33V	3.3	–	3.3	5.0	L33V	1833_iox

Table 5. Output Buffer Categories

Interface Category	Example Name	V_{HV}	$V_{OUT(H)}$	V_{TOL} (max)	PI Compatibility	Char. Groups	Max Available Drive
Base	PO44	–	1.8	1.8	Base	1818_io	24 mA
L25	PO44L25	2.5	2.5	2.5	L25	1825_iox	24 mA
L25V	PO44L25V	2.5	2.5	3.3	L25V	1825_iox	24 mA
L33	PO44L33	3.3	3.3	3.3	L33	1833_iox	24 mA
L33V	PO44L33V	3.3	3.3	5.0	L33V	1833_iox	24 mA

I/O Buffers

- Programmable output drive (2 mA–24 mA)
- Programmable slew rate control
- Programmable Pullup/Pulldown/Keeper

Timing and Derating Factors

Timings are generated from comprehensive transistor-level circuit simulation over temperature, voltage, process, loading and input slew rate. The library section includes pin-to-pin timings. Delays are represented as mx + b form, where *b* is the intrinsic delay through the cell (zero load), *x* is the output load and *m* is the load factor. All delays are expressed in nanoseconds. Load factors are in nanoseconds per picofarad for output buffers and in nanoseconds per load for all internal cells. Timing values listed are for nominal conditions (V_{DD} = 1.8 Volt, temperature = 25°C, nominal process).

Setup and hold times are worst case numbers for a military environment (1.6 Volts, 125°C, and worst case process). Timings are measured from the rising or falling edge of the data pin (50% of V_{DD}) to the rising edge of the clock (50% of V_{DD}). If setup or hold times are negative, the value is set to zero.

Simulation libraries contain individual derating for each cell, providing the most accurate delay numbers possible. Timing numbers in the cell library section can be used for estimation and comparison purposes under nominal conditions.

Note that timing numbers in the cell library should be used for rough approximation and relative comparison only. Atmel's simulation tools contain more sophisticated timing models.

Source of CMOS Power Dissipation

There are two primary components in standard CMOS power consumption:

- The major portion of the power dissipation is related to charging and discharging of gate and interconnect capacitance during switching. It directly varies with capacitance load, square of supply voltage, and frequency (P = C x V**2 x F).
- Quiescent or stand-by power dissipation comes primarily from two parasitic leakage paths. One is through the reverse bias P/N junctions inherent in CMOS, and the second is the subthreshold source to drain current of MOS transistors in their off state.

Peak current is calculated from the number of simultaneously switching registers in the device and may determine the minimum number of power and ground pins needed on a device. Another factor is the maximum amount of current drawn by I/O buffers between any two power or ground pads, which also influences the physical placement of power and ground pads.

Atmel provides a methodology for calculating both components separately. Refer to the *Atmel ASIC Power Estimation Worksheet* and the individual data sheets.

Testability Techniques

For complex designs involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs requires the use of more efficient testability techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in self-test (in addition to functional test patterns) must be employed to effectively test the product.

An example of a highly complex design could include analog blocks; a microprocessor or DSP engine or both; SRAM to support the microprocessor or DSP engine; and random logic to support customization and interconnectivity between blocks. Combinations of parametric, functional and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

Access to analog, microprocessor, DSP and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with minimum preconditioning. The ARM and MIPS microprocessors, AVR microcontroller, and TeakDSPCore/PalmDSPCore digital signal processors all support SCAN testing. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins is one method for providing this accessibility. BIST can also be used to perform SRAM testing.

The random logic can be designed using full SCAN techniques for testability.

Advanced Packaging

The ATL18 Series ASICs are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays and ball grid arrays. High-volume onshore and offshore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs. Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. If a standard package cannot meet a customer's needs, a package can be designed to precisely fit the customer-specific application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Table 6. Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
Power Quad	144, 160, 208, 240, 304
L/TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
PBGA	121, 169, 208, 217, 225, 240, 256, 272, 300, 304, 313, 316, 329, 352, 388, 420, 456
Super BGA	168, 204, 240, 256, 304, 352, 432, 560, 600
Low-profile Mini BGA	40, 48, 49, 56, 60, 64, 80, 81, 84, 96, 100, 108, 128, 132, 144, 160, 176, 192, 208, 224, 228
Chip-scale BGA(1)	32, 36, 40, 48, 49, 56, 64, 81, 84, 100, 108, 121, 128, 144, 160, 169, 176, 192, 208, 224, 256, 288, 324
Flex-tape BGA	48, 49, 64, 80, 81, 84, 96, 100, 112, 132, 144, 156, 160, 180, 192, 196, 204, 208, 220, 225, 228, 256, 280
FCBGA(2)	416, 480, 564, 672, 788, 896, 960, 1032, 1152, 1157, 1292, 1357, 1413, 1500, 1517, 1557, 1677, 1728, 1932

Notes: 1. Partial list
2. Require custom design substrate

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

---

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

2005A–ASIC–06/02