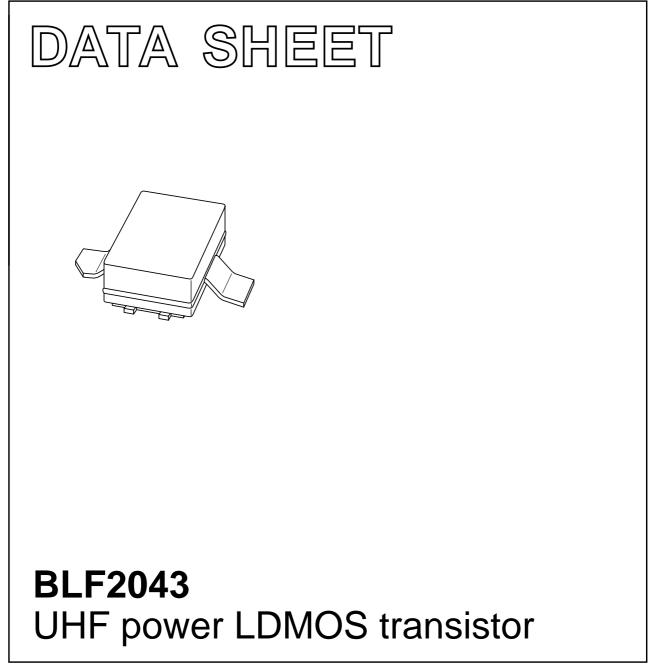
DISCRETE SEMICONDUCTORS



Product specification Supersedes data of 2002 Sep 10 2003 Feb 10



DESCRIPTION

UHF power LDMOS transistor

FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 85 mA:
 - Output power = 10 W (PEP)
 - Gain = 12 dB
 - Efficiency = 36.5%
 - dim = -32 dBc
- · Easy power control
- Excellent ruggedness
- High power gain
- · Excellent thermal stability
- Designed for broadband operation (HF to 2200 MHz)
- No internal matching for broadband operation.

APPLICATIONS

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the HF to 2200 MHz frequency range
- · Broadcast drivers.

DESCRIPTION

10 W LDMOS power transistor for base station applications at frequencies from HF to 2200 MHz.

QUICK REFERENCE DATA

Typical RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f	V _{DS}	P _L	G _p	η _D	d _{im}
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
CW, class-AB (2-tone)	f ₁ = 2000; f ₂ = 2000.1	26	10 (PEP)	12.5	36.5	-32

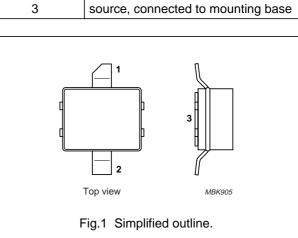
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		_	75	V
V _{GS}	gate-source voltage		_	±15	V
I _D	drain current (DC)		_	2.2	А
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	200	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.



PINNING - SOT538A

PIN

1

2

drain

gate

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-h}	thermal resistance from junction to heatsink	T _{mb} = 25 °C; note 1	9	K/W

Note

1. Thermal resistance is determined under RF operating conditions.

CHARACTERISTICS

 $T_i = 25 \ ^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	PARAMETER CONDITIONS		TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0; I_D = 0.2 \text{ mA}$	65	-	-	V
V _{GSth}	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; \text{ I}_{D} = 20 \text{ mA}$	4	-	5	V
I _{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 26 V$	-	-	1.5	μA
I _{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V$	2.8	-	-	A
I _{GSS}	gate leakage current	$V_{GS} = \pm 15 \text{ V}; V_{DS} = 0$	-	-	40	nA
g _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; \text{ I}_{D} = 0.75 \text{ A}$	-	0.5	-	S
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 0.75 A	-	1.2	-	Ω
C _{is}	input capacitance	V _{GS} = 0; V _{DS} = 26 V; f = 1 MHz	-	11	-	pF
C _{os}	output capacitance	$V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz$	-	9	-	pF
C _{rs}	feedback capacitance	V _{GS} = 0; V _{DS} = 26 V; f = 1 MHz	-	0.5	-	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25$ °C; $R_{th mb-h} = 0.4$ K/W, unless otherwise specified.

MODE OF OPERATION	f	V _{DS}	I _{DQ}	P _L	G _p	ղը	d _{im}
	(MHz)	(V)	(mA)	(W)	(dB)	(%)	(dBc)
CW, class-AB (2-tone)	f ₁ = 2000; f ₂ = 2000.1	26	85	10 (PEP)	>11.8	>33	≤–26

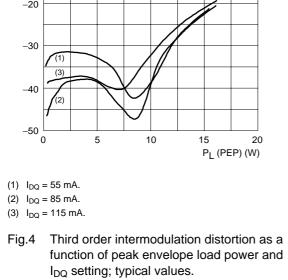
Ruggedness in class-AB operation

The BLF2043 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 2000 MHz at rated load power.

MCE017 60 MCE018 0 d_{im} (dBc) η_{D} (%) -20 d₃ 40 d₅ -40 d7 20 -60 0 -80 0 5 10 15 P_L (PEP) (W)

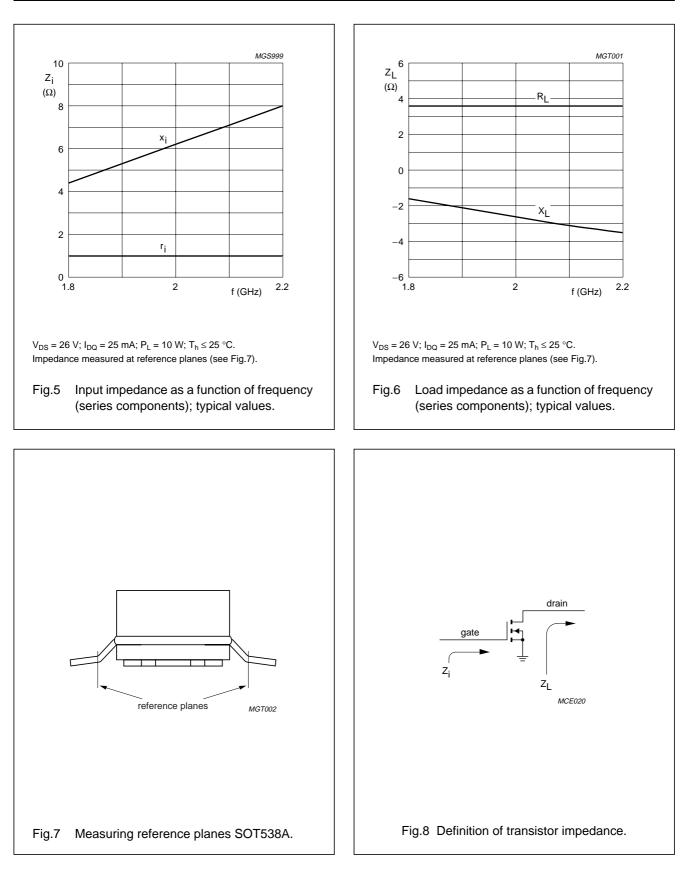
Intermodulation distortion as a function of Fig.3 peak envelope load power; typical values.

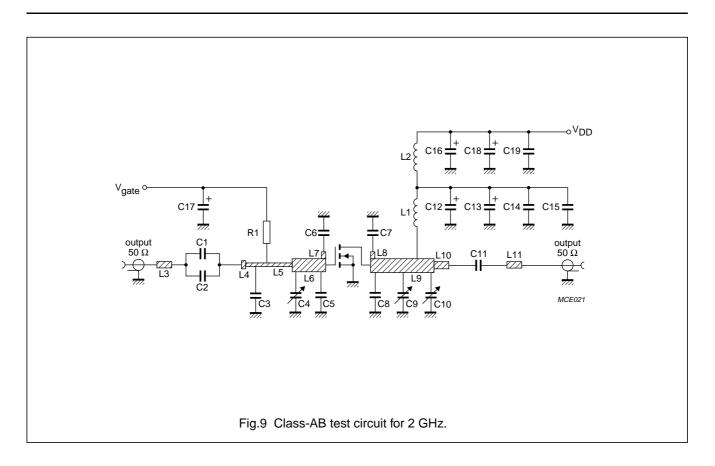
15 Gp G_p (dB) 10 η_D 5 0 0 5 10 15 20 P_L (PEP) (W) Fig.2 Power gain and efficiency as functions of peak envelope load power; typical values. MCE019 0 d_{im} (dBc) -10 -20



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20





List of components (see Figs 8 and 9)

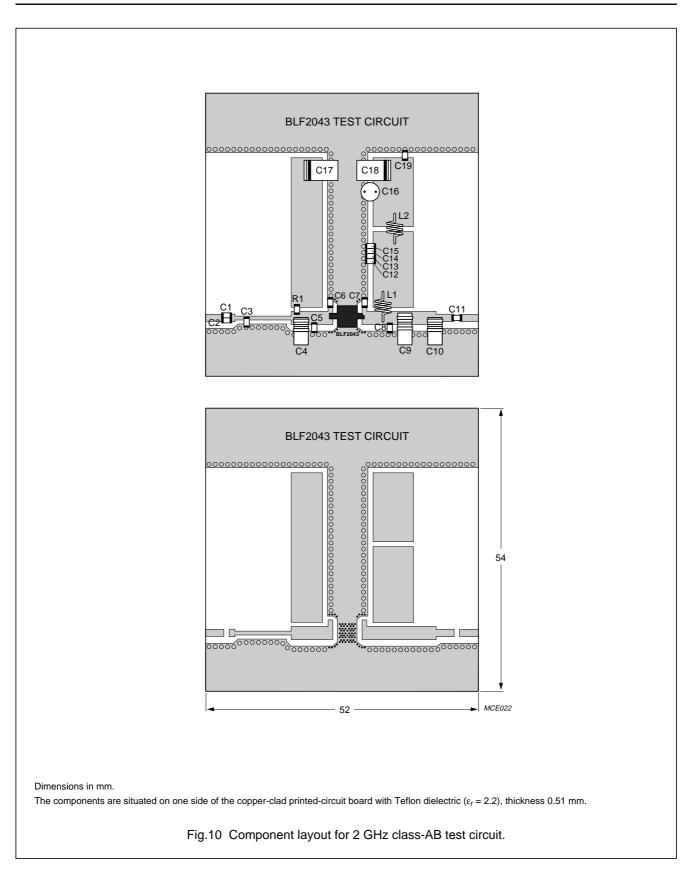
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	6.8 pF		
C3	multilayer ceramic chip capacitor; note 1	1.0 pF		
C4, C10, C11	tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C5, C7	multilayer ceramic chip capacitor; note 1	2.0 pF		
C6	multilayer ceramic chip capacitor; note 1	2.7 pF		
C8	multilayer ceramic chip capacitor; note 1	0.2 pF		
C9	multilayer ceramic chip capacitor; note 1	0.6 to 4.5 pF		
C12	multilayer ceramic chip capacitor; note 1	10 pF		
C13	multilayer ceramic chip capacitor; note 1	51 pF		
C14	multilayer ceramic chip capacitor; note 1	120 pF		
C15	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C16	electrolytic capacitor	100 μF; 63 V		2222 037 58101
C17, C18	tantalum SMD capacitor	10 μF; 35 V		
C19	multilayer ceramic chip capacitor; note 2	1 nF		
L1, L2	3 turns enamelled 0.5 mm copper wire		3 loops; d = 3 mm length = 3 mm	
L3	stripline; note 3	50 Ω	3.5 imes 1.5 mm	
L4	stripline; note 3	50 Ω	1.0 × 1.5 mm	
L5	stripline; note 3	73.2 Ω	5 × 2 mm	
L6	stripline; note 3	31 Ω	$11.0 \times 0.8 \text{ mm}$	
L7, L8	stripline; note 3	64.7 Ω	1.5 × 1.0 mm	
L9	stripline; note 3	31 Ω	$14.4 \times 3.0 \text{ mm}$	
L10, L11	stripline; note 3	50 Ω	3.5 imes 1.5 mm	
R1	metal film resistor	2.2 kΩ; 0.6 W		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.

2. American Technical Ceramics type 100B or capacitor of same quality.

3. The striplines are on a double copper-clad printed-circuit board with Rogers 5880 dielectric (ϵ_r = 2.2); thickness 0.51 mm.

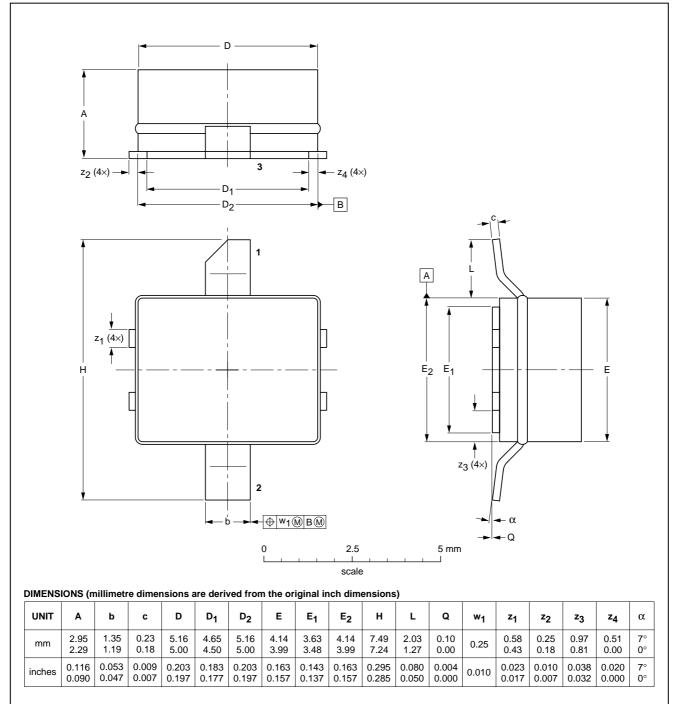


BLF2043

UHF power LDMOS transistor

PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads



OUTLINE		REFERENCES			EUROPEAN		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT538A						-00-03-03 02-08-20	

SOT538A

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
1	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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