

## CMOS 4-BIT MICROCONTROLLER

## TMP47C242BN

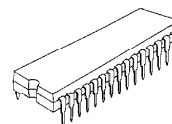
The 47C242B is high speed and high performance 4-bit single chip micro computers, integrating the 8-bit A/D converter and watchdog timer based on the TLC5-47 series.

| PART No.    | ROM          | RAM         | PACKAGE           | OTP         |
|-------------|--------------|-------------|-------------------|-------------|
| TMP47C242BN | 2048 × 8-bit | 128 × 4-bit | SDIP30-P-400-1.78 | TMP47P242VN |

## FEATURES

- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time : 1.9  $\mu$ s (at 4.2 MHz)
- ◆ 90 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting : 15 levels max.
- ◆ 6 interrupt sources (External : 2, Internal : 4)
  - All sources have independent latches each, and multiple interrupt control is available
- ◆ I/O port (23 pins)
  - Input 2 ports 5 pins
  - Output 2 ports 8 pins
  - I/O 4 ports 10 pins
- ◆ Interval timer
- ◆ Two 12-bit Timer / Counters
  - Timer, event counter, and pulse width measurement mode
- ◆ Watchdog Timer
- ◆ Serial Interface with 4-bit buffer
  - Internal clock, transfer only
- ◆ 8-bit successive approximate type A/D converter
  - With sample and hold
  - 4 analog inputs
  - Converting time : 48  $\mu$ s (4 MHz)
- ◆ High current outputs
  - LED direct drive capability (typ. 20 mA × 8 bits)
- ◆ Hold function
  - Battery / Capacitor back-up
- ◆ Real Time Emulator : BM47214A + BM1113

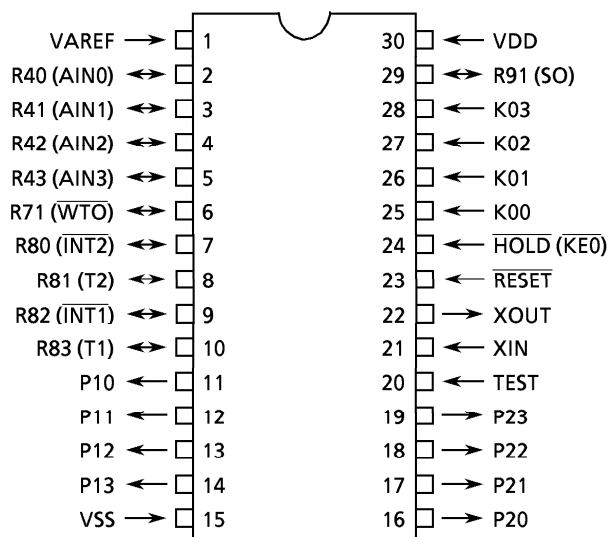
SDIP30-P-400-1.78



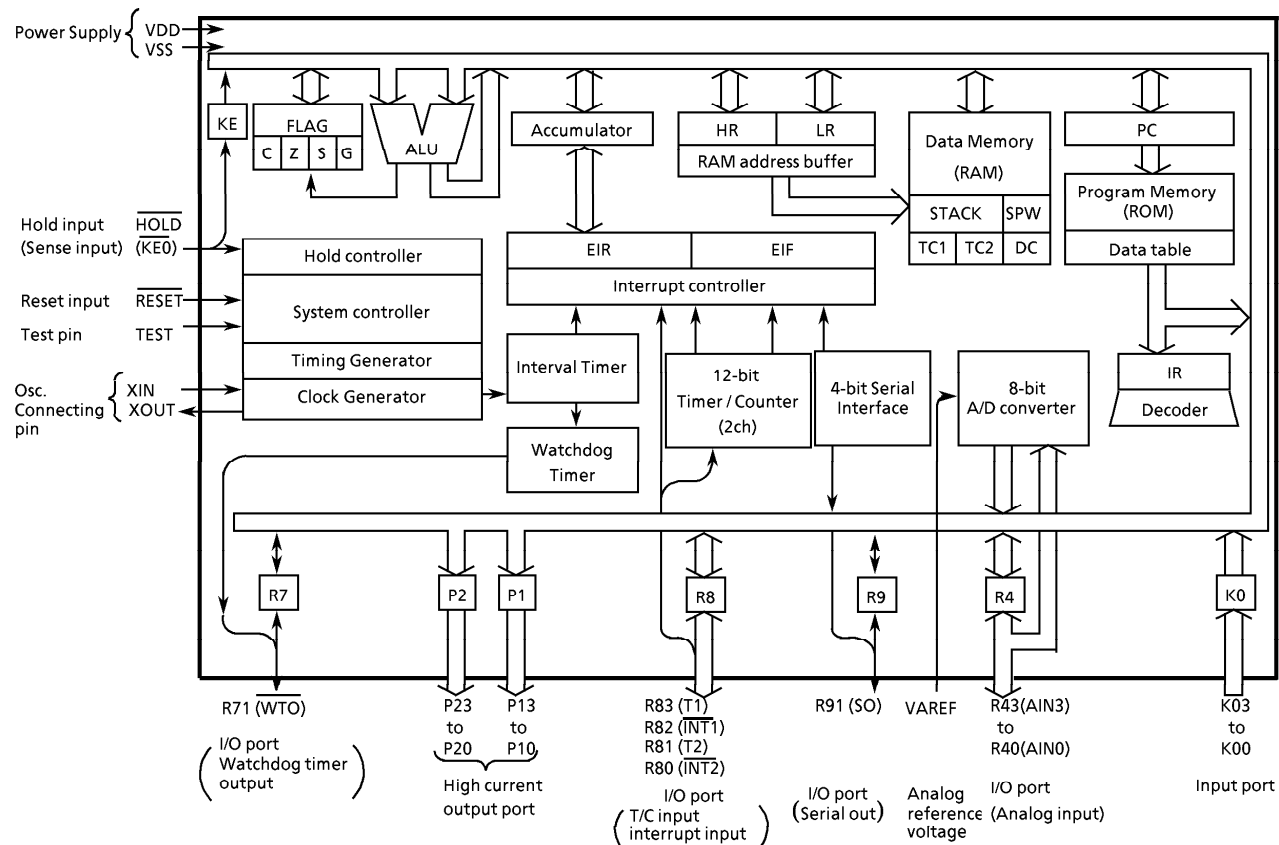
TMP47C242BN  
TMP47P242VN

## PIN ASSIGNMENT (TOP VIEW)

SDIP30-P-400-1.78



## BLOCK DIAGRAM



## PIN FUNCTION

| PIN NAME                         | Input/Output  | FUNCTIONS                                                                                                                                                      |                                        |
|----------------------------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|
| K03 to K00                       | Input         | 4-bit input port                                                                                                                                               |                                        |
| P13 to P10                       | Output        | 4-bit output port with latch.                                                                                                                                  |                                        |
| P23 to P20                       |               | 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].                                                                            |                                        |
| R43 (AIN3)<br>to<br>R40 (AIN0)   | I/O (Input)   | 4-bit I/O port with latch.<br>When using as input port, the latch must be set to "1".                                                                          | A/D converter analog input             |
| R71 ( $\overline{\text{WTO}}$ )  | I/O (Output)  | 1-bit I/O port with latch.<br>When using as input port or watchdog timer output, the latch must be set to "1".                                                 | Watchdog timer output                  |
| R83 (T1)                         | I/O (Input)   | 4-bit I/O port with latch.<br><br>When using as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1". | Timer / Counter 1 external input       |
| R82 ( $\overline{\text{INT1}}$ ) |               |                                                                                                                                                                | External interrupt 1 input             |
| R81 (T2)                         |               |                                                                                                                                                                | Timer / Counter 2 external input       |
| R80 ( $\overline{\text{INT2}}$ ) |               |                                                                                                                                                                | External interrupt 2 input             |
| R91 (SO)                         | I/O (Output)  | 1-bit I/O port with latch.<br>When using as input port or serial out, the latch must be set to "1".                                                            | Serial data output                     |
| XIN                              | Input         | Resonator connecting pin.<br>For inputting external clock, XIN is used and XOUT is opened.                                                                     |                                        |
| XOUT                             | Output        |                                                                                                                                                                |                                        |
| $\overline{\text{RESET}}$        | Input         | Reset signal input                                                                                                                                             |                                        |
| HOLD (KE0)                       | Input (Input) | HOLD request / release signal input                                                                                                                            | Sense input                            |
| TEST                             | Input         | Test pin for out-going test. Be opened or fixed to low level.                                                                                                  |                                        |
| VDD                              | Power supply  | + 5 V                                                                                                                                                          |                                        |
| VSS                              |               | 0 V (GND)                                                                                                                                                      | A/D converter analog reference voltage |
| VAREF                            |               | A/D converter analog reference voltage                                                                                                                         |                                        |

## OPERATIONAL DESCRIPTION

Concerning the 47C242B, the hardware configuration and operation are described.

As the description is provided with priority on those parts differing from the 47C200B, the technical data sheets for the 47C200B shall also be referred to.

### 1. SYSTEM CONFIGURATION

#### ◆ INTERNAL CPU FUNCTION

They are the same as those of the 47C200B.

#### ◆ PERIPHERAL HARDWARE FUNCTION

- ① I/O Ports
- ② Interval Timer
- ③ Timer / Counters (TC1, TC2)
- ④ A/D Converter
- ⑤ Watchdog Timer
- ⑥ Serial Interface

The description has been provided with priority on functions (①, ④, ⑤ and ⑥) added to and changed from the 47C200B.

### 2. PERIPHERAL HARDWARE FUNCTION

#### 2.1 Ports

The 47C242B has 8 I/O ports (23 pins) each as follows :

- ① K0 ; 4-bit input
- ② P1, P2 ; 4-bit output
- ③ R4 ; 4-bit input / output (shared by the A/D converter analog inputs)
- ④ R7 ; 1-bit input / output (shared by the watchdog timer output)
- ⑤ R8 ; 4-bit input / output (shared by external interrupt request input and timer / counter input)
- ⑥ R9 ; 1-bit input / output (shared by serial output)
- ⑦ KE ; 1-bit sense input (shared by hold request/release signal input)

This section describes ports of ③, ④ and ⑥ which are changed from the 47C200B.

Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

##### (1) Ports R4 (R43 to R40)

Ports R4 is 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

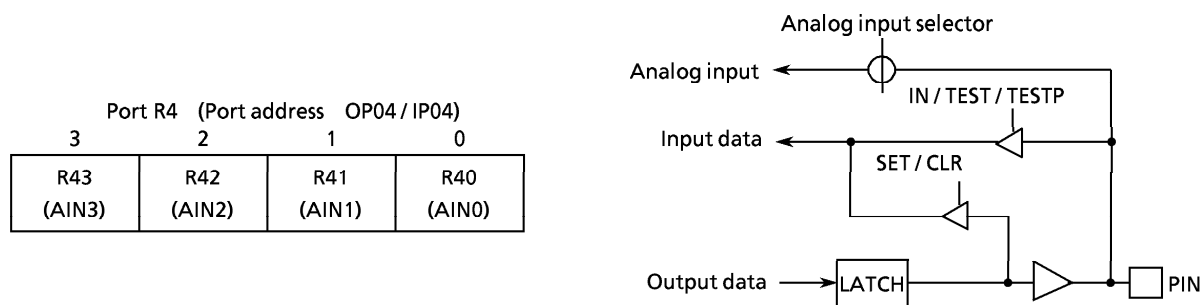


Figure 2-1. Port R4

## (2) Port R7 (R71)

1-bit I/O pin with latch. R71 pin is shared by the watchdog timer output. To use R71 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R70, R72, R73 pins do not exist actually but R70 has the latch. In R72 and R73, "1" is read when an input instruction is executed.

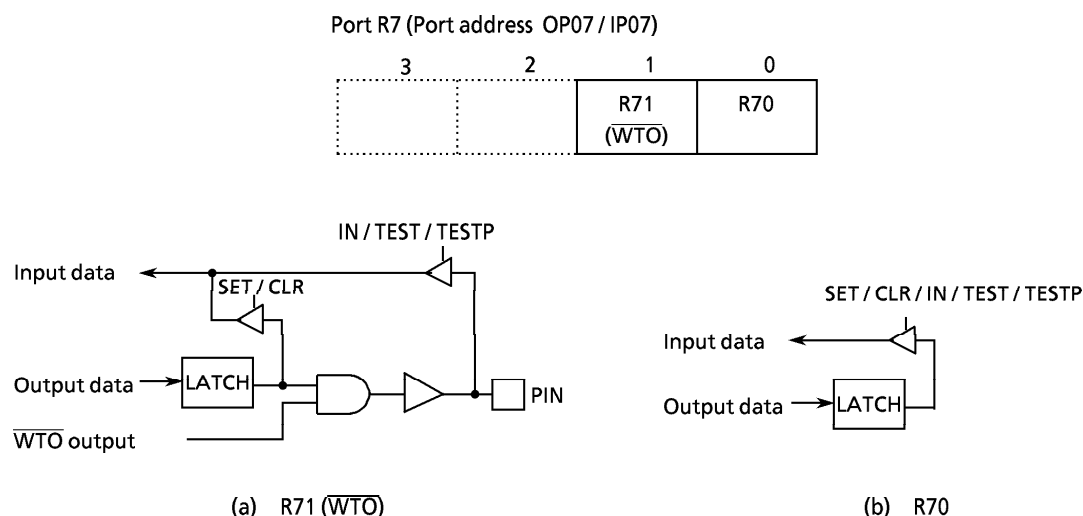


Figure 2-2. Port R7

## (3) Port R9 (R91)

1-bit I/O pin with latch. R91 pin is shared by the 4-bit serial output. To use R91 pin for the serial output, the latch should be set to "1". The latch is initialized to "1" during reset. R90, R92, R93 pins do not exist actually but R90 and R92 have the latches. In R93, "1" is read when an input instruction is executed.

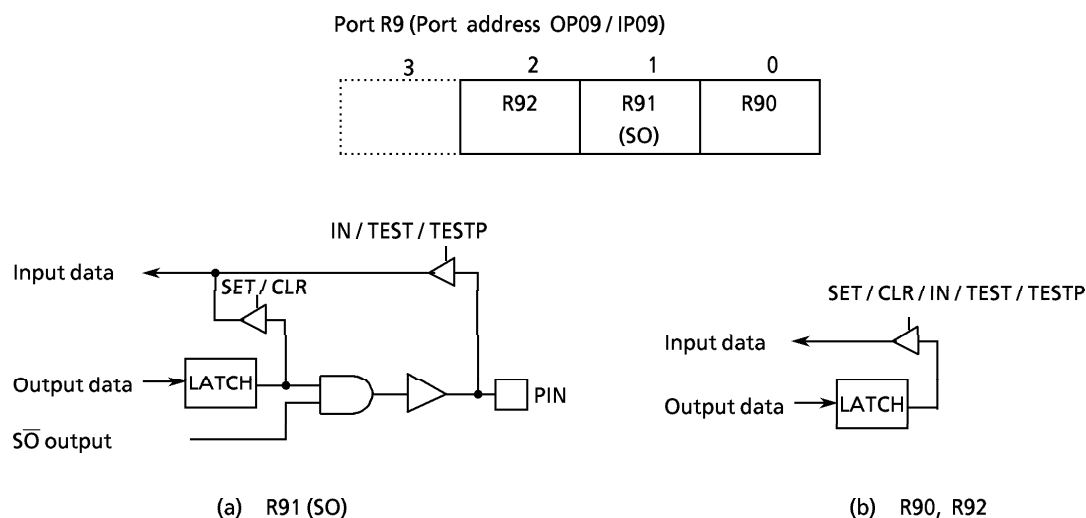


Figure 2-3. Port R9

Table 2-1. Port Address Assignments and Available I/O Instructions

| Port Address<br>(**) | Port                         |                                 | Input/Output instruction |                        |            |            |                      |                         |                             |
|----------------------|------------------------------|---------------------------------|--------------------------|------------------------|------------|------------|----------------------|-------------------------|-----------------------------|
|                      | Input (IP**)                 | Output (OP**)                   | IN %p, A<br>IN %p, @HL   | OUT A,%p<br>OUT @HL,%p | OUT #k, %p | OUTB @HL   | SET %p,b<br>CLR %p,b | TEST %p,b<br>TESTP %p,b | SET @L<br>CLR @L<br>TEST @L |
| 00 <sub>H</sub>      | K0 input port                | —                               | ○                        | -                      | -          | -          | -                    | ○                       | -                           |
| 01                   | P1 output latch              | P1 output port                  | ○                        | ○                      | ○          | ○ (Note 2) | ○                    | ○                       | -                           |
| 02                   | P2 output latch              | P2 output port                  | ○                        | ○                      | ○          | ○          | ○                    | ○                       | -                           |
| 03                   | —                            | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 04                   | R4 input port (Analog input) | R4 output port                  | ○                        | ○                      | ○          | -          | ○                    | ○                       | ○                           |
| 05                   | —                            | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 06                   | —                            | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 07                   | R7 input port                | R7 output port                  | ○                        | ○                      | ○          | -          | ○                    | ○                       | ○                           |
| 08                   | R8 input port                | R8 output port                  | ○                        | ○                      | ○          | -          | ○                    | ○                       | -                           |
| 09                   | R9 input port                | R9 output port                  | ○                        | ○                      | ○          | -          | ○                    | ○                       | -                           |
| 0A                   | —                            | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 0B                   | —                            | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 0C                   | A / D Status input           | —                               | ○                        | -                      | -          | -          | -                    | ○                       | -                           |
| 0D                   | A / D converted value        | —                               | ○                        | -                      | -          | -          | -                    | -                       | -                           |
| 0E                   | SIO, Hold status             | —                               | ○                        | -                      | -          | -          | -                    | ○                       | -                           |
| 0F                   | —                            | Serial transmit buffer          | -                        | ○                      | ○          | -          | -                    | -                       | -                           |
| 10 <sub>H</sub>      | Undefined                    | Hold operation mode control     | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 11                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 12                   | Undefined                    | A / D analog input selector     | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 13                   | Undefined                    | A / D start register            | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 14                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 15                   | Undefined                    | Watchdog Timer control          | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 16                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 17                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 18                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 19                   | Undefined                    | Interval Timer intrrupt control | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 1A                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 1B                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 1C                   | Undefined                    | Timer/Counter 1 control         | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 1D                   | Undefined                    | Timer/Counter 2 control         | -                        | ○                      | -          | -          | -                    | -                       | -                           |
| 1E                   | Undefined                    | —                               | -                        | -                      | -          | -          | -                    | -                       | -                           |
| 1F                   | Undefined                    | Serial interface control        | -                        | ○                      | -          | -          | -                    | -                       | -                           |

Note 1. “—” means the reserved state. Unavailable for the user programs.

Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

2.2 A/D Converter

The 47C242B has a 8-bit successive approximate type A/D converter and is capable of processing 4 analog inputs.

2.2.1 Circuit configuration

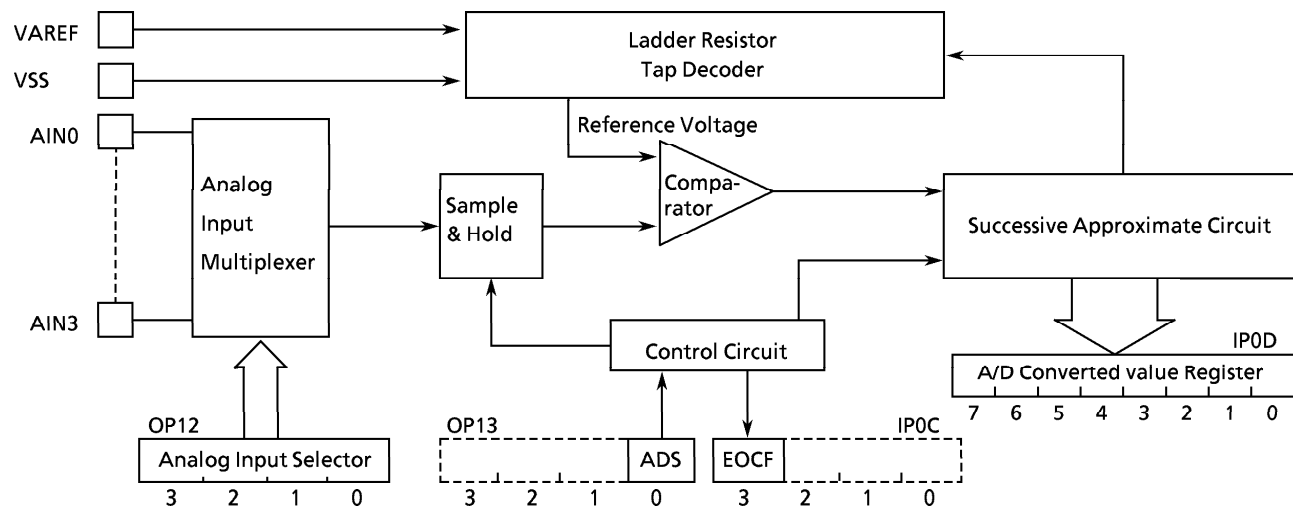


Figure 2-4. Block Diagram of A/D Converter

2.2.2 Control of A/D converter

The operation of A/D converter is controlled by a command register (OP12, OP13, IP0C, IP0D).

- (1) Analog input selector (OP12)  
Analog inputs (AIN0 through AIN3) are selected by values of this register.

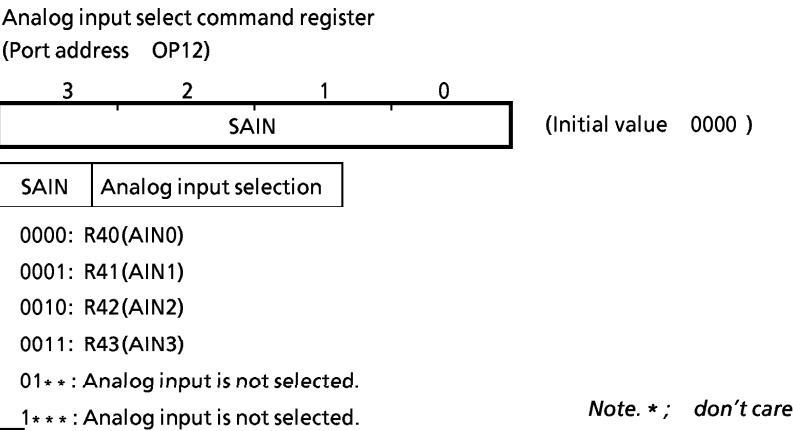


Figure 2-5. Analog input selector

## (2) Start of A/D conversion (OP13)

A/D conversion is started when ADS is set to "1". After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time. Analog input voltage is hold by the sample hold circuit.

A / D conversion start command register  
(Port address OP13)



|     |                         |
|-----|-------------------------|
| ADS | A / D conversion enable |
|-----|-------------------------|

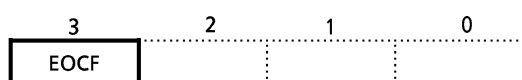
1: A/D conversion is started (clears after starting)

Figure 2-6. A/D conversion start register

## (3) A/D converter end register (IP0C)

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

A / D converter status register  
(Port address IP0C)



|      |                        |
|------|------------------------|
| EOCF | End of conversion flag |
|------|------------------------|

0: Under A/D conversion or before A/D conversion

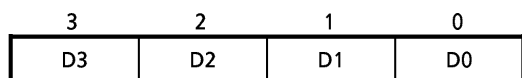
1: End of A/D conversion

Figure 2-7. A/D converter status register

## (4) A/D converted value register (IP0D)

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR<sub>0</sub> (LSB of the L-registers).

A / D converted value register  
(Port address IP0D)



|          |                              |
|----------|------------------------------|
| D7 to D0 | A/D converted value is read. |
|----------|------------------------------|

When LR<sub>0</sub> = 0, lower 4 bits of the converted value is read.

When LR<sub>0</sub> = 1, upper 4 bits of the converted value is read.

Figure 2-8. A/D converted value register

### 2.2.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VSS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VSS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

#### (1) Start of A/D conversion

Prior to conversion, select one of the analog input AIN0 through AIN3 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

Analog input voltage is sampled during the following 2 instruction cycles after setting conversion enable.

*Note.* The sample and hold circuit has capacitor ( $C_A = 12 \text{ pF typ.}$ ) with resistor ( $R_A = 5 \text{ k}\Omega \text{ typ.}$ ). See I/O circuitry table. This capacitor should be charged or discharged within 2 instruction cycles.

#### (2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).

Lower 4 bits of the A/D converted value can be read when  $LR_0 = 0$  and upper 4 bits when  $LR_0 = 1$ . Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during the conversion, it becomes an indefinite value.

#### (3) A/D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of A/D conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

Example: Selecting analog input (AIN3), starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10H] and RAM [11H] respectively.

```

LD      A, #3H          ; Selects analog input (AIN3)
OUT     A, %OP12
LD      A, #1H          ; Start of A/D conversion
OUT     A, %OP13
SLOOP : TEST    %IP0C, 3 ; To wait until EOCF goes to "1"
        B       SLOOP
LD      HL, #10H        ; HL ← 10H
IN      %IP0D, @HL      ; RAM [10H] ← Lower 4 bits
INC     L               ; Increment of L registers
IN      %IP0D, @HL      ; RAM [11H] ← Upper 4 bits

```

## 2.3 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (runaway) of program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the  $\overline{WTO}$  pin and  $\overline{RESET}$  pin are connected each other.

### 2.3.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

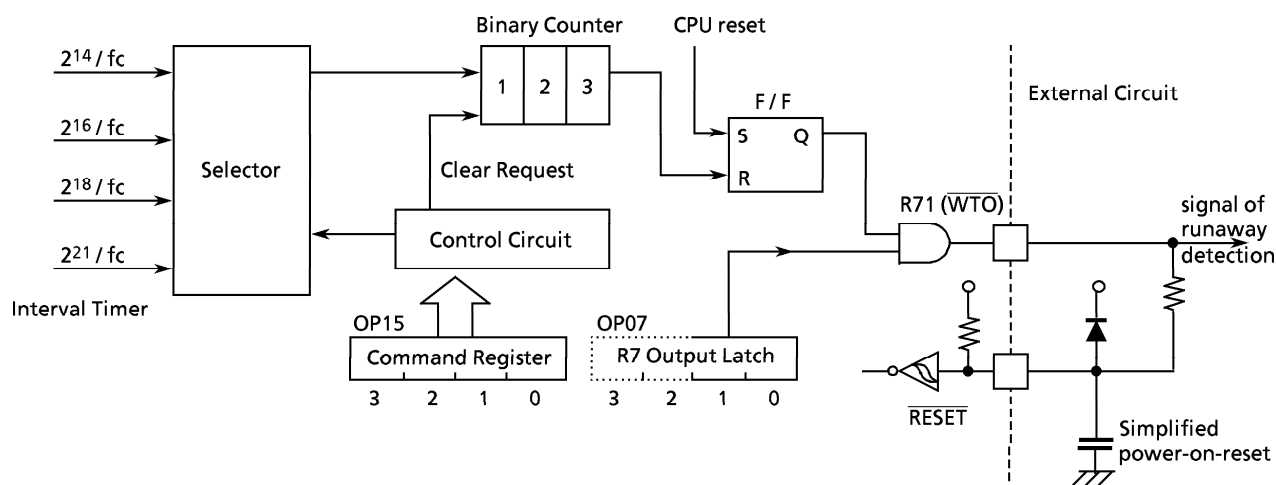


Figure 2-9. Watchdog Timer

### 2.3.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000<sub>B</sub>" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

- ① At first, detection time of the watchdog timer should be set and binary counter should be cleared.
- ② The watchdog timer should be become enable.
- ③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0" at the rising edge of the binary counter and signal of runaway detection is become active ( $\overline{WTO}$  output is "L").

Watchdog Timer control command register  
(Port address OP15)

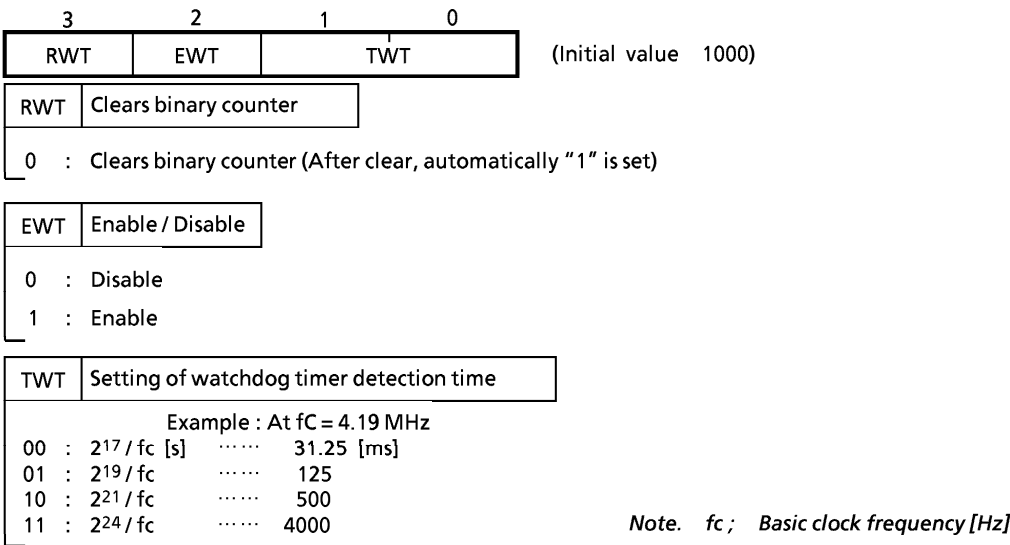


Figure 2-10. Command Register

Example : To set the watchdog detection time ( $2^{21}/f_C$  [s]). And to enable the watchdog timer.

```
LD      A, #0010B      ; OP15 ← 0010B
                               (Sets WDT detection time. Clears binary counter)
OUT     A, %OP15
LD      A, #0110B      ; OP15 ← 0110B (Enables WDT)
OUT     A, %OP15
Within WDT
detection time {
    :
    :
    :
    LD      A, #0110B      ; OP15 ← 0110B (Clears binary counter)
    OUT     A, %OP15
    :
    :
}
```

Note. RWT can be operated only clearing to "0". Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

## 2.4 Serial Interface

The 47C242B contain a serial output with 4-bit buffer. In the 47C242B, serial interface is available R91 (SO) pin only. This serial output is shared by R91 pin. For the serial output, the output latch of R91 must be set to "1". Serial clock do not care. However, buzzer driver, easy PWM output, and etc... can be used.

### 2.4.1 Condiguration of Serial Interface

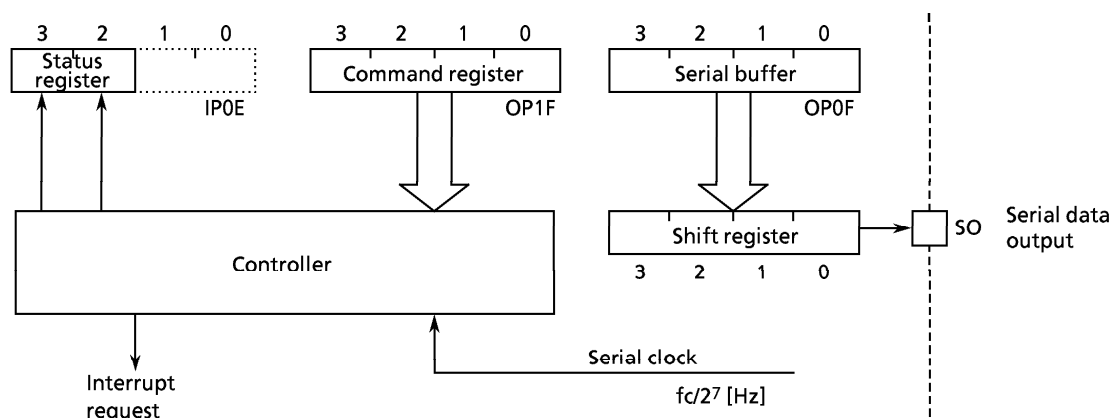


Figure 2-11. Configuration of Serial Interface

### 2.4.2 Control of Serial Interface

The serial output is controlled by the command register (OP1F). The command register is initialized to "0" during reset. The operating status of the serial output can monitor by the status register (IP0E). The status of the  $\overline{\text{HOLD}}$  (KE0) pis is assigned to bit 0 of this status register.

Serial Interface Control command register  
(Port address OP1F) (Initial value 0000)

| 3    | 2 | 1  | 0 |
|------|---|----|---|
| ESIO |   | RM |   |

| ESIO | Instructs serial output start/end |
|------|-----------------------------------|
|------|-----------------------------------|

0 : Serial output end  
1 : Serial output start

| RM | Serial output mode |
|----|--------------------|
|----|--------------------|

010 : Internal clock, shift at the leading edge of serial clock  
\*0\* : Unused  
\*\*1 : Unused  
1\*\* : Unused

Serial Interface status register  
(Port address IP0E)

| 3    | 2   | 1 | 0      |
|------|-----|---|--------|
| SIOF | SEF |   | (HOLD) |

| SIOF | Monitors serial output operation state |
|------|----------------------------------------|
|------|----------------------------------------|

0 : Output terminated  
1 : Output in process

| SEF | Monitors shit operation state |
|-----|-------------------------------|
|-----|-------------------------------|

0 : Shit terminated  
1 : Shift in process

**Note.** When setting the output mode, ESIO must be "0".  
\* : don't care

Figure 2-12. Command register / Status register

## (1) Serial clock

$f_c/27$  [Hz] is used for the shift clock (at  $f_c = 4.194304$  MHz, the shift clock frequency is 32.768 kHz). The shift clock can not be output on the pin.

When writing data in a program does not catch up the serial clock rate, this device stops the serial clock automatically. Additionally it provides the wait function in which the shift is not occurred until this processing is completed.

## (2) Serial output mode

Set the output mode by RM (bit 0 to 2 of the command register). The output mode is set to the command register then first output data (4-bits) is written to the buffer register OP0F (if the output mode is not set, the data is not written to the buffer register). Then, setting ESIO to "1" starts output. The output data is output to the SO pin synchronizaiton with the serial clock from the LSB side sequentially. When the LSB is output, the output data is moved from the buffer register to the shift register. When the buffer register becomes empty, the buffer empty interrupt (ISIO) to request for the next output data is generated. When the interrupt service program writes the output data to the buffer register, the interrupt request is reset. If no more data is set after the output of the 4-bit data, the serial clock is stopped and the wait state sets in.

To end output, ESIO is cleared to "0" instead of writing the next output data by the buffer empty interrupt service program. When ESIO is cleared, output stops upon output of the currently shifted-out data. The output end can be known by the SIOF state (SIOF goes to "0" upon output end).

Example 1: The data stored in the data memory (addresses is specified by HL register pair) output.

```
LD    A,#0010B
OUT   A,%OP1F
OUT   @HL,%OP0F
LD    A,#1010B
OUT   A,%OP1F
```

Example 2: After stopping the output is written, the operation waits until stopping.

```
LD    A,#0010B
OUT   A,%OP1F
SENDC :
      TESTP  %IP0E,3
      B      SENDC
      :
```

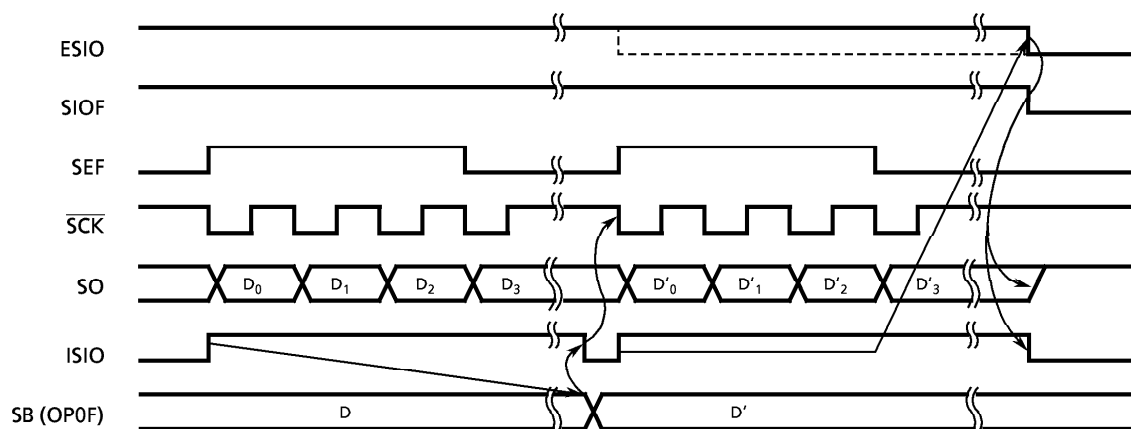


Figure 2-14. Output Timing with wait

## INPUT / OUTPUT CIRCUITRY

## (1) Control pins

The input / output circuitries of the 47C242B control pins are similar to that of the 47C200B.

## (2) I/O Ports

The input / output circuitries of the 47C242B I/O ports are shown as below, any one of the circuitries can be chosen by a code (SA-SC) as a mask option.

| PORT     | I/O    | INPUT/OUTPUT CIRCUITRY and CODE |    |    | REMARKS                                                                                                                                                                        |
|----------|--------|---------------------------------|----|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |        | SA                              | SB | SC |                                                                                                                                                                                |
| K0       | Input  |                                 |    |    | Pull-up / pull-down resistor<br>$R_{IN} = 70 \text{ k}\Omega \text{ (typ.)}$<br>$R = 1 \text{ k}\Omega \text{ (typ.)}$                                                         |
| P1<br>P2 | Output |                                 |    |    | Sink open drain output<br>Initial "Hi-Z"<br>High current<br>$I_{OL} = 20 \text{ mA (typ.)}$                                                                                    |
| R4       | I/O    |                                 |    |    | Sink open drain output<br>Initial "Hi-Z"<br>$R = 1 \text{ k}\Omega \text{ (typ.)}$<br>Analog input<br>$R_A = 5 \text{ k}\Omega \text{ (typ.)}$<br>$C_A = 12 \text{ pF (typ.)}$ |
| R7       | I/O    |                                 |    |    | Sink open drain output<br>Initial "Hi-Z"<br>$R = 1 \text{ k}\Omega \text{ (typ.)}$                                                                                             |
| R8<br>R9 | I/O    |                                 |    |    | Sink open drain output<br>Initial "Hi-Z"<br>Hysteresis input<br>$R = 1 \text{ k}\Omega \text{ (typ.)}$                                                                         |

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0 V)

| PARAMETER                                    | SYMBOL             | PINS                       | RATING                         | UNIT |
|----------------------------------------------|--------------------|----------------------------|--------------------------------|------|
| Supply Voltage                               | V <sub>DD</sub>    |                            | – 0.3 to 7                     | V    |
| Input Voltage                                | V <sub>IN</sub>    |                            | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output Voltage                               | V <sub>OUT1</sub>  | Except sink open drain pin | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
|                                              | V <sub>OUT2</sub>  | Ports P1, P2, R7 to R9     | – 0.3 to 10                    |      |
|                                              | V <sub>OUT3</sub>  | Port R4 (Analog inputs)    | – 0.3 to V <sub>DD</sub> + 0.3 |      |
| Output Current (Per 1 pin)                   | I <sub>OUT1</sub>  | Ports P1, P2               | 30                             | mA   |
|                                              | I <sub>OUT2</sub>  | Ports R4, R7 to R9         | 3.2                            |      |
| Output Current (Total)                       | ΣI <sub>OUT1</sub> | Ports P1, P2               | 120                            | mA   |
| Power Dissipation [T <sub>opr</sub> = 70 °C] | PD                 |                            | 600                            | mW   |
| Soldering Temperature (time)                 | T <sub>sld</sub>   |                            | 260 (10 s)                     | °C   |
| Storage Temperature                          | T <sub>stg</sub>   |                            | – 55 to 125                    | °C   |
| Operating Temperature                        | T <sub>opr</sub>   |                            | – 30 to 70                     | °C   |

## RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER          | SYMBOL           | PINS                    | CONDITIONS              | Min.                   | Max.                   | UNIT |
|--------------------|------------------|-------------------------|-------------------------|------------------------|------------------------|------|
| Supply Voltage     | V <sub>DD</sub>  |                         | In the Normal mode      | 2.7                    | 6.0                    | V    |
|                    |                  |                         | In the HOLD mode        | 2.0                    |                        |      |
| Input High Voltage | V <sub>IH1</sub> | Except Hysteresis Input | V <sub>DD</sub> ≥ 4.5 V | V <sub>DD</sub> × 0.7  | V <sub>DD</sub>        | V    |
|                    | V <sub>IH2</sub> | Hysteresis Input        |                         | V <sub>DD</sub> × 0.75 |                        |      |
|                    | V <sub>IH3</sub> |                         | V <sub>DD</sub> < 4.5 V | V <sub>DD</sub> × 0.9  |                        |      |
| Input Low Voltage  | V <sub>IL1</sub> | Except Hysteresis Input | V <sub>DD</sub> ≥ 4.5 V | 0                      | V <sub>DD</sub> × 0.3  | V    |
|                    | V <sub>IL2</sub> | Hysteresis Input        |                         |                        | V <sub>DD</sub> × 0.25 |      |
|                    | V <sub>IL3</sub> |                         | V <sub>DD</sub> < 4.5 V |                        | V <sub>DD</sub> × 0.1  |      |
| Clock Frequency    | f <sub>c</sub>   |                         |                         | 0.4                    | 4.2                    | MHz  |

Note. Input voltage V<sub>IH3</sub>, V<sub>IL3</sub> : in the HOLD mode

## D.C. CHARACTERISTICS

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER                              | SYMBOL           | PINS                           | CONDITIONS                                                | Min. | Typ. | Max. | UNIT |
|----------------------------------------|------------------|--------------------------------|-----------------------------------------------------------|------|------|------|------|
| Hysteresis Voltage                     | V <sub>HS</sub>  | Hysteresis Input               |                                                           | —    | 0.7  | —    | V    |
| Input Current                          | I <sub>IN1</sub> | Port K0, TEST,<br>RESET, HOLD  | V <sub>DD</sub> = 5.5 V,<br>V <sub>IN</sub> = 5.5 V / 0 V | —    | —    | ± 2  | μA   |
|                                        | I <sub>IN2</sub> | Ports R (open drain)           |                                                           |      |      |      |      |
| Low Input Current                      | I <sub>IL</sub>  | Ports R (push-pull)            | V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V          | —    | —    | – 2  | mA   |
| Input Resistance                       | R <sub>IN1</sub> | Port K0 with pull-up/pull-down |                                                           | 30   | 70   | 150  | kΩ   |
|                                        | R <sub>IN2</sub> | RESET                          |                                                           | 100  | 220  | 450  |      |
| Output Leakage Current                 | I <sub>LO</sub>  | Ports R (open drain)           | V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V         | —    | —    | 2    | μA   |
| Output Low Voltage                     | V <sub>OL2</sub> | Except XOUT, ports P           | V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA         | —    | —    | 0.4  | V    |
| Low Output Current                     | I <sub>OL1</sub> | Ports P1, P2                   | V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V          | —    | 20   | —    | mA   |
| Supply Current<br>(in the Normal mode) | I <sub>DD</sub>  |                                | V <sub>DD</sub> = 5.5 V, f <sub>c</sub> = 4 MHz           | —    | 3    | 6    | mA   |
| Supply Current<br>(in the HOLD mode)   | I <sub>DDH</sub> |                                | V <sub>DD</sub> = 5.5 V                                   | —    | 0.5  | 10   | μA   |

Note 1. Typ. values show those at T<sub>opr</sub> = 25 °C, V<sub>DD</sub> = 5 V.

Note 2. Input Current I<sub>IN1</sub> ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I<sub>DD</sub>, I<sub>DDH</sub> ; V<sub>IN</sub> = 5.3 V / 0.2 V

The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

## A / D CONVERSION CHARACTERISTICS

(T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER                      | SYMBOL             | CONDITIONS                                                                      | Min.                  | Typ. | Max.              | UNIT |
|--------------------------------|--------------------|---------------------------------------------------------------------------------|-----------------------|------|-------------------|------|
| Analog Reference Voltage       | V <sub>AREF</sub>  |                                                                                 | V <sub>DD</sub> – 1.5 | —    | V <sub>DD</sub>   | V    |
| Analog Reference Voltage Range | ΔV <sub>AREF</sub> | V <sub>AREF</sub> – V <sub>SS</sub>                                             | 3.0                   | —    | —                 | V    |
| Analog Input Voltage           | V <sub>AIN</sub>   |                                                                                 | V <sub>SS</sub>       | —    | V <sub>AREF</sub> | V    |
| Analog Supply current          | I <sub>REF</sub>   |                                                                                 | —                     | 0.5  | 1.0               | mA   |
| Nonlinearity Error             |                    | V <sub>DD</sub> = 5.0 V, V <sub>SS</sub> = 0.0 V<br>V <sub>AREF</sub> = 5.000 V | —                     | —    | ± 1               | LSB  |
| Zero Point Error               |                    |                                                                                 | —                     | —    | ± 1               |      |
| Full Scale Error               |                    |                                                                                 | —                     | —    | ± 1               |      |
| Total Error                    |                    |                                                                                 | —                     | —    | ± 2               |      |

A. C. CHARACTERISTICS

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 6.0 V, T<sub>opr</sub> = - 30 to 70 °C)

| PARAMETER                    | SYMBOL           | CONDITIONS             | Min. | Typ. | Max. | UNIT |
|------------------------------|------------------|------------------------|------|------|------|------|
| Instruction Cycle Time       | t <sub>cy</sub>  |                        | 1.9  | —    | 20   | μs   |
| High level Clock pulse Width | t <sub>WCH</sub> | External clock mode    | 80   | —    | —    | ns   |
| Low level Clock pulse Width  | t <sub>WCL</sub> |                        |      |      |      |      |
| A/D Sampling Time            | t <sub>AIN</sub> | f <sub>c</sub> = 4 MHz | —    | 4    | —    | μs   |

RECOMMENDED OSCILLATING CONDITIONS

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 6.0 V, T<sub>opr</sub> = - 30 to 70 °C)

(1) 4 MHz

Ceramic Resonator

CSA4. 00MG (MURATA)

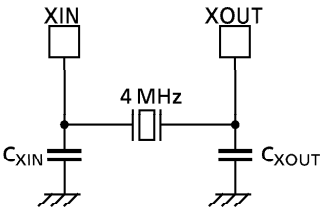
C<sub>XIN</sub> = C<sub>XOUT</sub> = 30 pF

KBR-4. 00MS (KYOCERA)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 30 pF

Crystal Oscillator

204B-6F 4. 0000 (TOYOCOM) C<sub>XIN</sub> = C<sub>XOUT</sub> = 20 pF



(2) 400 kHz

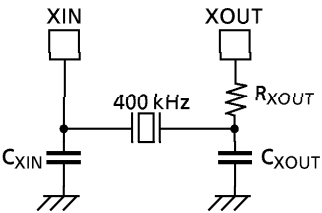
Ceramic Resonator

CSB400B (MURATA)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 220 pF, R<sub>XOUT</sub> = 6.8 kΩ

KBR-400B (KYOCERA)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 100 pF, R<sub>XOUT</sub> = 10 kΩ



## TYPICAL CHARACTERISTICS

