CMOS 4-BIT MICROCONTROLLER

TMP47C453AN
TMP47C453AF

The 47C453A is a high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series. And the 47C453A has a built-in largecapacity RAM for repertory dial and DTMF generator, which is suitable for application in telephones. The 47C453A is also capable of operation with low voltage such as those supplied by telephone line.

PART No.	ROM	RAM	PACKAGE	OTP
TMP47C453AN	4096 × 8-bit	768 × 4-bit	SDIP42-P-600-1.78	TMP47P453VN
TMP47C453AF			QFP44-P-1414-0.80D	TMP47P453VF

FEATURES

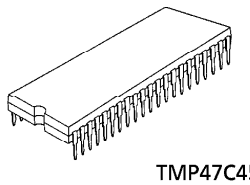
◆4-bit single chip microcomputer
◆Instruction execution time : 8.3μs (at 960kHz)
◆Low voltage operation : 2.2V min.
◆90 basic instructions
◆Table look-up instructions
◆Subroutine nesting : 15 levels max.
◆6 interrupt sources (External : 2, Internal : 4)
All sources have independent latches each, and multiple interrupt control is available
◆I/O port (35 pins)
- Input 2ports 5pins
- I/O 7ports 27pins
- Output 1port 3pins

◆Interval Timer
◆Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode
◆Serial Interface with 4-bit buffer
External/internal clock, leading/trailing edge shift mode
◆DTMF (Dual Tone Multi Frequency) output
- DTMF output with one instruction
- Single tone output function

◆RAM for repertory dial : 768 × 4-bit max.
◆BEEP output function
◆Warm-Start funtion
◆Hold function
- Battery/Capacitor back-up
- Hold function controlled by port K0

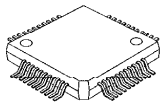
◆Real Time Emulatur : BM47C453A

SDIP42-P-600-1.78



TMP47C453AN
TMP47P453VN

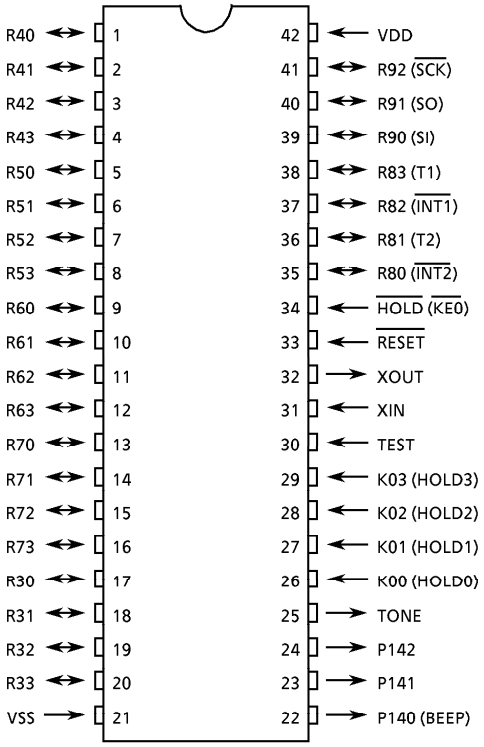
QFP44-P-1414-0.80D



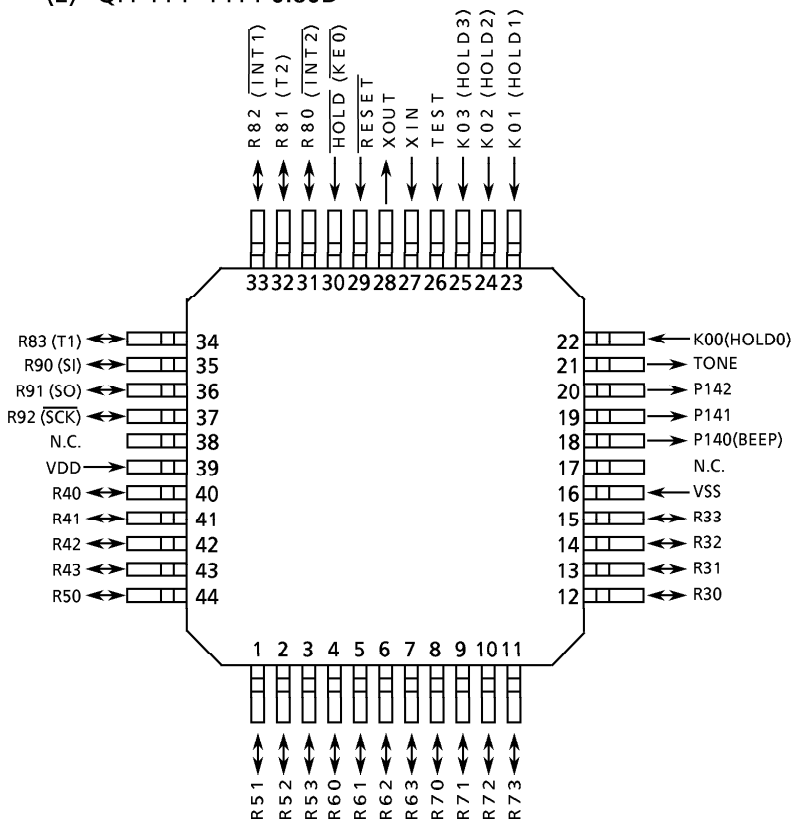
TMP47C453AF
TMP47P453VF

PIN ASSIGNMENTS (TOP VIEW)

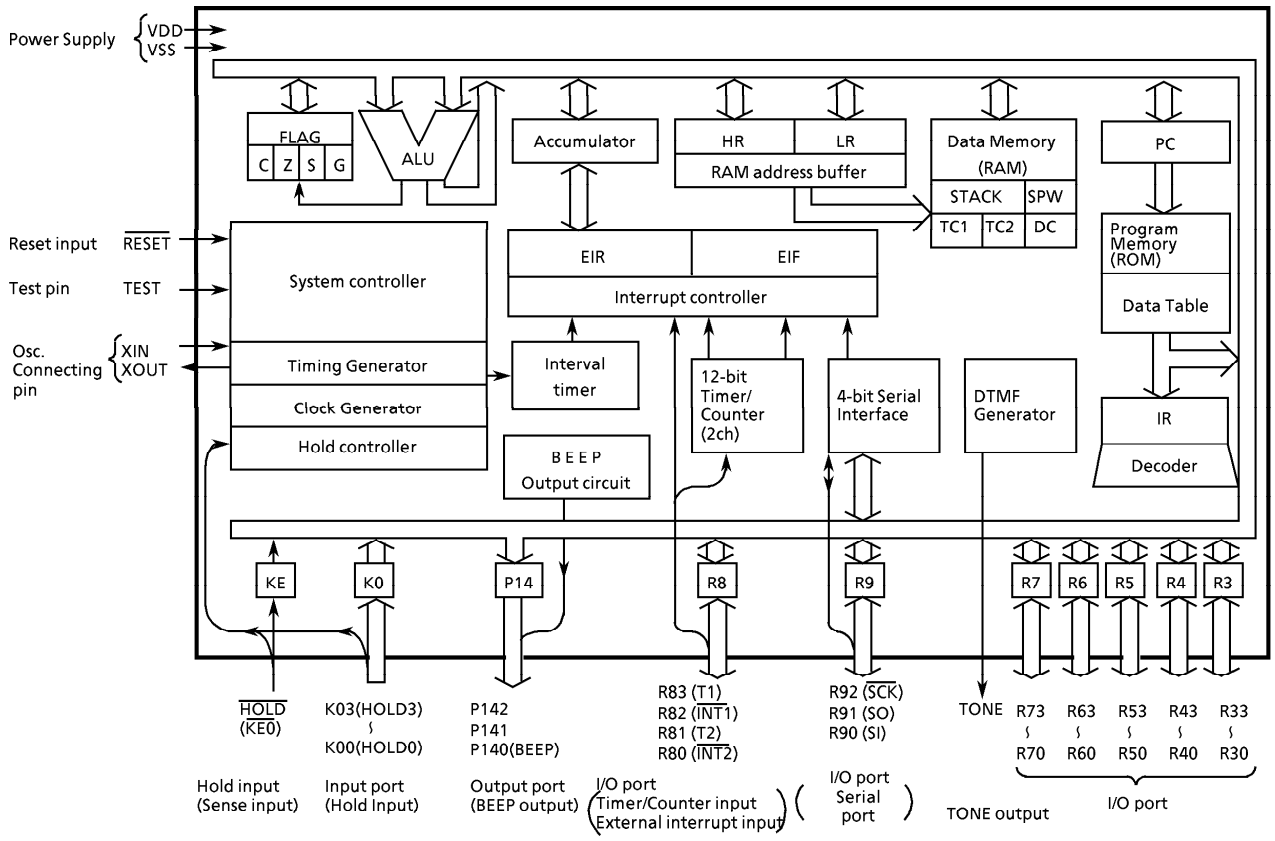
(1) SDIP42-P-600-1.78



(2) QFP44-P-1414-0.80D



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) - K00 (HOLD0)	Input (Input)	4-bit input port	Hold request/release signal input (Active "H")
R33 - R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 - R40			
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P142 - P141	Output	3-bit output port with latch	
P140(BEEP)	Output (Output)		BEEP Output
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 2.2V to 6.0V	
VSS		0V(GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C453A, the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C452B. The technical data sheets for the 47C452B shall also be reffered to.

1. SYSTEM CONFIGURATION

(1) CPU Core Function
Except for the control of a primary factor for HOLD operating Mode, the functions are the same as those of the 47C655/855.

(2) Peripheral Hardware Functions

① I/O Port
② Interval Timer
③ Timer/Counter
④ DTMF Generator
⑤ BEEP Output Circuit
⑥ Warm-Start Function
⑦ Serial Interface

The following are explanations of functions ②, ③ and ⑤ - ⑦ which have been added to the 47C453A or which are different from those of the 47C452B, and the HOLD Operating Mode Controller.

2. CPU CORE FUNCTIONS

2.1 DATA MEMORY

The 47C858 has a total of 768 × 4bits of data memory. This memory is same as the data memory built into the 47C452B, so refer to the technical data sheets for the 47C452B for an explanation of the operation.

2.2 HOLD Operating Mode

The HOLD feature stops the system and holds the system's internal states active before stop with a low power. The HOLD operation is controlled by the $\overline{\text{HOLD}}$ pin and K0 port inputs. The $\overline{\text{HOLD}}$ pin and K0 port input state can be known by the status registers (IP0E). The $\overline{\text{HOLD}}$ pin is shared with the $\overline{\text{KE0}}$ pin.

2.2.1 HOLD Operation control circuit

Configuration of HOLD operation circuit is shown in Figure 2-1.

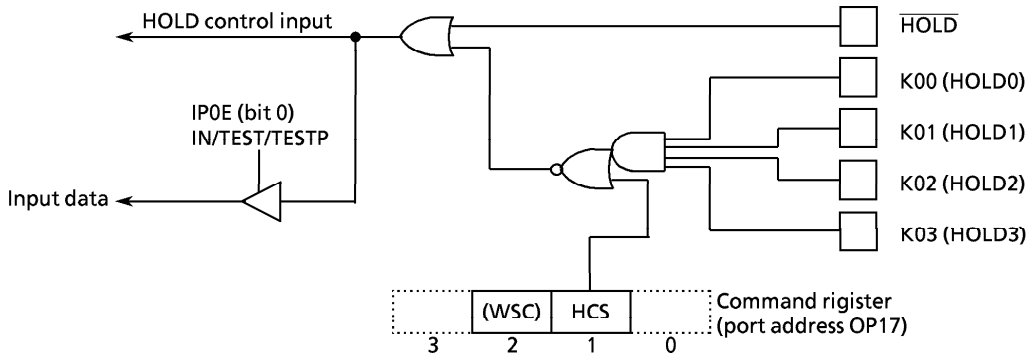


Figure 2-1. Hold control circuit

The 47C453A has a $\overline{\text{HOLD}}$ pin and K0 port as HOLD control input. Therefore, in the case of using K0 port for key inputs, the HOLD operation can be released by key inputs. HOLD control by K0 port input can be inhibited by HOLD control input select command register. (bit 1 of OP17)

HOLD control input select command register (port address OP17)

3	2	1	0
	(WSC)	HCS	

(Initial value *10*)

HCS	Selects HOLD control input

0 : Controls HOLD operation by $\overline{\text{HOLD}}$ pin and K0 port inputs
1 : Controls HOLD operation by $\overline{\text{HOLD}}$ pin input

Figure 2-2. Hold control input select command register

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C453A has 10 ports (35 pins) each as follows :

①	K0	;	4-bit input (shared by hold request/release signal input)
②	R3	;	4-bit input/output
③	R4, R5, R6, R7	;	4-bit input/output
④	R8	;	4-bit input/output (shared by external interrupt input and timer/counter input)
⑤	R9	;	3-bit input/output (shared by serial port)
⑥	P14	;	3-bit output (P140 is shared by BEEP output)
⑦	KE	;	1-bit sense input (shared by hold request/release signal input)

The 47C453A does not have the port P1 and P2.
Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03-K00)

The 4-bit input port with pull-up resistors, shared by hold request/release signal input.

Port K0 (Port address IP00)

3	2	1	0
K03 (HOLD3)	K02 (HOLD2)	K01 (HOLD1)	K00 (HOLD0)

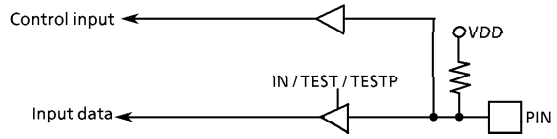


Figure 3-1. Port K0

(2) Port R3 (R33-R30)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R3 (Port address OP03 / IP03)

3	2	1	0
R33	R32	R31	R30

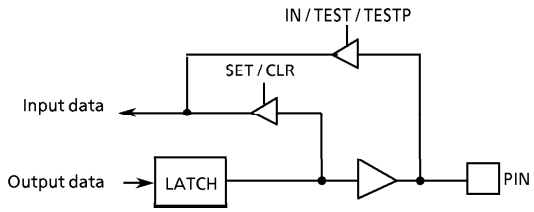


Figure 3-2. Port R3

(3) Port P14 (P142-P140)

The 3-bit output port with latch. The latch is initialized to "1" during reset. The pin P140 is shared by the BEEP output. When used as the BEEP output, the latch must be set to "1".

Port P14 (Port address OP14)

3	2	1	0
	P142	P141	P140 (BEEP)

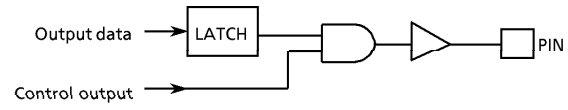


Figure 3-3. Port P14

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 Input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ (Note2)	○	○	–
02	COLUMN register	COLUMN register	○	○	○	○	○	○	–
03	R3 Input port	R3 Output port	○	○	○	–	○	○	–
04	R4 Input port	R4 Output port	○	○	○	–	○	○	○
05	R5 Input port	R5 Output port	○	○	○	–	○	○	○
06	R6 Input port	R6 Output port	○	○	○	–	○	○	○
07	R7 Input port	R7 Output port	○	○	○	–	○	○	○
08	R8 Input port	R8 Output port	○	○	○	–	○	○	–
09	R9 Input port	R9 Output port	○	○	○	–	○	○	–
0A	RAM address register	RAM address register	○	○	○	–	○	○	–
0B	RAM address register	RAM address register	○	○	○	–	○	○	–
0C	RAM data buffer register	RAM data buffer register	○	○	○	–	○	○	–
0D	RAM command register	RAM command register	○	○	○	–	–	○	–
0E	SIO, Hold status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transfer buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	RAM address register	–	○	–	–	–	–	–
13	Undefined	BEEP output control	–	○	–	–	–	–	–
14	Undefined	P14 Output port	–	○	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	HOLD input / worm start control	–	○	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. "——" means the reserved state. Unavailable for the user program.

Note 2. The 5-bit to 8-bit data conversion instruction [OUT @ HL] , automatic access to ROW register and COLUMN register.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.2 Interval Timer Interrupt (ITMR)

The interval timer can be used to generate an interrupt with a fixed frequency. For an interval timer interrupt, one of 4 frequencies can be selected by command. The command register (OP19) is initialized to "0" during reset. An interval timer interrupt is generated at the first rising edge of the binary counters output after the command has been set. The interval timer is not cleared by command, so that the first interrupt may occur earlier than the preset interrupt period.

Example: To set the interval timer interrupt frequency to $fc/2^{11}$ [Hz].

```
LD      A,  #0110B    ;  OP19←0110B
OUT     A,  %OP19
```

Interval Timer interrupt command register (Port address OP19)

3	2	1	0

(Initial value 0000)

Example: At fc = 960kHZ

00**	: Interrupt disabled			
0100	: Interrupt frequency	$fc / 2^9$ [Hz]	···	1875 [Hz]
0101	: Interrupt frequency	$fc / 2^{10}$	···	937.5
0110	: Interrupt frequency	$fc / 2^{11}$	···	468.8
0111	: Interrupt frequency	$fc / 2^{12}$	···	234.4
1***	: Reserved			

*(Note 1) * ; don't care*

(Note 2) fc ; Basic clock frequency [Hz]

Figure 3-4. Interval Timer Interrupt Command Register

3.3 Serial Interface

When operating using the internal clock, $fc/2^6$ [Hz] is used as the serial clock. Consequently, when operating at fc = 960kHz, the maximum transfer rate is 15000bit/ s. When the reading and writing of serial data cannot follow this clock rate, the serial clock is automatically stopped and the next shift operation stands by untill the processing is completed.

External clock can be used in the same way as for the 47C452B. The serial interface cannot be used in the SLOW operating mode.

3.4 Timer/Counter

The following operating frequencies differ from those of the 47C452B.

(1) Internal pulse rate

The intrnal pulse rates shown in Table 3-2 can be selected by setting the values of the lower 2 bits of the TC1 and TC2 control command registers (OP1C, OP1D).

The values of lower 2 bits (bit1, 0)	Internal pulse rate	Max. setting time	At fc = 960kHz	
			Internal pulse rate	Max. setting time
00	$fc / 2^9$ [Hz]	$2^{21} / fc$ [s]	1875 [Hz]	2.2 [s]
01	$fc / 2^{13}$	$2^{25} / fc$	117.2	35
10	$fc / 2^{17}$	$2^{29} / fc$	7.3	559.2
11	$fc / 2^{21}$	$2^{33} / fc$	0.46	8947.8

Table 3-2. Internal Pulse Rate and Max. setting time

3.5 BEEP Output Circuit

BEEP output circuit generates square wave in the audible frequency range. This circuit can drive the key input confirmation tone generator circuit for telephone applications.

BEEP output is from the P140 (BEEP) pin. This pin is for both P140 output and BEEP output. Set the P140 output latch to "1" for BEEP output.

3.5.1 Configuration of BEEP Output Circuit

Figure 3-5 shows configuration of the BEEP output circuit. The clock pulse of BEEP output circuit is supplied by an interval timer. BEEP output is controlled by frequency selection and output enable/disable setting.

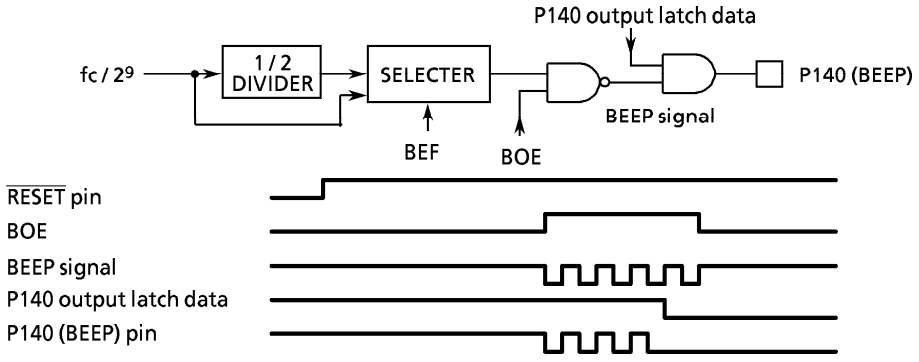


Figure 3-5. BEEP Output Circuit Configuration and Timing Chart

3.5.2 Control of BEEP Output

BEEP output is controlled with the BEEP output control command register (OP13).

BEEP Output Control command register (Port address OP13)

3	2	1	0	
BOE			BEF	(Initial value 0**0)

BOE	Controls BEEP output
0:	Disable output
1:	Enable output

BEF	Selects BEEP output frequency	Example: At fc = 960kHz
0:	fc / 512 [Hz] ····· 1875 [Hz]	
1:	fc / 1024 ····· 937.5	

Figure 3-6. BEEP Output Control Command Register

3.6 Warm-Start Function

The 47C453A has Warm-start function which is performed reset-operation by setting a command register (OP17).

Warm-Start control regiter (port address OP17)

3	2	1	0	
	WSC	(HCS)		(Initial value *10*)

WSC	Warm-Start control
0:	Warm-Start operation
1:	Warm-Start inhibit

Figure 3-7. Warm-Start Control Register

3.7 DTMF Generator

The 47C453A has a built-in DTMF generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF ; Dual Tone Multi Frequency)

3.7.1 Configuration of DTMF Generator

Figure 3-4 shows configuration of the DTMF generator. The 47C453A generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

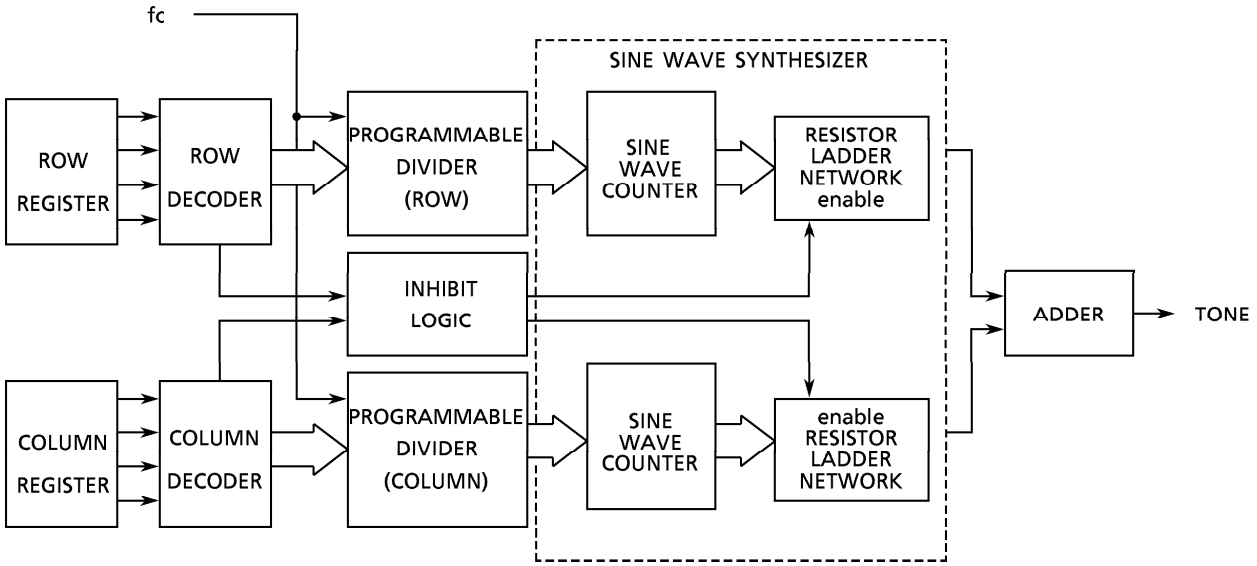


Figure 3-8. Configuration of DTMF Generator

3.7.2 Control of DTMF Generator

Tone output is controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02). And single tone is controlled by TONE command register (OP0D/IP0D). ROW register and COLUMN register are initialized to "0" during reset.

TONE command register (Port address OP0D/IP0D)

3	2	1	0
STE		(R / W)	(CE)

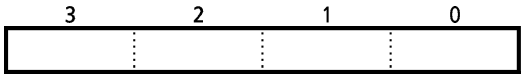
(Initial value **00)

STE	Controls single tone output
0 :	Disable mode of single tone output
1 :	Enable mode of single tone output

Note 1. **; don't care*
Note 2. *When read STE bit, "1" is always read.*

Figure 3-9. TONE command register

ROW register (Port address OP01 / IP01)

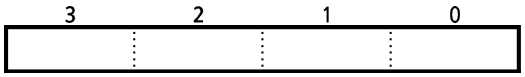


(Initial value 0000)

Selects ROW tone frequency

0001 : Outputs 697.7Hz single tone
0010 : Outputs 769.2Hz single tone
0100 : Outputs 857.1Hz single tone
1000 : Outputs 937.5Hz single tone

COLUMN register (Port address OP02 / IP02)



(Initial value 0000)

Selects COLUMN tone frequency

0001 : Outputs 1212.1Hz single tone
0010 : Outputs 1333.3Hz single tone
0100 : Outputs 1481.5Hz single tone
1000 : Outputs 1621.6Hz single tone

Figure 3-10. ROW, COLUMN Register

Tones are outputted by loading the frequency selection codes shown in Figure 3-6 into the ROW and COLUMN registers. In the enable mode of single tone output and either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be outputted, by loading an ineffective code into the register. When both the registers are enabled, dual tone can be outputted. In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted. At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C453A has no tone output signal.
The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data go to the COLUMN register and the lower 4 bits go to the ROW register) at the same time, and DTMF signal is outputted without single tone output.

Example 1 : To output 1481.5Hz single tone

```
OUT     #8,%OP0D ;  Sets the enable mode of single tone output.
OUT     #0,%OP01 ;  Sets an ineffective code into ROW register.
OUT     #4,%OP02 ;  Sets data "4" into COLUMN register
```

Example 2 : 8 bits data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM address 90_H are read from the ROM, frequency selection codes are loaded into ROW and COLUMN registers, and dual tone is outputted.

```
LD      HL,#90H  ;  HL←90H (Sets the address of the data memory)
OUTB    @HL      ;  Sets the ROM data into the ROW and COLUMN register.
```

Table 3-3 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-4 shows the deviation between the 47C453A tone output frequency and standard frequency.

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01/IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit : Hz

Table 3-3. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	– 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	– 0.37

COLUMN Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	– 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	– 0.70

Table 3-4. Tone output frequencies and Deviation from standard

3.7.3 Test mode for tone output

The 47C453A includes a test mode for checking tone output waveforms. Tones can be outputted by the curcuit shown in Figure 3-11. ROW data are inputted from the R6 port and COLUMN data are inputted from the R3 port, and any desired single or dual tones can be outputted by setting the frequency selection codes shown in Figure 3-10. Figure 3-12 shows a single tone waveform and Figure 3-13 shows a dual tone waveform.

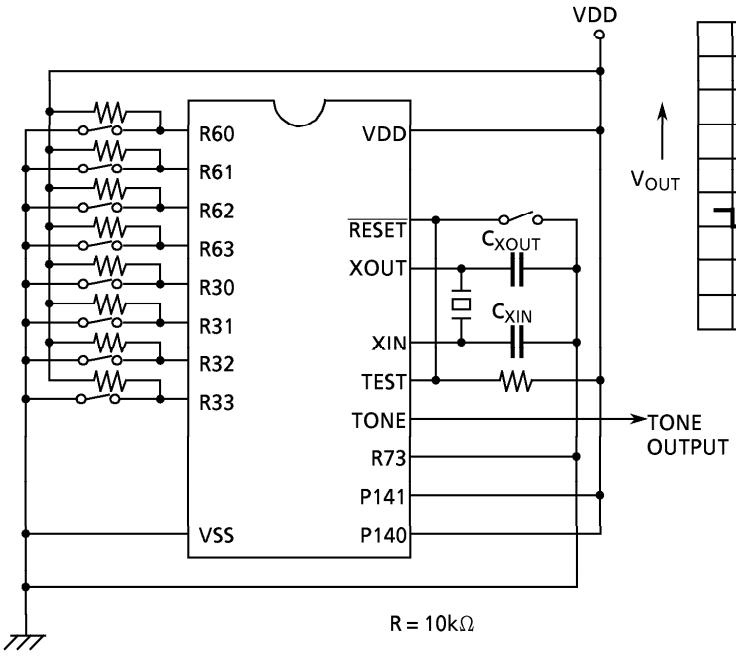


Figure 3-11. Tone test circuit

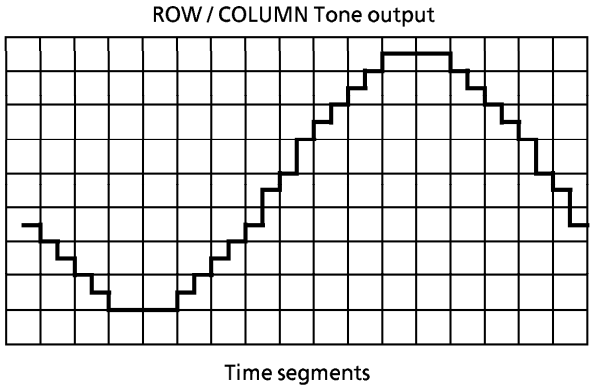


Figure 3-12. Single tone waveform

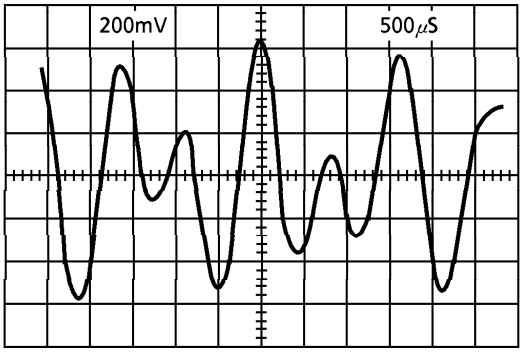
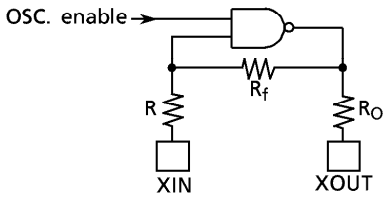
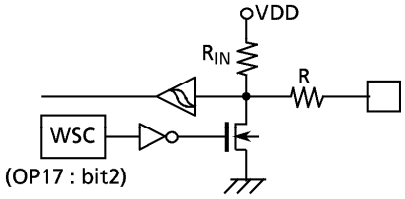
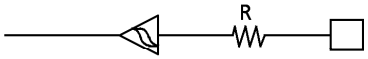
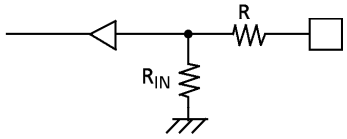


Figure 3-13. Dual tone waveform

INPUT/OUTPUT CIRCUITRY

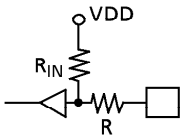
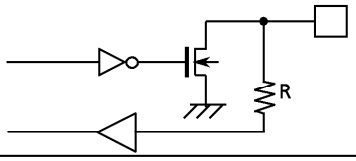
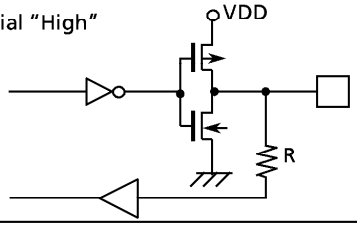
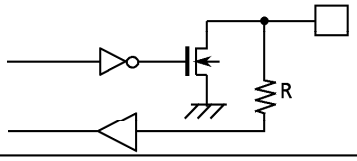
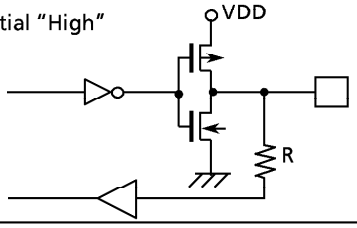
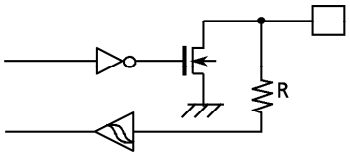
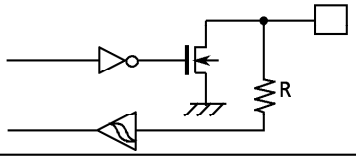
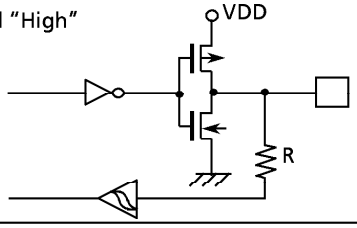
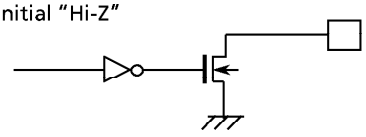
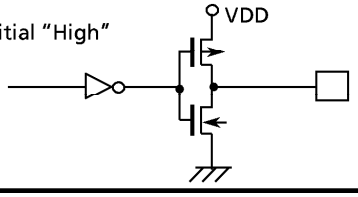
(1) Control pins

The input/output circuitries of the 47C452B control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1kΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2kΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Pull-up resistor R_{IN} = 220kΩ (typ.) R = 1kΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sense input) R = 1kΩ (typ.)
TEST	Input		Pull-down resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 47C453A I/O ports are shown as below, any one of the circuitries can be chosen by a code (WB, WE, WH) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY (CODE)	REMARKS
K0	Input		Pull-up resister R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)
R3 R4 R5 R6	I/O	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output R = 1kΩ (typ.)
R7	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output R = 1kΩ (typ.)
R8	I/O	Initial "Hi-Z" 	Sink open drain Hysteresis input R = 1kΩ (typ.)
R9	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output Hysteresis input R = 1kΩ (typ.)
P14	Output	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	VOUT2	Sink open drain pin	– 0.3 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 60°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	Ts_{tg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 60	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.2	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			960		kHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports P, R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Port R (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Supply Current (in the Normal mode)	I_{DD}		Except TONE generating V_{DD} = 2.2V fc = 480kHz	—	0.3	0.5	mA
	I_{DDT}		TONE generating V_{DD} = 2.2 V fc = 480kHz	—	0.6	1.2	
Supply Current (in the HOLD mode)	I_{DDT}		V_{DD} = 5.5V	—	0.5	10	μA
			V_{DD} = 2.2V, Topr = 25°C	—	—	0.5	

Note 1. Typ.values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resister is not included, when the pull-up/pull-down resister is contained.

Note 3. Supply Current : V_{IN} = 2.0V / 0.2V

The K0 port is opened when the pull-up/pull-down resister is contained.

The Voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

TONE OUTPUT CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10kΩ, V_{DD} = 2.2V	125	185	250	mVrms
Pre-Emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL /ROW)	1	2	3	dB
Output Distortion	DIS		—	—	10	%
Frequency Stability	△f	Except error of osc. frequency	—	—	0.7	%

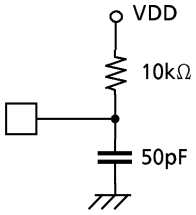
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

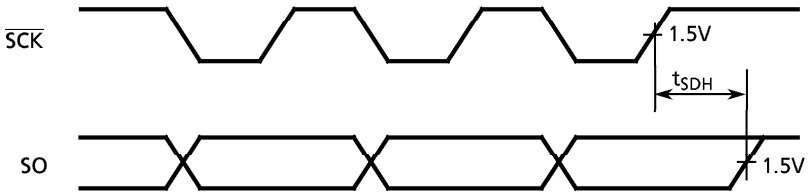
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		16.7			μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$-300	—	—	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)

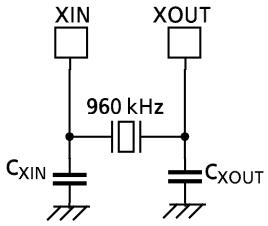


RECOMMENDED OSCILLATING CONDITION

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

960kHz
Ceramic Resonator

CSB960J916	(MURATA)	$C_{XIN} = C_{XOUT}$ = 100pF
KBR-960F6	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 33pF
KBR-960F7	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100pF



TYPICAL CHARACTERISTICS