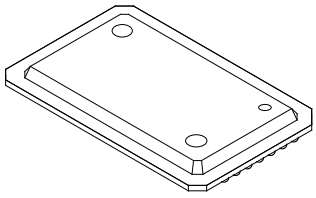
SONY

CXK77B3611AGB -5/6

High Speed Bi-CMOS Synchronous Static RAM

Preliminary

119 pin BGA (Plastic)



Description

The CXK77B3611AGB-5/6 is a high speed 1M bit Bi-CMOS synchronous static RAM organized as 32768 words by 36 bits. This SRAM integrates input registers, high speed SRAM and write buffer onto a single monolithic IC and features the delayed write system to reduce the dead cycles.

Features

- Fast cycle time (Cycle) (Frequency)
  CXK77B3611AGB-5 5ns 200MHz
  -6 6ns 167MHz
- Inputs and outputs are GTL/HSTL compatible
- Controlled Impedance Driver
- Single 3.3V power supply: 3.3V±0.15V
- Byte-write possible
- $\overline{OE}$ asynchronization
- JTAG test circuit
- Package 119TBGA
- 4 kinds of synchronous operation mode
  Register-Register mode (R-R mode)
  Register-Flow Thru mode (R-F mode)
  Register-Latch mode (R-L mode)
  Dual clock mode (D-C mode)

Function

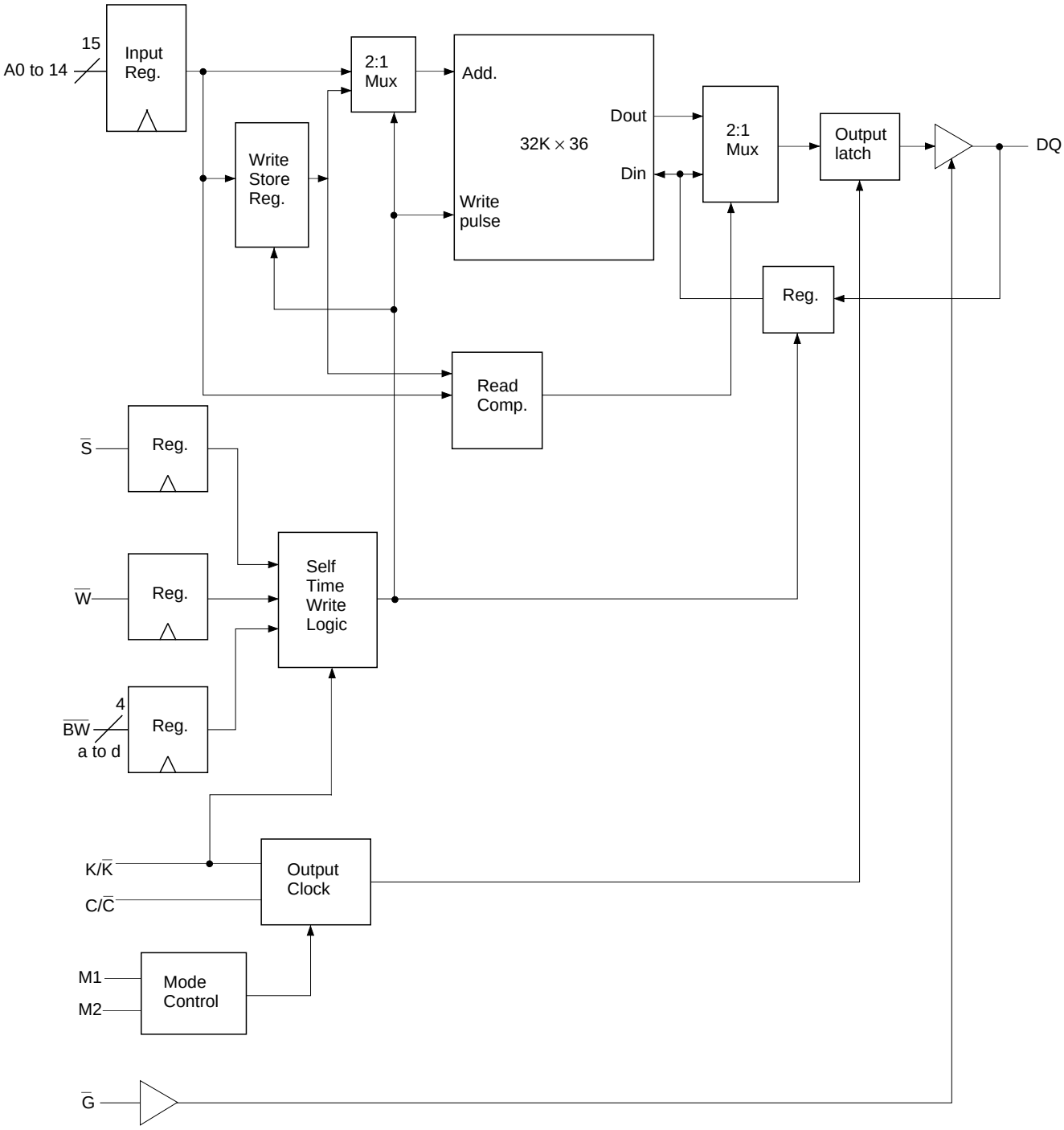
32768 word x 36bit High Speed Bi-CMOS Synchronous SRAM

Structure

Silicon gate Bi-CMOS IC

PE96812

Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7
A	$V_{DD}Q$	A	A	NC	A	A	$V_{DD}Q$
B	NC	NC	NC	NC	NC	NC	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{S}$	V_{SS}	DQb	DQb
F	$V_{DD}Q$	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	$V_{DD}Q$
G	DQc	DQc	$\overline{BW}$c	$\overline{C}$	$\overline{BW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	C	V_{SS}	DQb	DQb
J	$V_{DD}Q$	V_{DD}	VREF	V_{DD}	VREF	V_{DD}	$V_{DD}Q$
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BW}$d	$\overline{K}$	$\overline{BW}$a	DQa	DQa
M	$V_{DD}Q$	DQd	V_{SS}	$\overline{W}$	V_{SS}	DQa	$V_{DD}Q$
N	DQd	DQd	V_{SS}	A	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	A	V_{SS}	DQa	DQa
R	NC	A	M1	V_{DD}	M2	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	$V_{DD}Q$	TMS	TDI	TCK	TDO	NC	$V_{DD}Q$

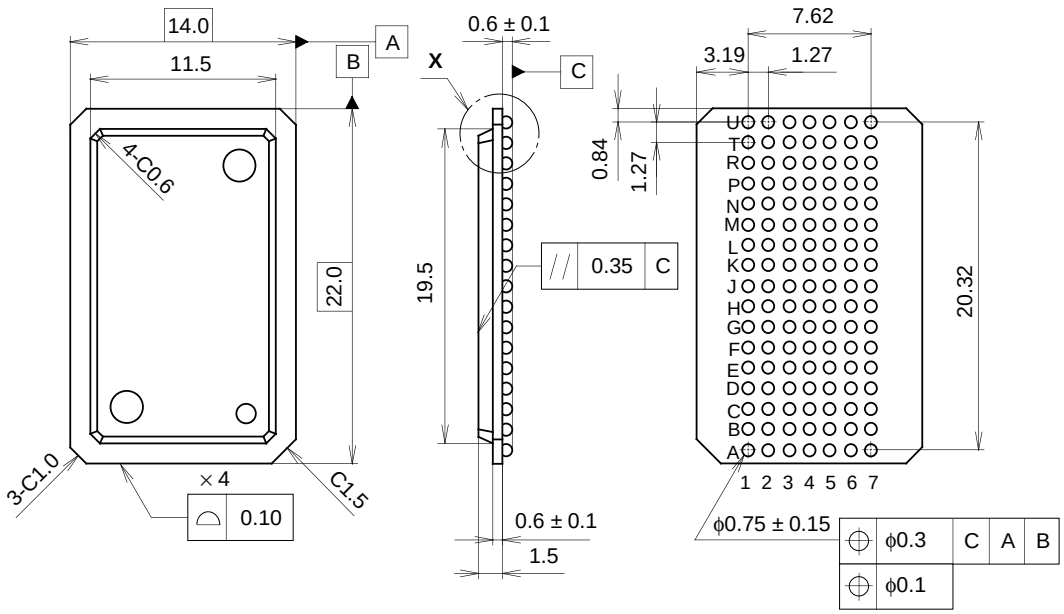
Pin Description

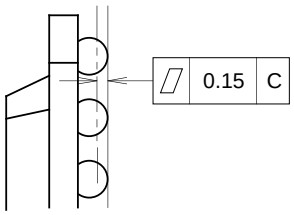
Symbol	Description	Symbol	Description	Symbol	Description
A	Address Input	$\overline{BWX}$	Byte Write Enable (a to d)	V_{DD}	+3.3V power supply
DQx	Data I/O in byte (a to d)	$\overline{S}$	Chip Select	$V_{DD}Q$	Output power supply
K	Positive Clock	$\overline{G}$	Asyn Output Enable	V_{SS}	Ground
$\overline{K}$	Negative Clock	ZZ	Sleep Mode Select	M1, M2	Mode Select
C	Output Positive Clock(*)	TCK	JTAG Clock	ZQ	Output Impedance Control
$\overline{C}$	Output Negative Clock(*)	TMS	JTAG Mode Select	NC	No Connect
VREF	Input Reference	TDI	JTAG Data In		
$\overline{W}$	Write Enable	TDO	JTAG Data Out		

(*) These pins should be tied to V_{DD} or V_{SS} except D-C mode.

Package Outline Unit: mm

119 TERMINAL BGA (PLASTIC)





DETAIL **X**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
BOARD MATERIAL	COPPER-CLAD LAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE WEIGHT	0.8g

SONY CODE	BGA-119P-01
EIAJ CODE	————
JEDEC CODE	————