

MOS FIELD EFFECT TRANSISTOR 2SK2498

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

2SK2498 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

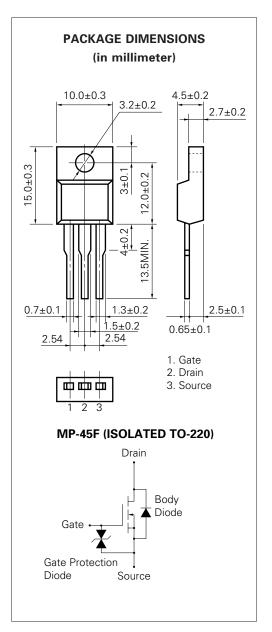
FEATURES

- Super Low On-State Resistance $R_{DS~(on)}1 \leq 9~m\Omega~(V_{GS}=10~V,~I_{D}=25~A)$ $R_{DS~(on)}2 \leq 14~m\Omega~(V_{GS}=4~V,~I_{D}=25~A)$
- Low Ciss Ciss = 3400 pF TYP.
- High Avalanche Capability Ratings
- · Isolate TO-220 Package
- · Buit-in G-S Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

| Drain to Source Voltage | Voss | 60 | V |
|--|------------------------|-------------|----|
| Gate to Source Voltage | Vgss | ±20 | ٧ |
| Drain Current (DC) | I _{D(DC)} | ±50 | Α |
| Drain Current (pulse)* | I _D (pulse) | ±200 | Α |
| Total Power Dissipation (Tc = 25 °C) | P _{T1} | 35 | W |
| Total Power Dissipation (T _A = 25 °C) | P _{T2} | 2.0 | W |
| Channel Temperature | T_ch | 150 | °C |
| Storage Temperature | T _{stg} - | -55 to +150 | °C |
| Single Avalanche Current** | las | 50 | Α |
| Single Avalanche Energy** | Eas | 250 | mJ |

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0



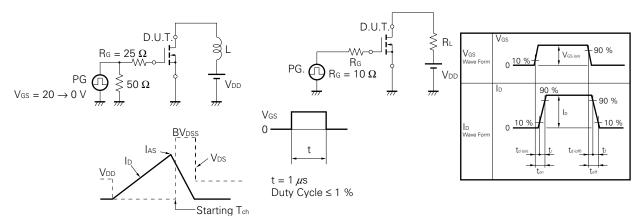


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

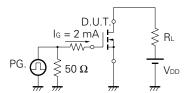
| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|--------------------------------|-----------------|------|------|------|------|---|
| Drain to Source On-Resistance | RDS (on)1 | | 7.3 | 9.0 | mΩ | Vgs = 10 V, ID = 25 A |
| | RDS (on)2 | | 11 | 14 | mΩ | Vgs = 4 V, ID = 25 A |
| Gate to Source Cutoff Voltage | VGS (off) | 1.0 | 1.5 | 2.0 | V | V _{DS} = 10 V, I _D = 1 mA |
| Forward Transfer Admittance | l yfs l | 20 | 58 | | S | V _{DS} = 10 V, I _D = 25 A |
| Drain Leakage Current | IDSS | | | 10 | μΑ | V _{DS} = 60 V, V _{GS} = 0 |
| Gate to Source Leakage Current | Igss | | | ±10 | nA | $V_{GS} = \pm 20 \text{ V, } V_{DS} = 0$ |
| Input Capacitance | Ciss | | 3400 | | pF | V _{DS} = 10 V |
| Output Capacitance | Coss | | 1600 | | pF | Vgs = 0 |
| Reverse Transfer Capacitance | Crss | | 770 | | pF | f = 1 MHz |
| Turn-On Delay Time | td (on) | | 55 | | ns | ID = 25 A |
| Rise Time | tr | | 360 | | ns | VGS(on) = 10 V |
| Turn-Off Delay Time | td (off) | | 480 | | ns | V _{DD} = 30 V |
| Fall Time | tf | | 360 | | ns | $R_G = 10 \Omega$ |
| Total Gate Charge | Q _G | | 152 | | nC | ID = 50 A |
| Gate to Source Charge | Qgs | | 11 | | nC | V _{DD} = 48 V |
| Gate to Drain Charge | Q _{GD} | | 60 | | nC | Vgs = 10 V |
| Body Diode Forward Voltage | VF (S-D) | | 0.92 | | V | IF = 50 A, VGS = 0 |
| Reverse Recovery Time | trr | | 105 | | ns | IF = 50 A, VGS = 0 |
| Reverse Recovery Charge | Qrr | | 265 | | μC | di/dt = 100 A/μs |

Test Circuit 1 Avalanche Capability

Test Circuit 2 Switching Time



Test Circuit 3 Gate Charge

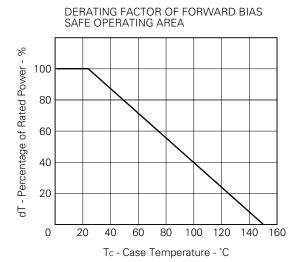


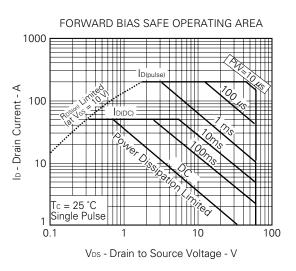
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

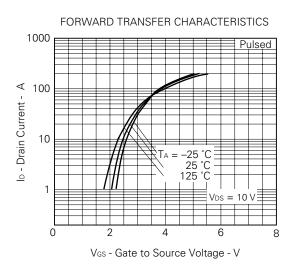
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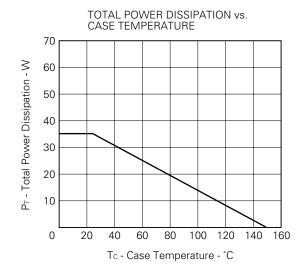


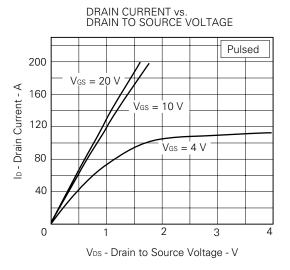
TYPICAL CHARACTERISTICS (TA = 25 °C)





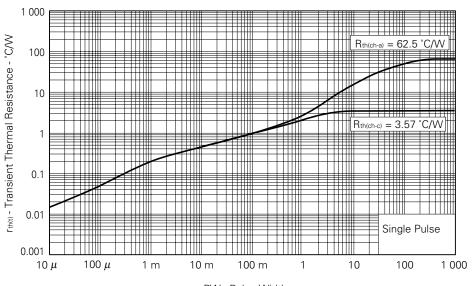






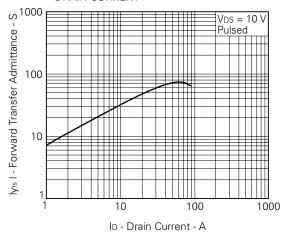
NEC

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

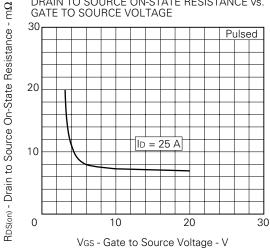


PW - Pulse Width - s

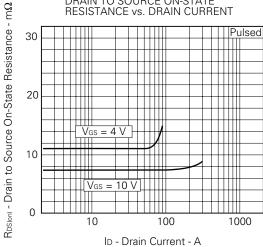




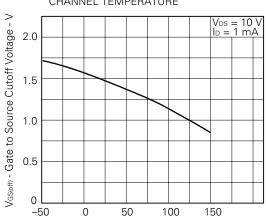




DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

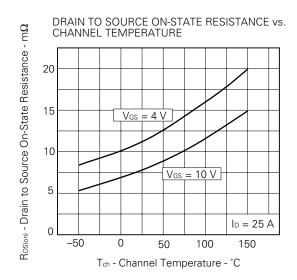


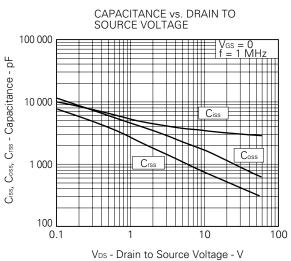
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

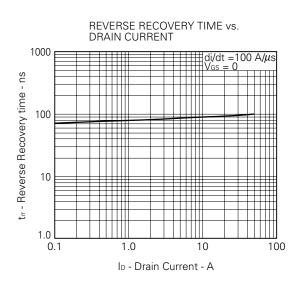


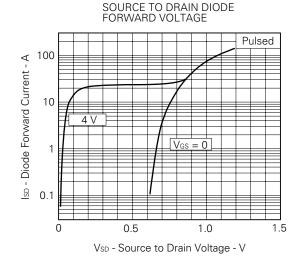
Tch - Channel Temperature - °C

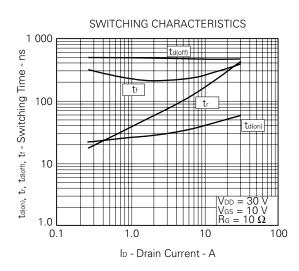


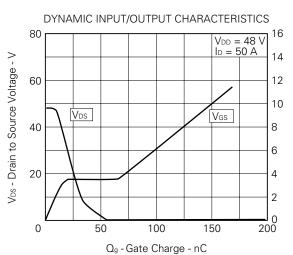




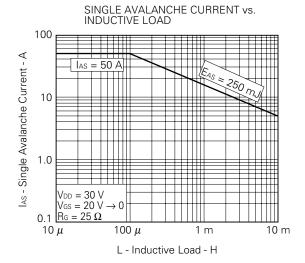


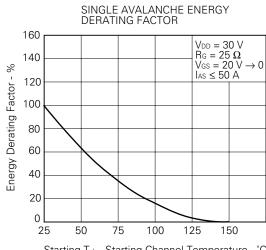














REFERENCE

| Document Name | Document No. |
|--|--------------|
| NEC semiconductor device reliability/quality control system. | TEI-1202 |
| Quality grade on NEC semiconductor devices. | IEI-1209 |
| Semiconductor device mounting technology manual. | IEI-1207 |
| Semiconductor device package manual. | IEI-1213 |
| Guide to quality assurance for semiconductor devices. | MEI-1202 |
| Semiconductor selection guide. | MF-1134 |
| Power MOS FET features and application switching power supply. | TEA-1034 |
| Application circuits using Power MOS FET. | TEA-1035 |
| Safe operating area of Power MOS FET. | TEA-1037 |

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.