Features

- **DC to DC Step Down 1.2 A, 0.9 V (Dynamically Adjustable to 0.87 V/1.1 V/1.2 V)**
- **DC to DC step Down 1.2 A, 1.2 V (Dynamically Adjustable to 1.0 V/1.1 V/1.3 V) or 1.75 V (Dynamically Adjustable 1.65 V/1.70 V/1.80 V)**
- **DC to DC Step Down 1.2 A, 1.8V (Dynamically Adjustable to 1.70 V/1.75 V/1.85 V) or 2.5 V (Dynamically Adjustable 2.3 V/2.4 V/2.6 V)**
- **DC to DC Step Up/Down 520 mA, 3.3V (Dynamically Adjustable to 3.0V/3.1V/3.4V)**
- **Dual Battery Chargers: Li+ Precharge, Fast Charge, Top-up Charge, 4.1 V (or Adjustable), Processor Tuned Algorithms**
  - **USB Trickle Charge: Precharge Flat Battery from USB Pre-enumeration, then Auto-wake of Processor at 3.8 V Battery Level**
  - **Battery Charge Select: 25 mA to 500 mA**
  - **Real-time Charge Inhibit: Allows Charge Suspend (e.g. During TX Slots)**
- **Supply Monitor of Four Power Sources: Thermistors, Temperature, DC/DC Rails, all Supplied with Out-of-regulation Threshold Detection**
- **SIM Interface: SIM / USIM, 1.8V / 3.0V Standards, Integrated TX and RX Data FIFO**
- **SPI Control Interface: Up to 13 MHz; Tuned for SA1110/PXA250/PXA255 1.2 MHz SPI, 128 8-bit Registers**
- **Power on Reset: for SA1110/PXA250/PXA255 Architectures plus Additional Sequenced System Level Resets**
- **Voltage and Temperature Supervision**
- **Calibrated Voltage Reference**
- **8-bit ADC with 5-input multiplexer**
- **Integrated Oscillator, Start-up and Self-protection Circuitry**
- **Off Power: 60 µA with External “Button Select” for Restart**
- **Applications Include: PDAs, PCMCIA Cards, SMART Phones, Pocket PCs, 3G Applications, Intel® XScale™ Powered Applications**

Description

The AT73C203 device provides an integrated solution to portable and handheld applications built around microprocessors requiring "smart" power management functions, such as PDAs, Palmtop computers, point-of-sales terminals, 3G modems, etc.

Its compact package outline and small size of external components make the AT73C203 suitable for PCMCIA card power management as well.

The AT73C203 integrates a power switch controller that, when connected to an external power switch, may be used for for automatically selecting one of four possible power sources:

- Internal battery
- External battery
- Plugtop power supply unit 5 V (PSU)
- PC Host USB supply

The power switch output (VDD-PSU line) is connected directly to external auxiliary components such as a radio or any other "current hungry" module.

The AT73C203 is also equipped with four digital rails from VDD-PSU to supply a baseband chip, a reset generator for the baseband chip, and a SPI interface to control the AT73C203 via an internal register set. The USIM interface allows the application processor to communicate with and control a USIM card. Charge control enables the application processor to charge the battery from the PSU or USB. A state machine can also determine whether to charge the internal battery through USB at start-up. Additionally, hardware monitoring gives information to the application processor when a voltage drop occurs (programmed via internal registers).

Power Management

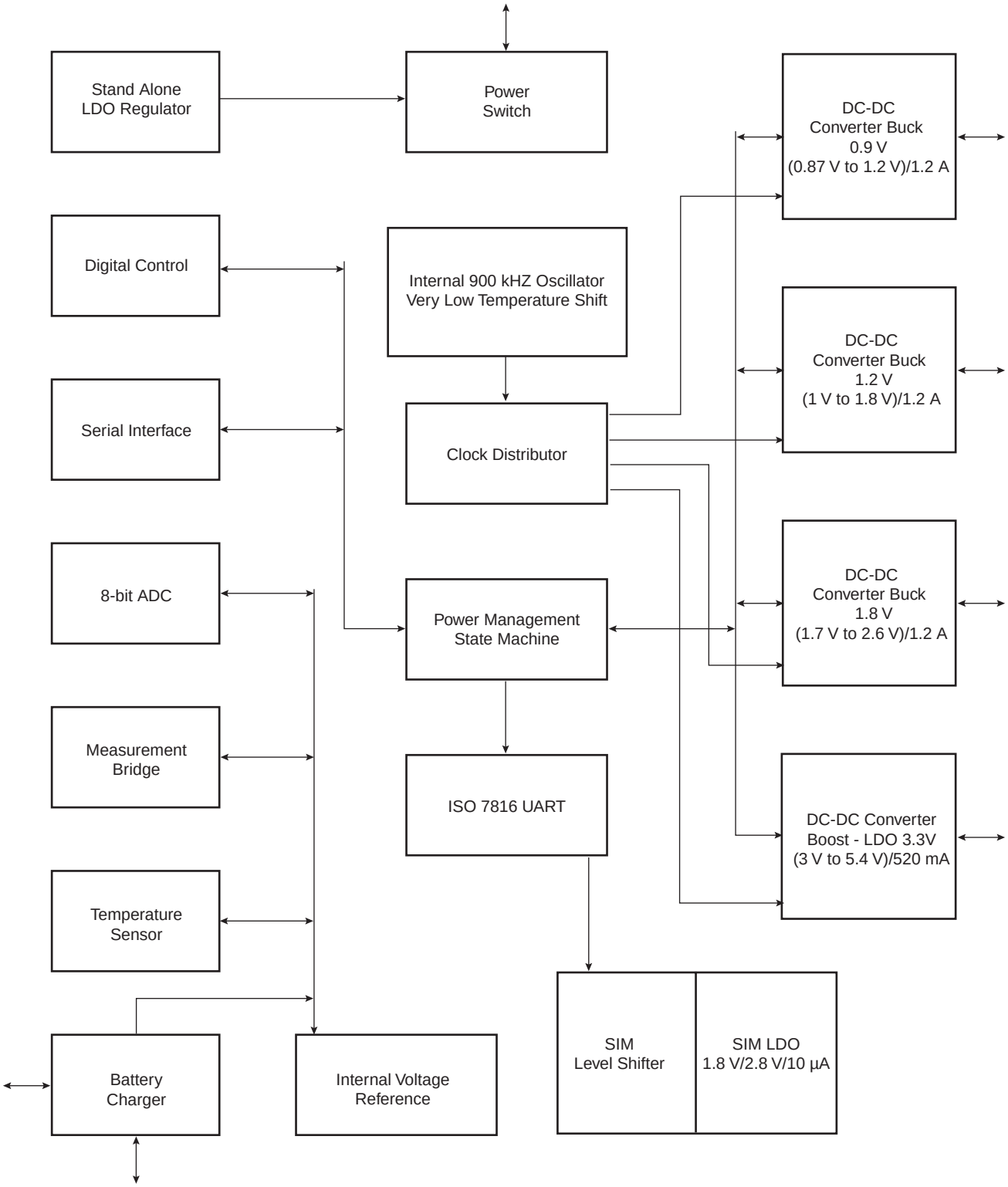
AT73C203 Power Management IC for Datacom Platforms

Preliminary

2742A–PMGMT–09/03

Functional Diagram

Figure 1. AT73C203 Functional Diagram



Pin Description

Table 1. AT73C203 Pin Description

Signal Name	Pin Type	Pack Pin	Level	ESD Protection	Comments
AVSS	A-I	A1	AVSS		ESD Ground
SELDC175	D-I	B2	gnddig - vsauv	avss - vswin	Digital control
SELDC25	D-I	B1	gnddig - vsauv	avss - vswin	Digital control
nEN_RAIL3	D-I/O	A3	gnddig - vsauv	avss - vswin	Digital control
nEN_RAIL4	D-I/O	A2	gnddig - vsauv	avss - vswin	Digital control
nASIC_RESET	D-O	C3	gnddig - vout3	avss - vout3	RESET
nBOARD_RESET	D-O	C1	gnddig - vout3	avss - vout3	RESET
BOARD_RESET	D-O	C2	gnddig - vout3	avss - vout3	RESET
nPROC_RESET	D-O	D4	gnddig - vout3	avss - vout3	RESET
nPROC_RESET_OUT	D-I	D3	gnddig - vout3	avss - vout3	RESET
nASIC_RESET_REQUEST	D-I	D1	gnddig - vout3	avss - vout3	RESET
POWER_EN	D-I	D2	gnddig - vout3	avss - vout3	Digital control
SYST_CLK	D-I	A4	gnddig - vout3	avss - vout3	Digital control
nUSIM_INT	D-O	E1	gnddig - vout3	avss - vout3	Digital control
nINT	D-O	E2	gnddig - vout3	avss - vout3	Digital control
BUTTON_OUT	D-O	E3	gnddig - vout3	avss - vout3	Digital control
CHG_INHIBIT	D-I	F1	gnddig - vout3	avss - vout3	Digital control
TEST1	D-I/O	F2	gnddig - vsauv	avss – vsauv	TEST
TEST2	D-I/O	F3	gnddig - vsauv	avss - vsauv	TEST
IDBITS3	D-I/O	G1	gnddig - vout3	avss - vout3	Digital control
IDBITS2	D-I/O	F4	gnddig - vout3	avss - vout3	Digital control
IDBITS1	D-I/O	G2	gnddig - vout3	avss - vout3	Digital control
IDBITS0	D-I/O	H1	gnddig - vout3	avss - vout3	Digital control
SDO	D-I/O	G3	gnddig - vout3	avss - vout3	SPI
SDI	D-I	H2	gnddig - vout3	avss - vout3	SPI
SCLK	D-I	J1	gnddig - vout3	avss - vout3	SPI
nSEN	D-I	E5	gnddig - vout3	avss - vout3	SPI
GNDDIG	A-I	K1	GND	avss - gnddig	Digital ground
VOUT3	A-I	K2	gnddc3 - vout3	avss - vboost	DCDC rail3
VBOOST	A-I	J2	gnddc3 - vddpsu	PCboost	DCDC rail3
DH3	A-O	K3	gnddc3 - vddpsu	avss - vboost	DCDC rail3
GNDDC3	A-I	H3	GND	avss - gnddc3	DCDC rail3
DL3	A-O	J3	gnddc3 - vddpsu	avss - PCmax	DCDC rail3
VDDPSU3	A-I	G4	gnddc3 - vddpsu	avss - PCmax	DCDC rail3

Table 1. AT73C203 Pin Description (Continued)

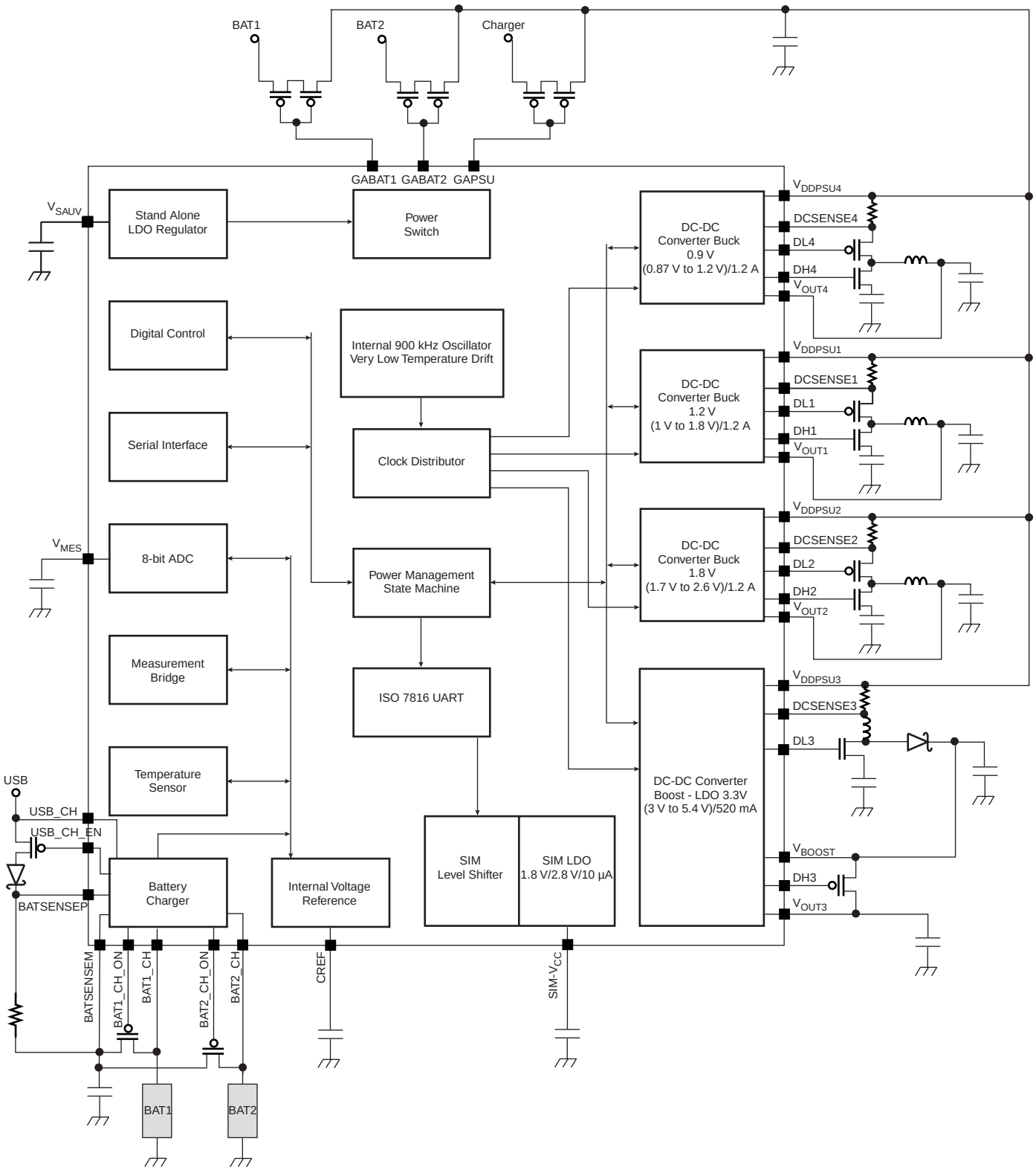
Signal Name	Pin Type	Pack Pin	Level	ESD Protection	Comments
DCSENSE3	A-I	H4	gnddc3 - vddpsu	avss - PCmax	DCDC rail3
VOUT2	A-I	K4	gnddc2 - vout2	avss - PCmax	DCDC rail2
DCSENSE2	A-I	H5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
DH2	A-O	K5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
VDDPSU2	A-I	G5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
GNDDC2	A-I	J4	GND	avss - gnddc2	DCDC rail2
DL2	A-O	J5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
VOUT1	A-I	K6	gnddc1 - vout1	avss - PCmax	DCDC rail1
DCSENSE1	A-I	H6	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
DH1	A-O	K7	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
VDDPSU1	A-I	G6	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
GNDDC1	A-I	J6	GND	avss - gnddc1	DCDC rail1
DL1	A-O	J7	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
VOUT4	A-I	J10	gnddc4 - vout4	avss - PCmax	DCDC rail4
DCSENSE4	A-I	K9	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
DH4	A-O	K8	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
VDDPSU4	A-I	K10	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
GNDDC4	A-I	J9	GND	avss - gnddc4	DCDC rail4
DL4	A-O	J8	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
SIM_CLK	D-O	H10	gnddig - vsim	avss - PCmax	SIM
SIM_RESET	D-O	H9	gnddig - vsim	avss - PCmax	SIM
SIM_IO	D-I/O	G7	gnddig - vsim	avss - PCmax	SIM
SIM_VCC	A-O	G8	gnddig - vsim	avss - PCmax	SIM regulator
GND_CH	A-I	E6	GND	avss - gndch	Charger
BAT2_CH	A-I	F7	gndch - maxsupply	avss - PCmax	Charger
BAT1_CH	A-I	F10	gndch - maxsupply	avss - PCmax	Charger
BAT2_CH_ON	A-O	F9	gndch - maxsupply	avss - PCmax	Charger
BAT1_CH_ON	A-O	F8	gndch - maxsupply	avss - PCmax	Charger
BATSENSEM	A-I	E10	gndch - maxsupply	avss - PCmax	Charger
BATSENSEP	A-I	E9	gndch - maxsupply	avss - PCmax	Charger
USB_CH_EN	A-O	E8	gndch - maxsupply	avss - PCmax	Charger
USB_CH	A-I	D10	gndch - maxsupply	avss - PCmax	Charger
GABAT1	D-O	E7	gnda1 - maxsupply	avss - PCmax	Power switch
GABAT2	D-O	D9	gnda1 - maxsupply	avss - PCmax	Power switch
GAPSU	D-O	C10	gnda1 - maxsupply	avss - PCmax	Power switch
VDDPSU	A-I	G10	gnda1 - vddpsu	avss - PCmax	Power switch

Table 1. AT73C203 Pin Description (Continued)

Signal Name	Pin Type	Pack Pin	Level	ESD Protection	Comments
BAT1_PIO	A-I	D8	gnda1 - bat1	avss - PCmax	Power switch
BAT2_PIO	A-I	C9	gnda1 - bat2	avss - PCmax	Power switch
PSU_PIO	A-I	B10	gnda1 - psu	avss - PCmax	Power switch
USB_PIO	A-I	D6	gnda1 - usb	avss - PCmax	Power switch
MAXSUPPLY	A-O	A10	gnda1 - maxsupply	PCmax	Power switch
GND_PIO	A-I	B9	GND	avss - gnda1	Power switch
VREFFUSE	A-I	A9	avss - 5.5v	avss-vswin	FUSES
VBIAS	A-O	C8	gnda - vsauv	avss - vswin	Reference generator
CREF	A-O	A8	gnda - vsauv	avss - vswin	Reference generator
VMES	A-O	B8	gnda - vsauv	avss - vswin	Measurement bridge
PORTEST	D-O	D7	gnda - vsauv	avss - vswin	Power on reset
THERM1	A-O	C7	gnda - vsauv	avss - vswin	Current generator
THERM2	A-O	A7	gnda - vsauv	avss - vswin	Current generator
GNDA	A-I	B7	GND	avss - gnda	Internal regulator
VSAUV	A-O	C6	gnda - vsauv	avss - vswin	Internal regulator
VSW	A-I	A6	gnda - vswin	avss - vswin	Internal regulator
VSWIN	A-I	B6	gnda - vswin	PCvswin	Internal regulator
SCAN_TEST_MD	D-I/O	C4	gnddig - vsauv	avss - vswin	TEST
SCAN_ENABLE	D-I/O	A5	gnddig - vsauv	avss - vswin	TEST
nSHUTDOWN	D-I	B5	gnddig - vsauv	avss - vswin	Digital control
PCMCIA	D-I	C5	gnddig - vsauv	avss - vswin	Digital control
SIM_PRES	D-I	G9	gnddig - vsauv	avss - vswin	Digital control
BUTTON_IN	D-I	D5	gnddig - vsauv	avss - vswin	Digital control
NC		B4			Not Connected
NC		E4			Not Connected
NC		H8			Not Connected
NC		H7			Not Connected
NC		F5			Not Connected
NC		B3			Not Connected
NC		F6			Not Connected

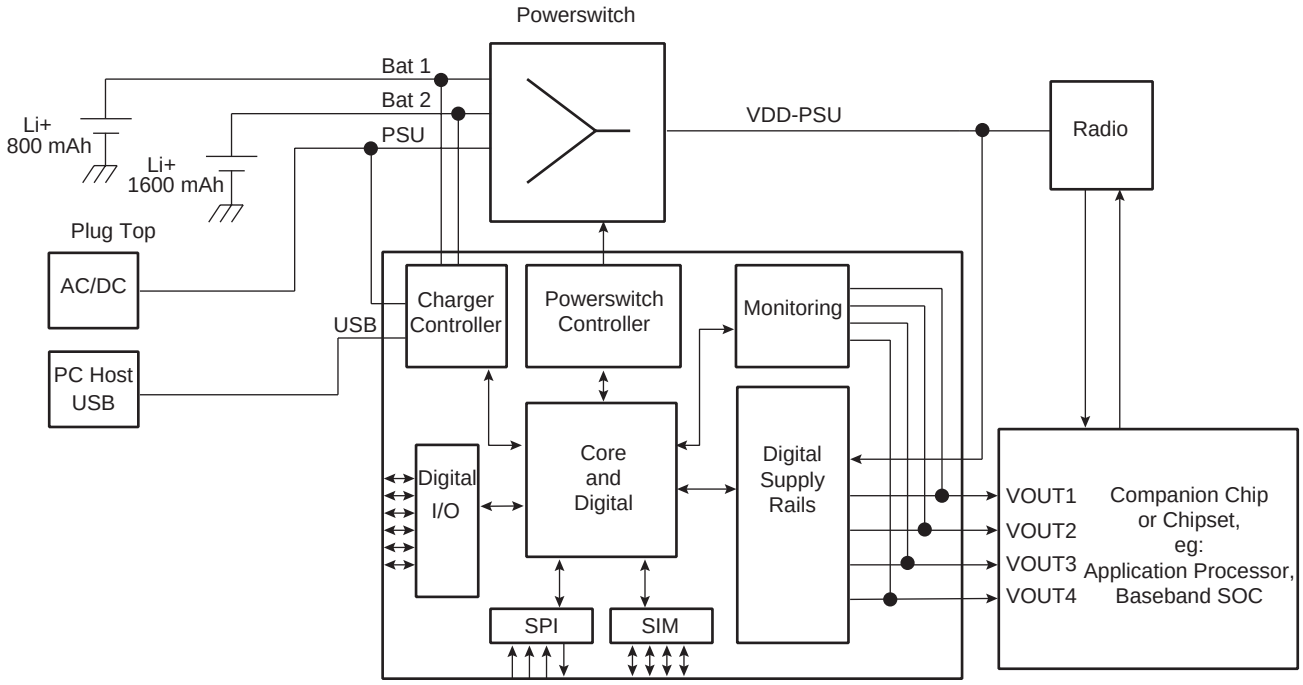
Application Schematic

Figure 2. AT73C203 Application Schematic



Architecture Overview

Figure 3. AT73C203 Architecture Overview



System Level Description

Several power sources may be used to power the AT73C203 circuitry including an internal or external battery, external PSU or USB. The internal battery is always physically present in the unit, but any or all of the other sources may be connected or disconnected at any time.

The AT73C203 enables one application to be powered up from the correct source of up to four possible power sources under hardware control. When powered, the external processor can monitor the input power sources and initiate battery charging as required via the SPI. The application processor is also able to enable/disable the circuit power rails and configure a low power sleep state.

An input-multiplexed 8-bit ADC is available that allows the application processor to monitor the presence of and measure the voltage of the power sources, batteries and rails. An associated threshold and comparator circuit may be used to indicate to the processor that an out-of limit event has occurred.

The battery charging circuitry is designed to allow charging from the PSU input and to allow current-limited 'supplement' charging from the USB input. In both cases, the chargers operate under processor control and monitoring with hardware safety lockout.

When the PSU is present, a power path is selected (e.g. from a DC jack) through the power switching circuitry to the external components (e.g. radio and companion chips or chipset, baseband chip etc.) This power path enables the application processor to boot up. A parallel path exists from the PSU input (e.g. jack) through current limiting devices to two battery chargers. The current switches only block reverse current when disabled so care must be taken when controlling them.

When a USB input is powered, a single power path exists through the current limiting devices to the two battery chargers. The hardware defaults to a current limit of 100 mA but the application processor may set 500 mA after negotiation with the PC. This power should always be used to charge the batteries in the absence of the PSU power source.

SIM/USIM interface hardware is provided, allowing the application processor to communicate and control a SIM/USIM card according to the required analog and digital specifications.

Most of the blocks are switched on or off by the digital control block (not all the control lines are drawn on the block diagram).

Only the supply monitor, digital control, power on reset, 10 kHz internal oscillator and internal regulator are always on.

All these blocks are designed to have very low power consumption, capable of achieving three months standby time for the application.

Functional Integration

The AT73C203 integrates the following functions:

Supply Monitor

The supply monitor block enables the AT73C203 to correctly switch the four main supplies (two batteries, PSU and USB). All the outputs are sent to the digital control.

Internal Regulator

The internal regulator is a low drop out regulator generating V_{SAUV} at 2.5 V with a maximum load of 5 mA. Its input is V_{SW}.

Power-on Reset

The internal power-on reset is supplied by V_{SAUV} and resets the AT73C203 digital circuitry at 2 V.

10 kHz Internal Oscillator

The 10 kHz low power oscillator is the clock source for the AT73C203 digital circuitry. V_{SAUV} supplies it.

Digital Control

The digital block controls each block and drives the SPI interface and the different interrupts (external and internal). The controls, inputs and outputs are level shifted when necessary and protected to avoid current flowing between the blocks (not represented in the block diagram). A state machine controls the AT73C203 circuitry according the supplies and inputs states. A table of registers is accessible via SPI to command or read status of the AT73C203.

Reference Generator

The reference generator provides the AT73C203 with a precise bandgap voltage (V_{REF}) and current bias (I_{REF}) used by all analog blocks (DC/DC, ADC, charger) except the core blocks. It is turned off under digital control when necessary and is V_{SAUV} supplied.

900 kHz Oscillator and Clock Distribution

The 900 kHz oscillator provides the clock to all DC/DC converters. The clock distributor provides phased clocks to the DC/DC converters to avoid switching at the same time. The frequency of the oscillator is trimmed during production to optimize the DC/DC efficiency.

DC to DC Step Down 1.2 A, 0.9 V

The DC to DC step Down 1.2A, 0.9 V (dynamically adjustable to 0.87 V/0.9 V/1.1 V/ 1.2 V) is a programmable buck DC/DC converter dedicated to advanced sub-micron processors and SoC ASIC logic cores requiring dynamic power management at low voltages and high currents.

The default voltage is 0.9 V for which the device is optimized.

The external components needed include a current sensing resistor, a dual PMOS-NMOS, an inductor and an output capacitor.

The application processor can change the output voltage via registers accessible by SPI.

When the cell is off, the output is in high impedance state.

If not used, this section can be permanently deactivated.

DC to DC Step Down 1.2 A, 1.2V OR 1.75 V

The DC to DC step Down 1.2 A, 1.2 V (dynamically adjustable to 1.0 V/1.1 V/1.2 V/ 1.3 V) is a programmable buck synchronous DC/DC converter dedicated to the application processor core and/or a "companion" ASIC SoC Processor Core. The default voltage is 1.2 V. An external pin can select 1.75 V output voltage with tuning: 1.80 V, 1.70 V or 1.65 V. The entire cell is optimized for 1.2 V. The application processor can change the output voltage as described above via registers accessible by SPI.

The external components needed include a current sensing resistor, a dual PMOS-NMOS, one inductor and one output capacitor.

When the cell is off, the output is pulled to ground.

If not used, this section can be permanently deactivated

DC to DC Step Down 1.2 A, 1.8 V OR 2.5 V

The DC to DC step Down 1.2 A, 1.8 V (dynamically adjustable to 1.70 V/1.75 V/1.80 V/1.85 V) is a programmable buck synchronous DC/DC converter dedicated to the supply of recent and future Flash and SDRAM memories and their associated buses on the application processor I/O section as well as additional memory extension modules such as CF cards, MMCards, Memory Stick, etc. The default voltage is 1.8 V. An external pin can select 2.5 V output voltage with tuning: 2.6 V, 2.4 V and 2.3 V. The entire cell is optimized for 1.8 V. The application processor can change the output voltage as described above via registers accessible by SPI.

The external components needed include a current sensing resistor, a dual PMOS-NMOS, an inductor and an output capacitor.

A low quiescent current mode is implemented when a very low standby current is needed with a parallel voltage regulator.

When the cell is off, the output is in high impedance state.

DC to DC Step Up/ Down 520 mA, 3.3 V

The DC to DC step Up/Down 520 mA, 3.3 V (dynamically adjustable to 3.0 V/3.1 V/ 3.4 V) is a boost DC/DC 3.6 V converter followed by a linear drop out regulator. It is intended to supply 3.3 V I/Os needed in the application (Audio Codec, LCD, Memories).

The external components needed include a current sensing resistor, an NMOS, a Schottky diode, an inductor and an output capacitor.

The default value of the LDO is 3.3 V but three other values can be programmed: 3.1 V, 3.2 V and 3.4 V. The entire cell is optimized for 3.3 V. The application processor can change the output voltage as described above via registers accessible by SPI.

When the cell is off, the output is pulled to ground.

Power Switch Controller

The power switch controller drives an external PMOS switch to multiplex VDD-PSU from the internal or external battery or USB. The purpose of this cell is to guarantee a sufficient supply for VDD-PSU and to limit voltage drops even during switchover. In-rush current and current flow between the inputs must be avoided.

When this cell is off, VDD-PSU is left in high impedance.

Current Generators

Two accurate current generators allow the measurement of the resistance of two external battery thermistors. The outputs V_{THE1} and V_{THE2} go to the measurement bridge. The current generators are supplied by V_{SAUV} and controlled by the digital control for use during battery charging.

Temperature Sensor

The temperature sensor voltage output depends linearly on temperature. It is supplied by V_{SAUV} and driven by the digital control. The temperature seen by the sensor is directly related to the chip activity and the power internally dissipated. To get a good indication of the ambient temperature, the software must take into account this offset.

Measurement Bridge/ Multiplexer

The measurement bridge provides adapted voltages of the internal and external batteries, DC/DC converter outputs, USB, VDD-PSU, V_{THE1} and V_{THE2} to the multiplexed input of the serial analog to digital converter.

Analog to Digital Converter

An 8-bit analog to digital converter is integrated into the AT73C203 to give information about voltage and temperature to the application processor via the SPI interface.

Li-Ion/Battery Chargers

The battery chargers both have stand-alone constant current (CC) precharge and microprocessor-controlled CC fast charge as well as top-off mode end-of-charge algorithm.

The digital block controls this cell. All current and voltage settings are programmable via registers.

The charger controller is divided into two similar parts, one for the internal battery and one for the external battery. Each charger multiplexes the source (USB or PSU) and limits the programmable current charge (via sense resistor). An external PMOS and a Schottky diode are needed for each charger.

The application processor must check that the temperature allows charging via the current generator, measurement bridge and ADC.

USIM Voltage Regulator

A regulator is provided to power up the USIM card. It is supplied directly from VDD_PSU. One of two different voltages can be selected:

- 2.8 V (50 mA)
- 1.8 V (30 mA)

By default, the regulator is in power-down mode.

The pins connected to the USIM (SIM_CLK, SIM_IO, SIM_PWR) must have driver specification according to ETS TS 102 221.

USIM Digital Section

The main part of the USIM digital section is an ISO7816 UART compatible interface.

Reset Generation

A reset is generated via the internal state machine. The timer for this internal reset generator is 150 ms (typical). The application processor can set the AT73C203 to off mode via the POWER_EN pin. The "internal" reset is active at low level.

Another way to generate a reset is to program it through the monitoring function (ADC with measurement bridge and data registers). The "monitoring" reset is active at low level.

A logical AND of the "internal" and the "monitoring" reset drives the reset of the external application processor (NPROC_RESET pin).

Other pins are used to generate separated resets for external "companion" chips such as baseband chips.

NSHUTDOWN forces the AT73C203 internal digital block to the reset state. This turns all the supplies off and then restarts the internal state machine.

External Recommended Components

Table 2. External Recommended Components

Schematic Reference	Component Reference
C1, C3, C5, C8, C16, C17, C18, C19	22 µF ceramic
C2, C4, C9	2 x 22 µF tantalum low ESR
C6, C7	22 µF tantalum low ESR
C10,	100 nF XR5 ±10%
C11, C13, C22	2.2 µF X5R ± 10%
C12	330 nF X5R ± 10%
C14, C15	10 nF X5R ± 10%
C20	100 nF
C21	100 pF X5R ± 10%
D2, D3	Bat54C
D4, D5, D1	MBRA120LT3 (ON Semiconductor®)
L1, L4	4.7µH SMT3106-471M (Gowanda®)
L2, L3	10 µH SMT3106-102M (Gowanda)
R1, R2, R4	100 mΩ± 2% 250mW
R3	100 mΩ ± 2% 250mW
R5	220 kΩ ± 1%
R6	200 mΩ ± 2% 50mW
T1, T2, T3	Si4965DY
T4	Si5513DC
T5	Si5513DC
T6	Si1400DL
T7, T9, T10	Si8401DL
T8	Si5513DC
T11	Si1405DL

Absolute Maximum Ratings

Operating Ambient Temperature.....-40°C to +85°C
Storage Temperature.....-55°C to + 150°C
BAT1_PIO, BAT2_PIO, PSU_PIO, USB_PIO,
USB_CH, BAT1_CH, BAT2_CH, VSW_IN to ground Pins.....-0.3V to +6.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

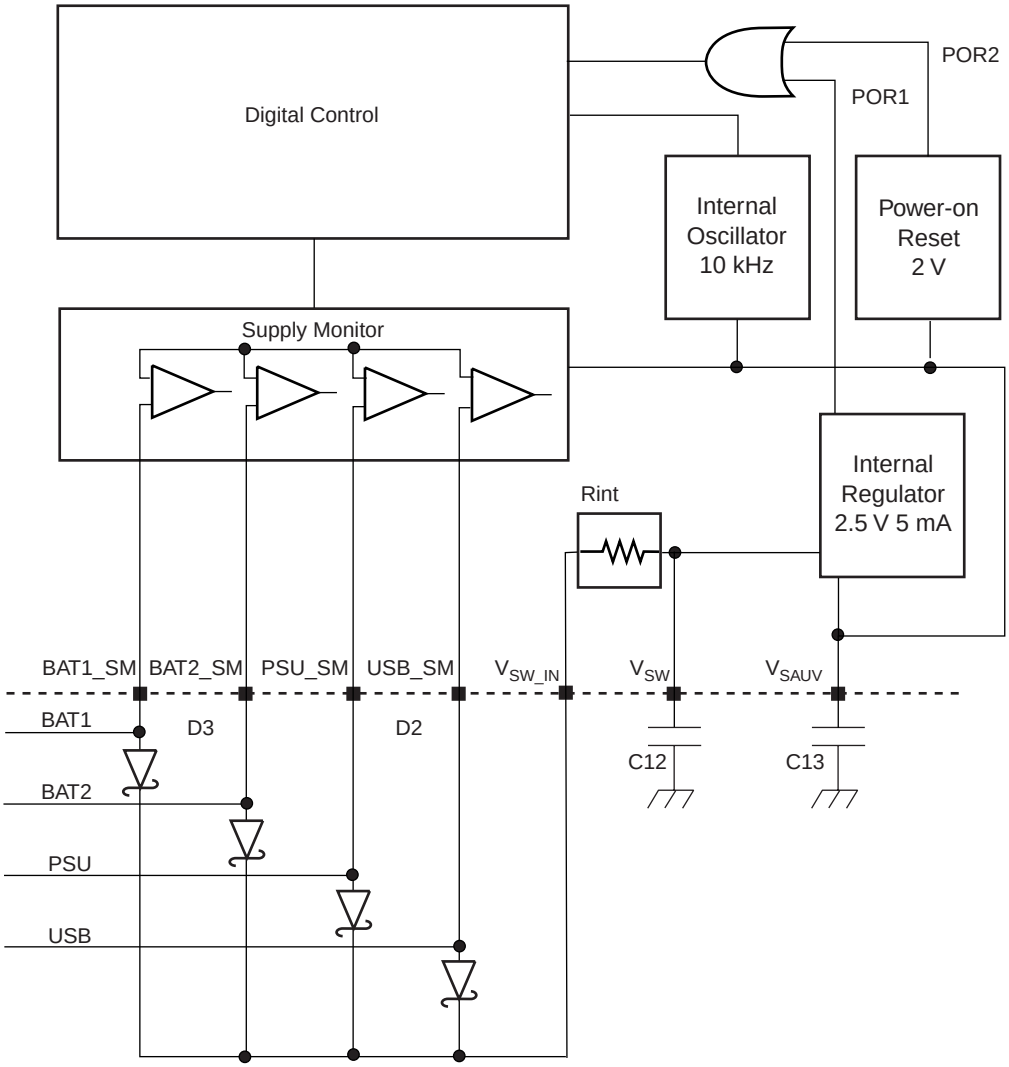
Parameter	Conditions	Min	Max	Unit
Operating Ambient Temperature		-40	+85	°C
Storage Temperature		-55	+150	°C
Signal to Ground Pins	BAT1_PIO, BAT2_PIO, PSU_PIO, USB_PIO, USB_CH, BAT1_CH, BAT2_CH, VSW_IN	-0.3	+5.5	V

System Overview

Startup and Off Mode

Most of the blocks are switched on or off by the digital block. Only the supply monitor, digital control, power-on reset, internal 10kHz oscillator and internal regulator are always on.

Figure 4. Start-up Overview



The system has two modes: Off and Active.

Off Mode: All the cells are off except the supply monitor, digital control, power-on reset, internal 10 kHz oscillator and internal regulator. These blocks are designed to consume very little power in order to achieve an off time of three months from a 600 mAh fully charged battery.

Active Mode: The power switch and all the DC/DC controllers are on. All the other cells are controlled by software (via internal registers).

Startup Description

V_{SW_IN} is an analog OR of BAT1, BAT2, USB and PSU implemented using four external Schottky diodes. Schottky diodes are used to minimize the power source to the AT73C203 voltage drop in order to maximize battery life. See Figure 4 on page 13.

When at least one of these supplies are present, V_{SW_IN} tracks the highest voltage of the four inputs. An internal resistor (Rint) between V_{SW} and V_{SW_IN} limits the current flowing through the diodes and C12.

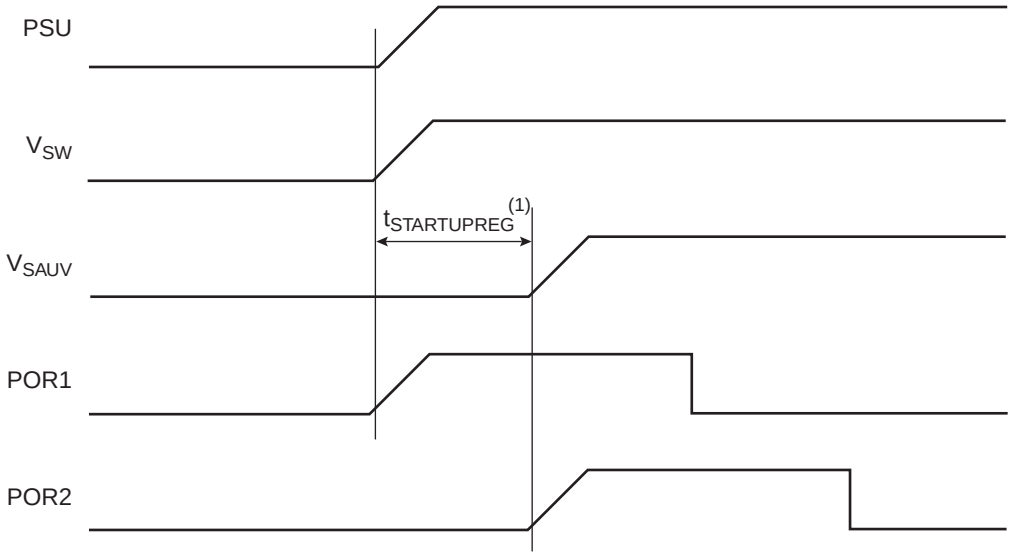
V_{SW} is the input of the internal regulator, which delivers the supply for the digital, oscillators, power-on reset, measurement bridge, reference generator, AD converter, temperature sensor, current generator and supply monitor blocks. Only a small current is supplied from V_{SW_IN} which minimizes the voltage drop across the Schottky diodes.

Power-on-reset Protection

Figure 5 below and Figure 6 on page 15 illustrate the start-up sequence of the AT73C203 under the following conditions.

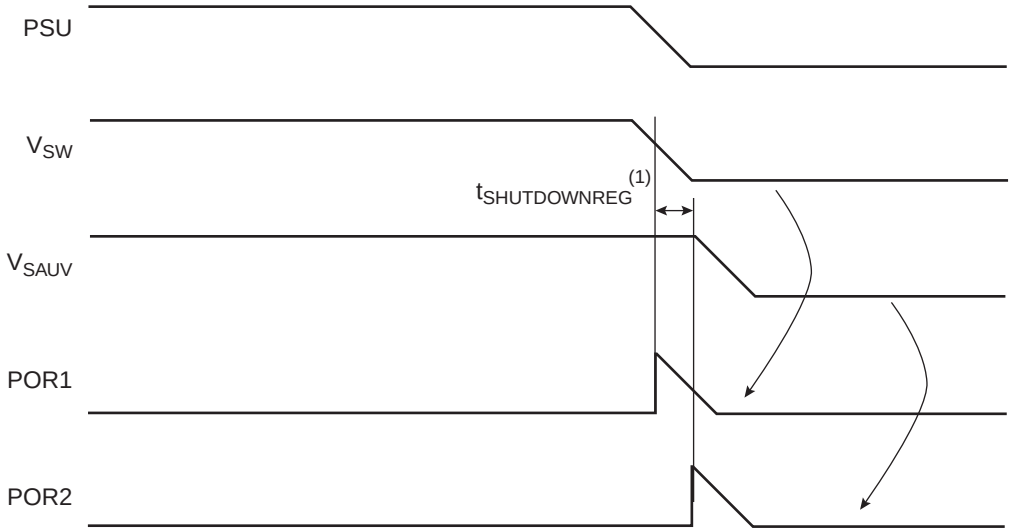
- One supply is present (PSU), the others are connected to ground or not present.
- POR1 supervises V_{SW}. It goes to low level after the start-up time of the internal regulator.
- POR2 supervises V_{SAUV}. It goes to low after V_{SAUV} reaches the correct value for the digital core to run.
- Both V_{SW} and V_{SAUV} must be stable for the digital block to operate correctly.
- The reset for the digital core is the logical OR of POR1 and POR2.

Figure 5. PSU Rising Sequence



Note: 1. $t_{STARTUPREG}$ = Startup time of the internal regulator.

Figure 6. PSU Drop Sequence



Note: 1. $t_{SHUTDOWNREG}$ = Shutdown time of the internal regulator.

State Machine Description

State machines for the start-up and off modes are described in the following pages.

The state machine is completely synchronous to the internal 10 kHz oscillator and all the signals connected to the analog blocks are level shifted as necessary and protected to allow a reliable level.

USB_FST is a digital flag. By default USB_FST is set at 0. If the digital core begins to precharge battery 1 from USB at startup, USB_FST is set to 1 by the internal digital block. The application processor can reset it to 0 via the SPI if needed by setting the USB_FCR flag. This flag acts to avoid digital oscillation when the charge through USB is the start condition. It is also used to inform the application processor that the AT73C203 has charged the internal battery from USB with a minimal amount of charge.

The digital core can also put the AT73C203 via USB_SCR register into a mode where the digital core is off and battery1 is charged (25 mA) through USB until 4,1 V. In this mode (see Figure 10 on page 19) and when battery1 is precharged by USB (see Figure 8 on page 17), a CTN thermistor must be connected to therm1. The CTN thermistor used must be equivalent to the thermistor 103JT-025 from SEMITEC®.

- Temperature to allow precharging through USB: 0°C to 60°C.
- Safety timer for the USB stand alone mode: 1 hour
- Safety timer for the USB Sleep mode: 24 hours

Figure 7. Startup State Machine (1of 3)

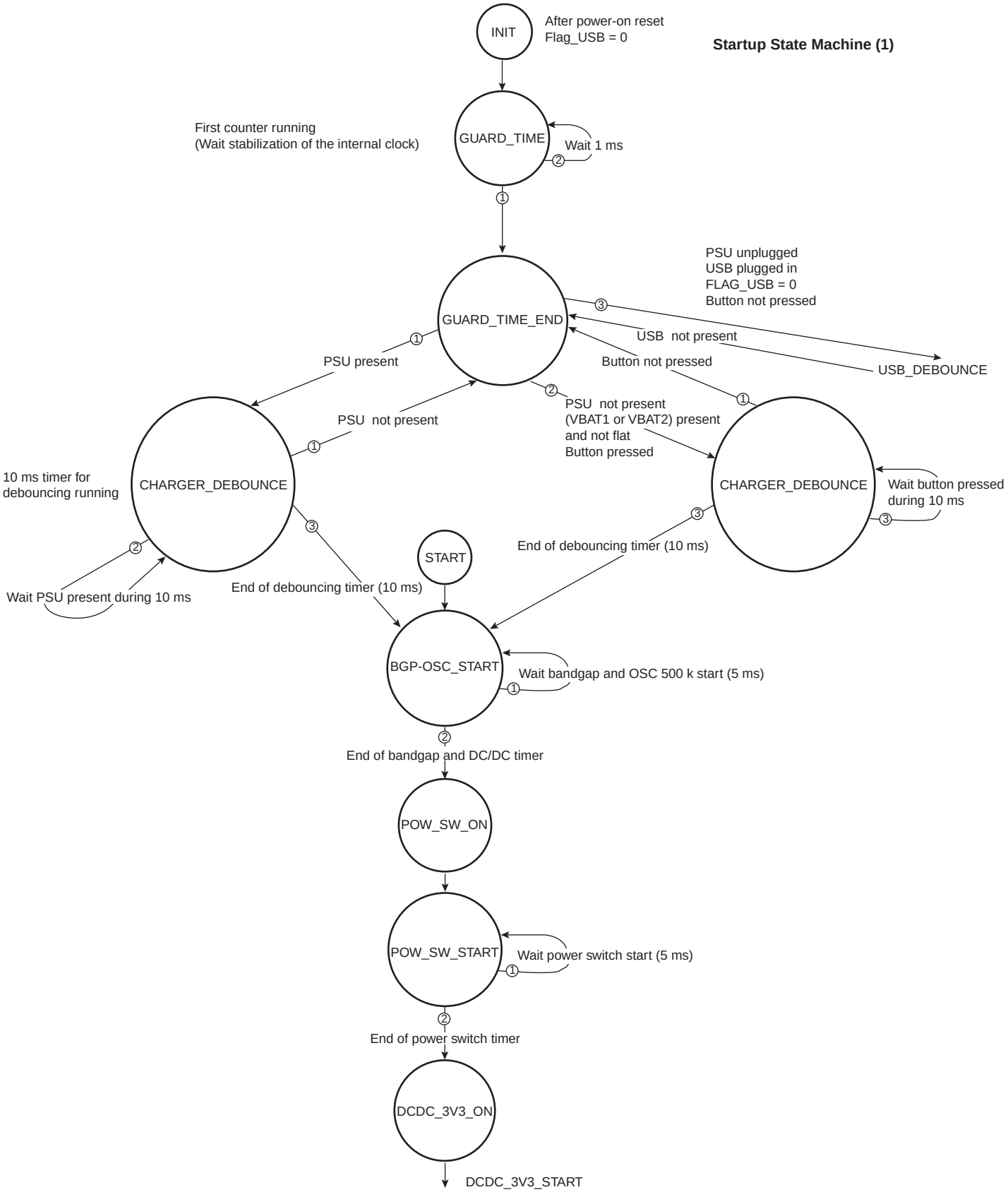


Figure 8. Startup State Machine (2 of 3)

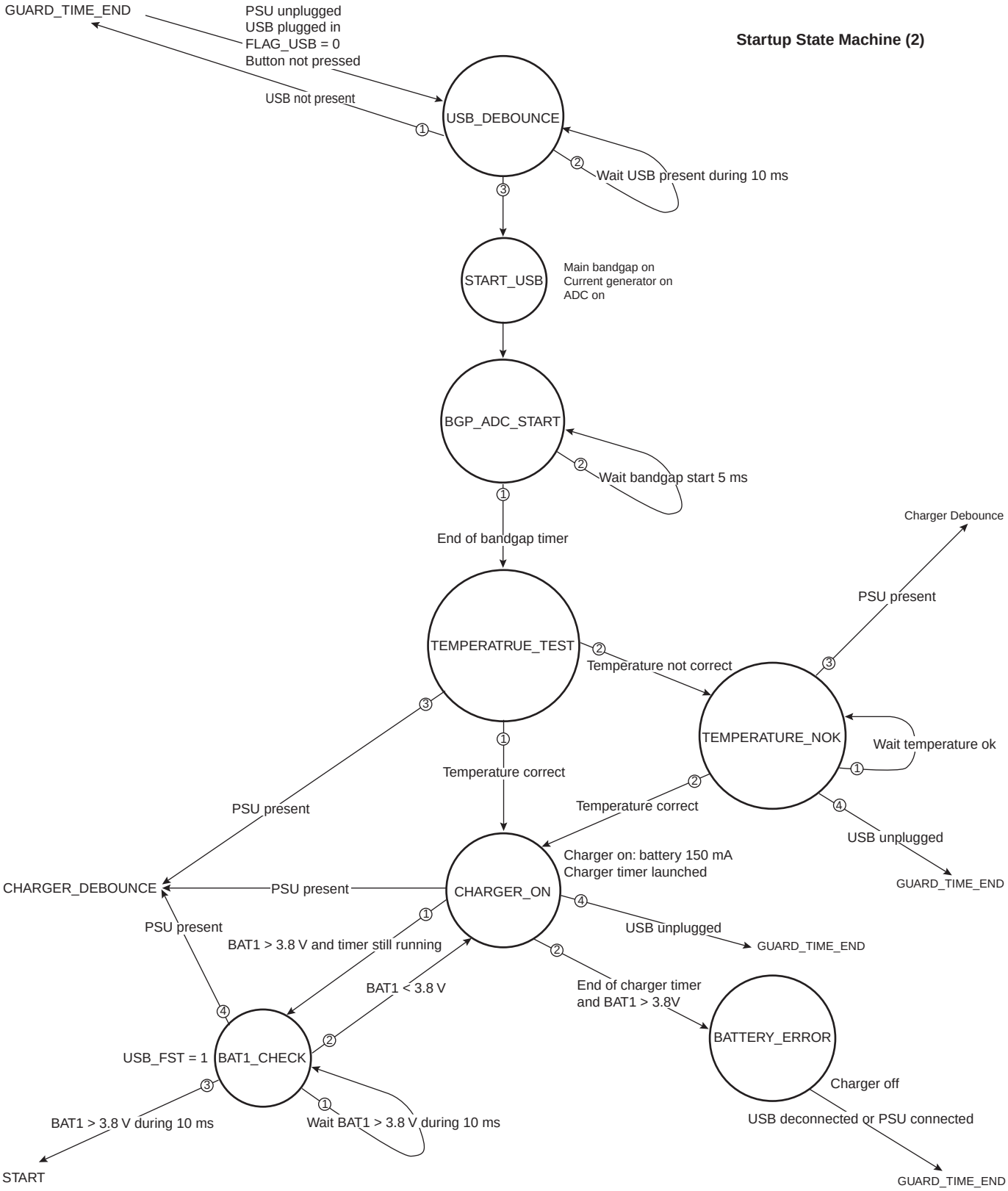


Figure 9. Startup State Machine (3 of 3)

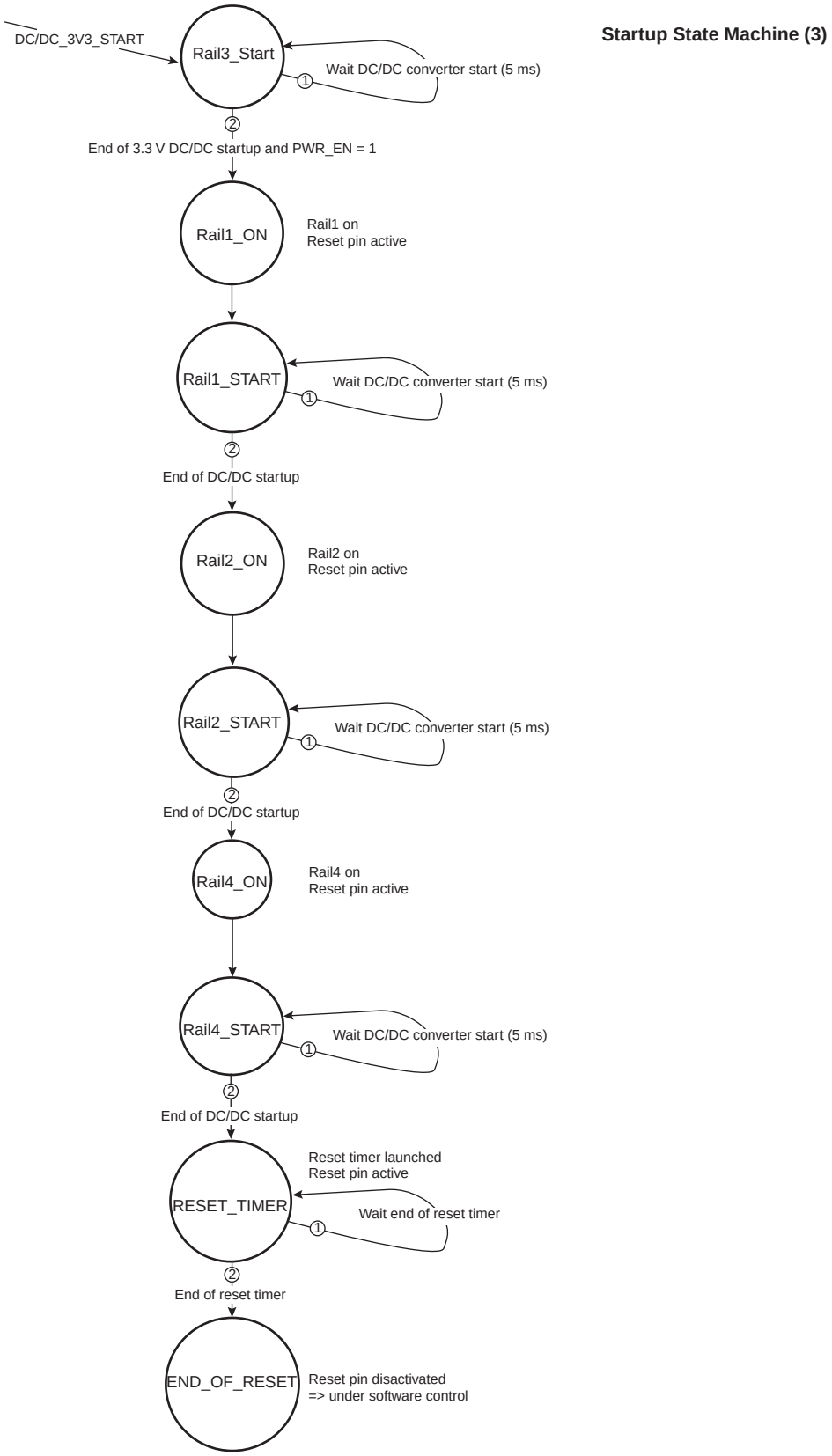


Figure 10. USB Sleep State Machine

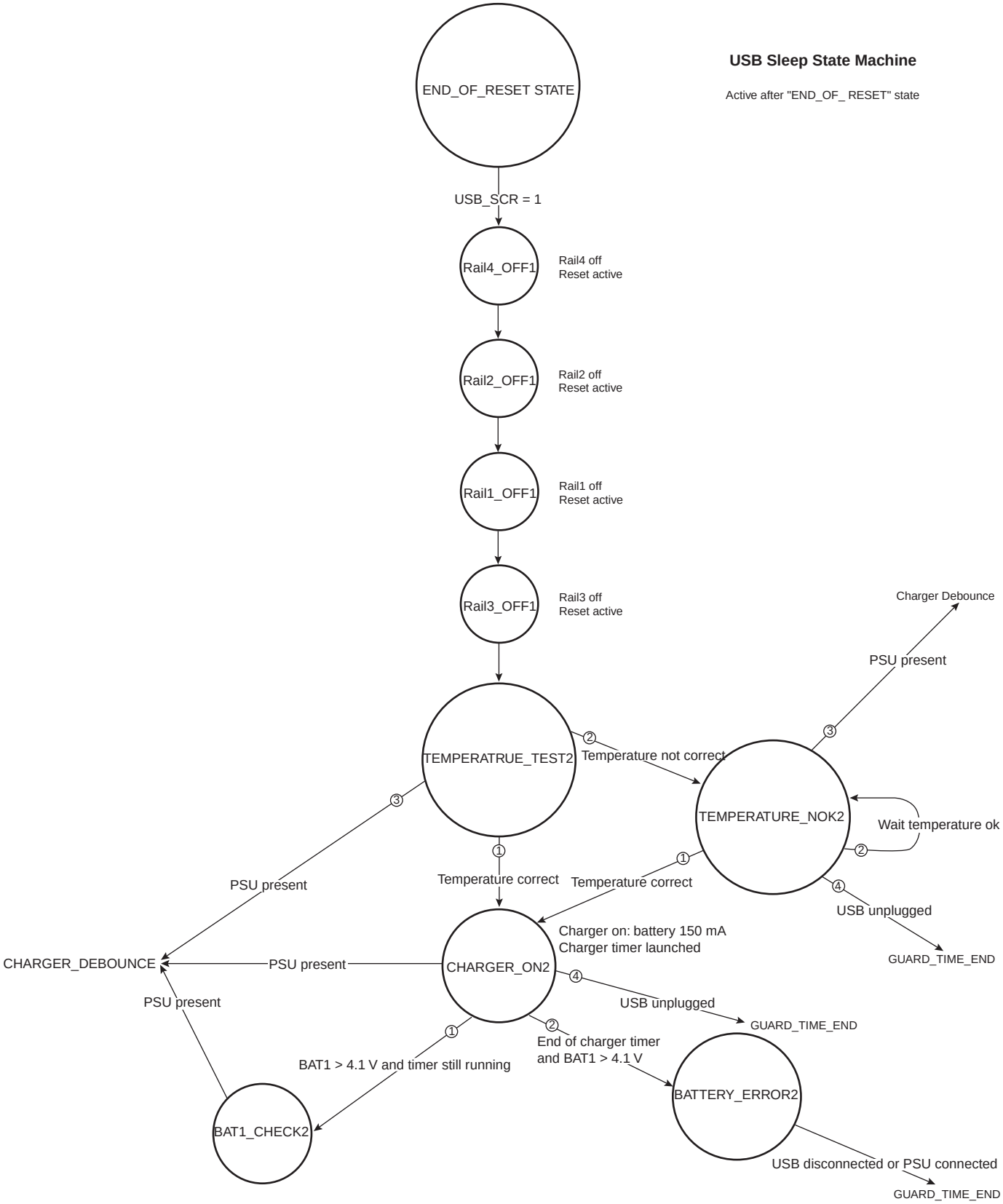
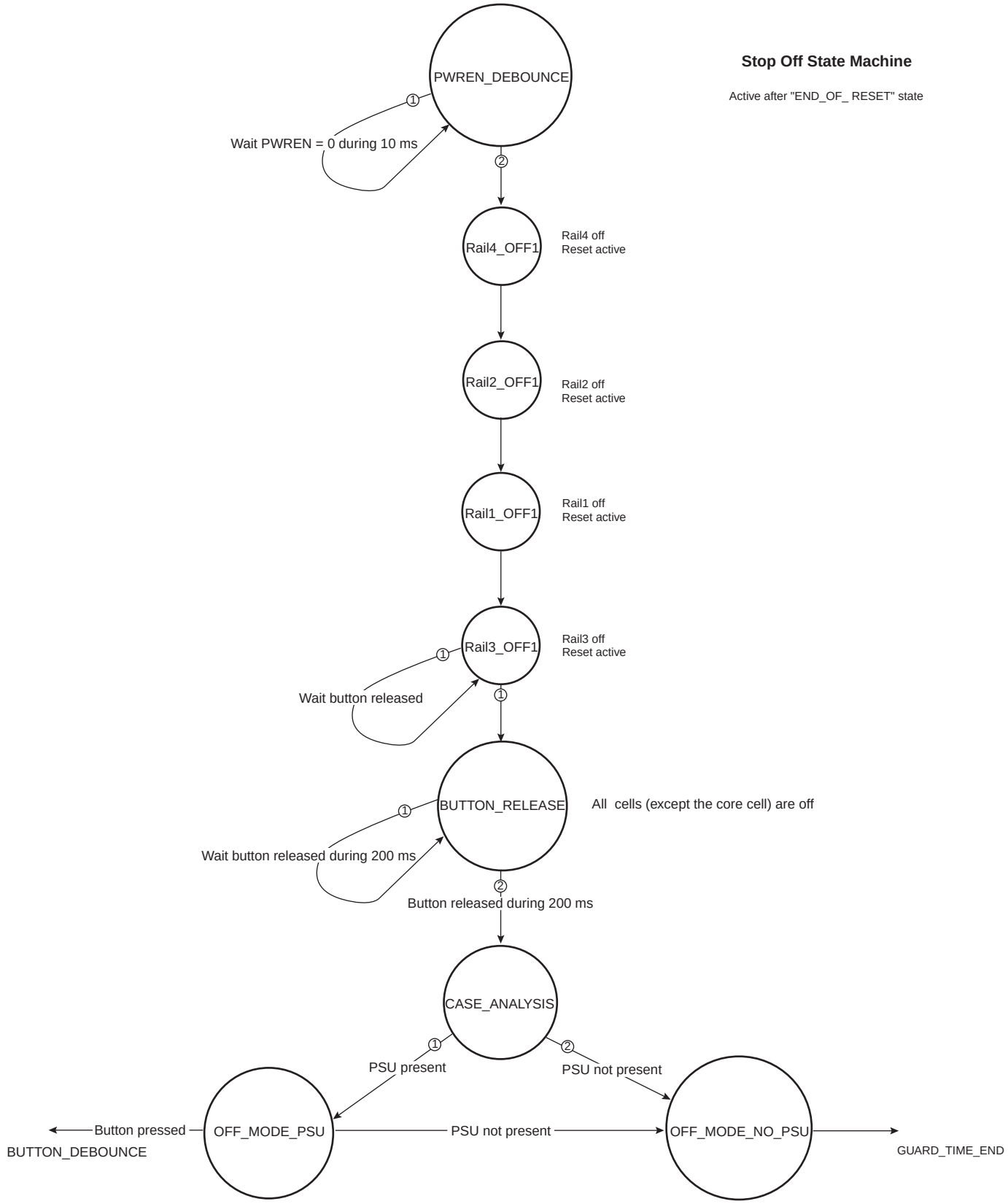


Figure 11. Stop Off State Machine



Reset Generation

A reset is generated via the internal state machine as described in Figure 7 on page 16, Figure 8 on page 17, Figure 9 on page 18 and Figure 11 on page 20. The timer for the internal reset generator is 150 ms (typical).

The application processor can set the AT73C203 to off mode via the POWER_EN pin (Figure 11 on page 20). This "internal" reset is active at low level.

Another way to generate a reset is to program it through the monitoring function. The "monitoring" reset is active at low level.

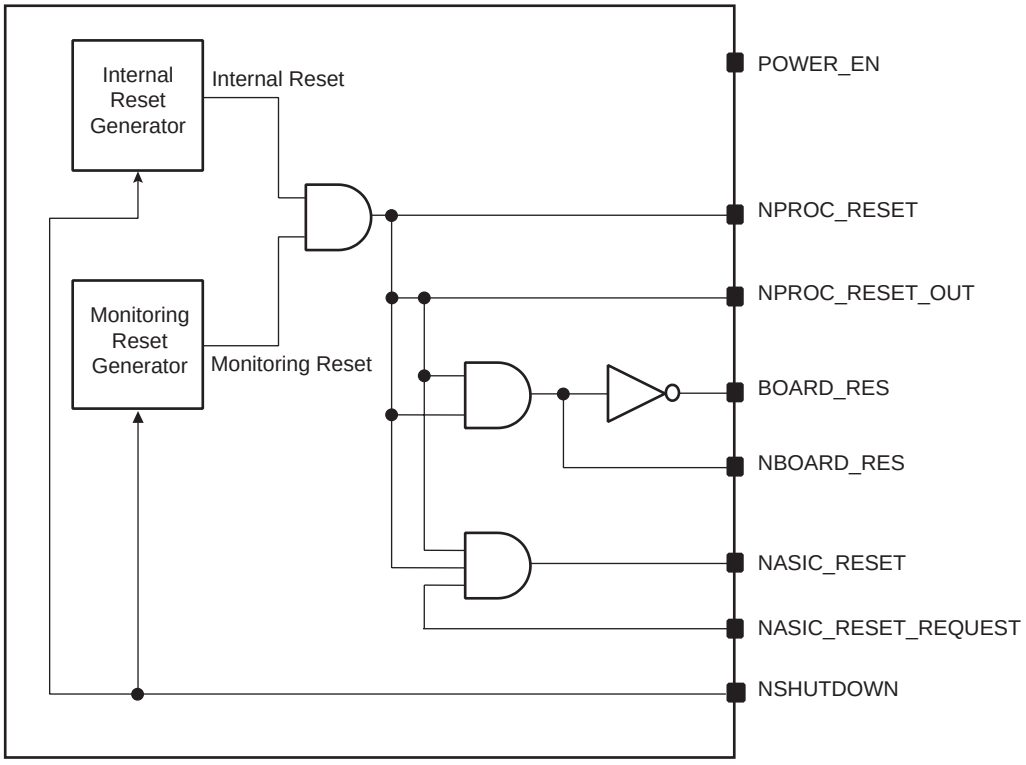
An logical AND of the "internal" reset and the "monitoring" reset drives the reset of the external microprocessor. It is connected to the NPROC_RESET pin and directly drives the external microprocessor.

Additional pins are used to generate separated resets for the baseband chips (see Figure 12 below).

NSHUTDOWN forces the AT73C203 internal digital block to the reset state. This turns all the supplies off and then restarts the internal state machine.

Power-on reset resets the internal state machine. nPROC_RESET resets all other digital parts, with the exception of the USIM interface which is reset via the nBOARD_RES pin.

Figure 12. Reset Generation Architecture



Electrical Characteristics

Power Switch

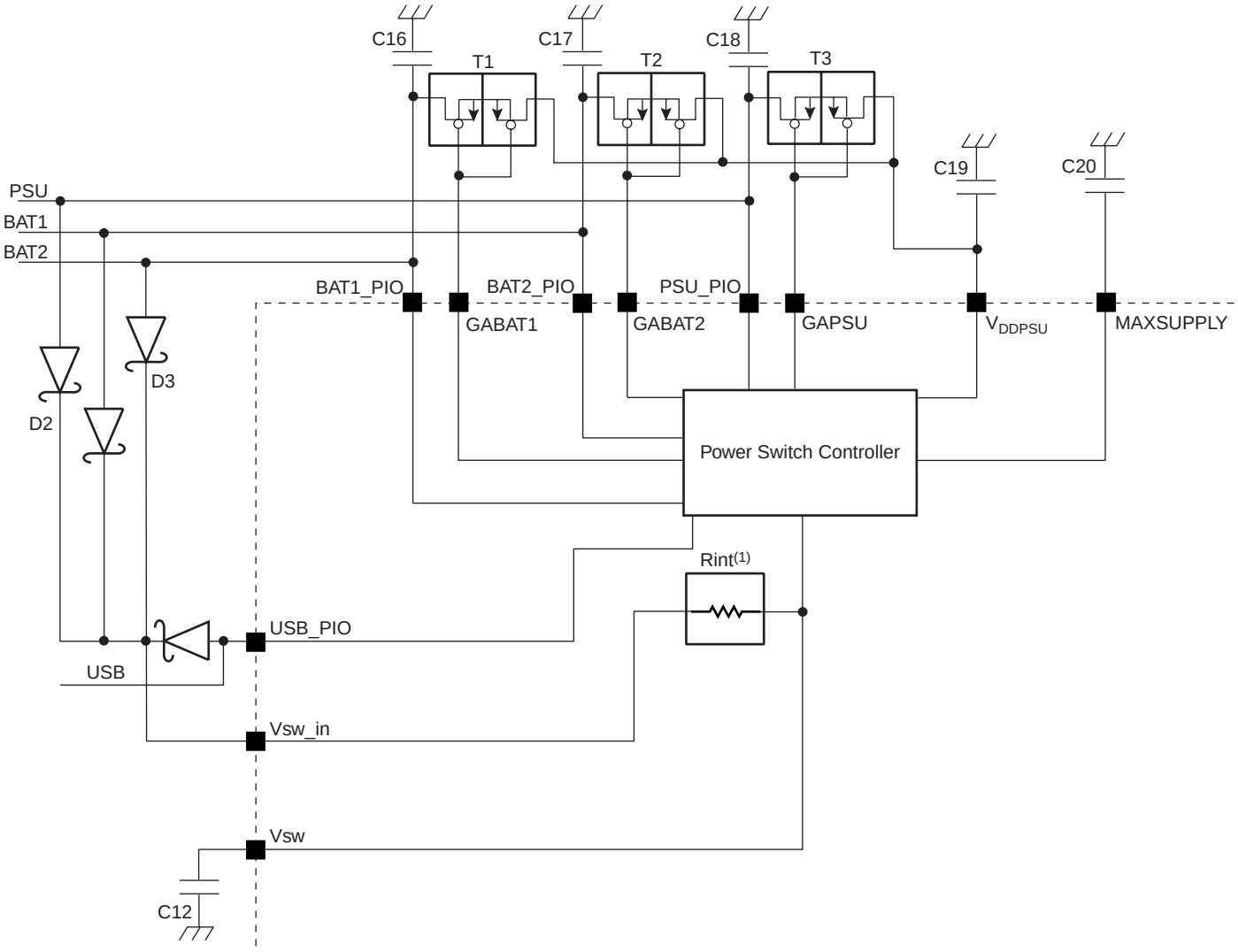
The power switch control block drives external dual PMOS devices to multiplex V_{DDPSU} from battery 1 (BAT1), battery 2 (BAT2) and an AC/DC Power supply unit (PSUIN).

The purpose of this cell is to guarantee a sufficient supply for V_{DDPSU} and to limit drops even during switchover.

Inrush current from source to V_{DDPSU} must be avoided.

Back powering from a selected power source to all other power sources must be avoided.

Figure 13. Power Switch Controller



Note: 1. Rint is internal to the AT73C203.

Automatic Selection

When the power switch digital control block is off, V_{DDPSU} is set to the high impedance state. The supply of this cell comes from an analog OR done with four external Schottky diodes connected to BAT_1PIO, BAT2_PIO, PSU_PIO and USB_IN.

The system should respect the "Universal Serial Bus Specification", especially section 7.2.4.1, which specifies that the maximum equivalent load seen by the USB is 10 µF in parallel with 44 ohms.

When the cell is on, the power switch must automatically select the correct power source.

PSU is a non current-limited 5 V supply output. BAT2 is a Lithium Ion battery and can be removed. BAT1 is a Lithium Ion battery and is always soldered to the PCB.

A selection priority rule is used:

PSU > BAT2 > BAT1

When the PSU is plugged in, it is selected by default.

If the PSU is not plugged in, BAT2 is used if it is present and has enough voltage.

If PSU is not plugged in, and BAT2 is unplugged or below the flat threshold, BAT1 is used if BAT1's voltage is high enough.

For a critical situation on any of the power sources, the automatic switching shall ensure that V_{DDPSU} stays within specifications. This means that the automatic supply selection FETs must be switched as quickly as possible, ideally with a maximum switchover of 1 µs (max: 5 µs) and guarantee that the already enabled FETs are switched off before the newly selected FETs are switched on.

The faster the switching, the smaller the capacitance required to hold up V_{DDPSU} (target: 100 µF max).

To handle all cases, fast analog comparators on each input with appropriate hysteresis (in voltage and in time) must be used within the AT73C203.

To meet the 5 µs requirement, the comparator must be fast enough to detect when a source is disconnected (or a low voltage threshold is reached) but slow enough when detecting that a new source is plugged in (depending on contact bounce during the insertion/removal of a power source). The slow delay is done with the 10 kHz internal oscillator.

At start-up, the cell is off and is turned on by the internal digital block.

With PWS_CR register (bits accessible via SPI), the application processor can force an input source to be selected. This may be used for testing the AT73C203 or by the application processor to force use of one of the batteries.

Using PWS_SR register, the application processor can read which supply is currently selected by the AT73C203.

If one input is not used (PSU, BAT1 or BAT2), it can be grounded. The corresponding unused output (GAPSU, GABAT1 or GABAT2) can be left unconnected in this case.

Power Switch Controller Electrical Specifications

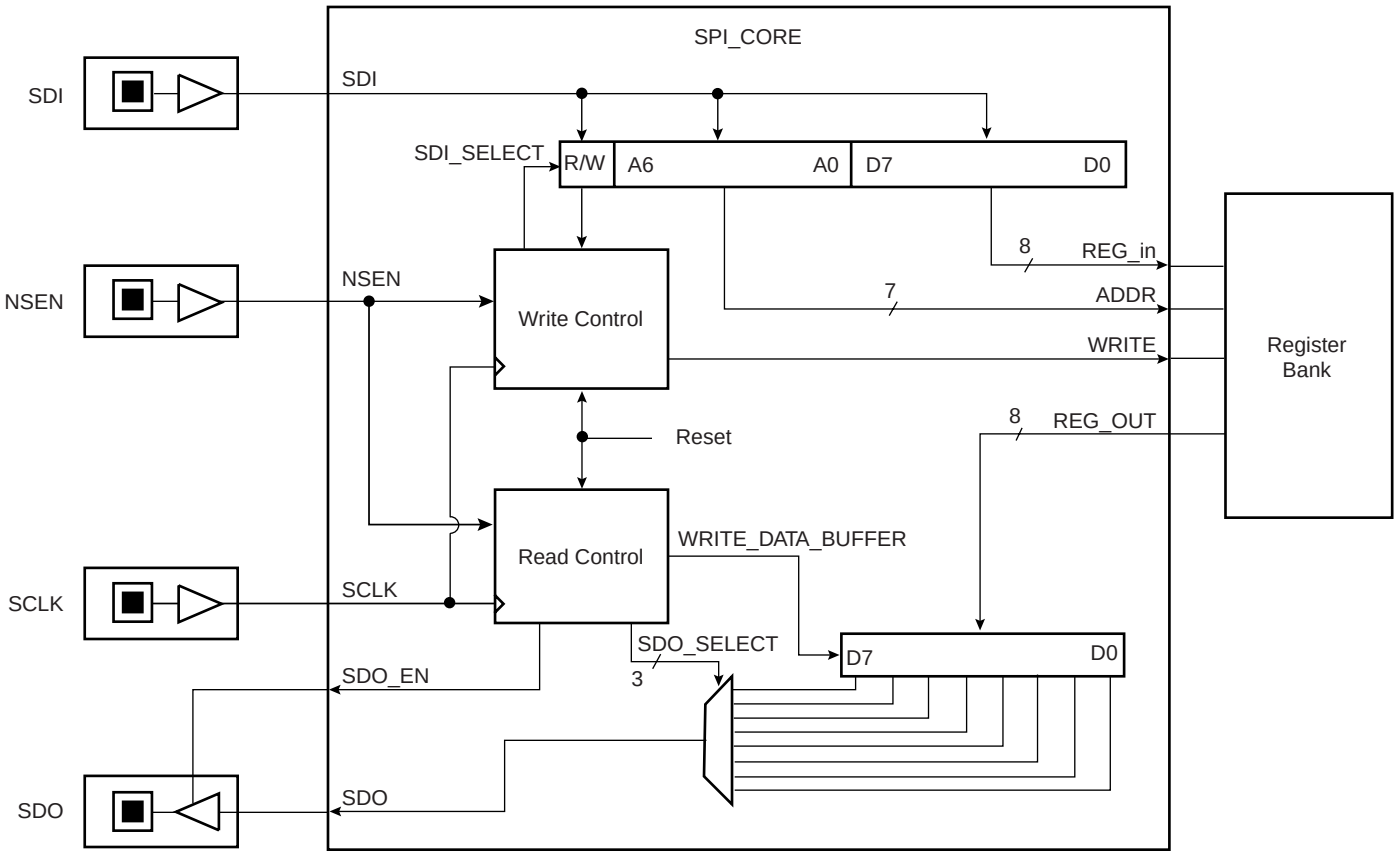
Table 4. Power Switch Controller Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Top	Operating temperature		-20		+85	°C
Psupio	Charger supply voltage			5	5.5	V
B_{AT2PIO}	Battery 2 supply voltage			3.6	4.35	V
B_{AT1PIO}	Battery 1 supply voltage			3.6	4.35	V
I_{PSU}	Current load on V_{DDPSU}				2	A
I_{CC}	Current consumption	onpio = 1, psupio = 5.5 V, B_{AT2PIO} = 4.35 V and B_{AT1PIO} = 4.35 V.			500	uA
I_{OFF}	Off current	onpio = 0 and precharg = 0			30	µA
t_{SW}	Switching time between two sources			1	5	µs
$V_{DDPSUMIN}$	Minimum voltage on V_{DDPSU}	onpio = 1, input selected = 3.1 V	2.85			V
$t_{STARTUP}$	Time to start			50	100	µs
$t_{PRECHAREGE}$	Time to precharge the V_{DDPSU} capacitor	onpio = 0 and precharg = 1, external load on V_{DDPSU} = 100 µA			100	ms
t_{DEBOUN_PSU}	Time for debouncing the PSU presence				100	ms
t_{DEBOUN_BAT2}	Time for debouncing the bat2 presence				100	ms
Psupio_r1	Voltage to consider PSU plugged in	Rising, V_{BG} = 1.23 V, Pcmcia = 0		3.43		V
Psupio_f1	Voltage to consider PSU removed	Falling, V_{BG} = 1.23 V, Pcmcia = 0		2.96		V
Psupio_hy1	PSU hysteresis	Input hysteresis, Pcmcia = 0		470		mV
Psupio_r2	Voltage to consider PSU plugged in	Rising, V_{BG} = 1.23 V, Pcmcia = 1		3.05		V
Psupio_f2	Voltage to consider PSU removed	Falling, V_{BG} = 1.23 V, Pcmcia = 1		2.80		V
Psupio_hy2	PSU hysteresis	Input hysteresis, Pcmcia = 1		250		mV
Bat2pio_r	Voltage to consider BAT2 available	Rising, V_{BG} = 1.23 V		3.20		V
Bat2pio_f	Voltage to consider BAT2 removed or flat	Falling, V_{BG} = 1.23 V		2.95		V
Bat2pio_hy	BAT2 hysteresis	Input hysteresis		250		mV
Bat1pio_r	Voltage to consider bat1 available	Rising, V_{BG} = 1.23 V		3.20		V
Bat1pio_f	Voltage to consider bat1 removed or flat	Falling, V_{BG} = 1.23 V		2.95		V
Bat1pio_hy	BAT1 hysteresis	Input hysteresis		250		mV

Serial Peripheral Interface (SPI)

The SPI interface between the system and the AT73C203 is detailed below.

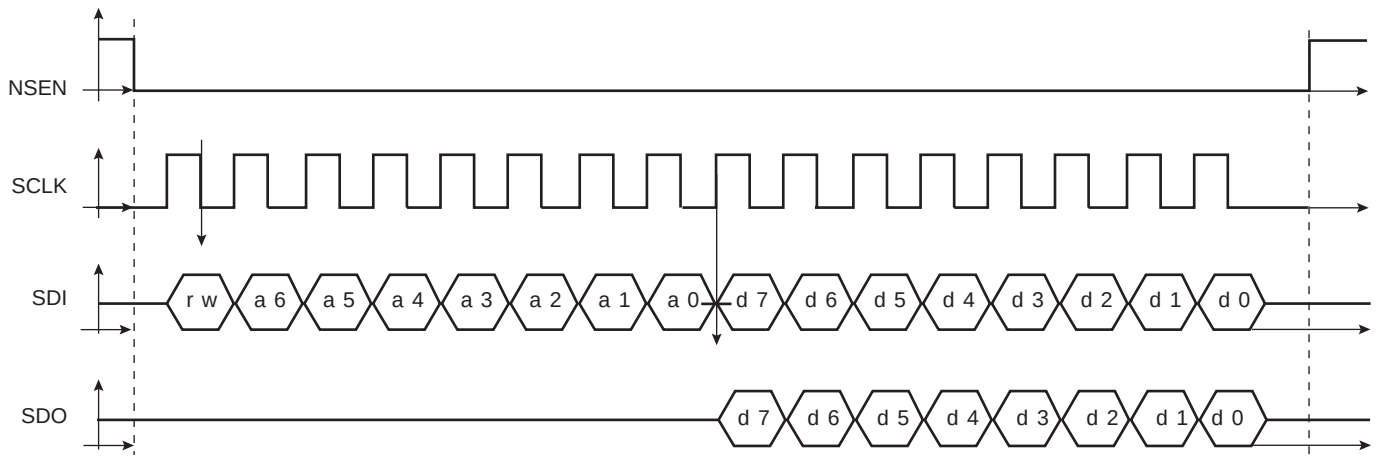
Figure 14. SPI Architecture



Protocol

The SPI is a 4-wire bidirectional asynchronous serial link providing 128 x 8 register access by the microprocessor. The SPI operates in slave mode only. The SPI protocol is as follows.

Figure 15. SPI Protocol



On SDI, the first bit is read/write. “0” indicates a write operation while “1” denotes a read operation. The seven following bits are used for the register address and the eight that follow are the write data. For both address and data, the most significant bit is the first one.

In case of a read operation, SDO first provides the contents of the read register, MSB.

The transfer is enabled by the NSEN signal active low. When the SPI is not operating, SDO output is set to high impedance to allow sharing of the CPU serial interface with other devices. The interface is reset at every rising edge of NSEN in order to return to an idle state, even if the transfer does not succeed.

The SPI is synchronized with the serial clock SCLK. Falling edge latches SDI input and rising edge shifts SDO output bits.

Timing for SPI Interface

SPI interface timings are as follows.

Figure 16. SPI Interface Timing Diagram

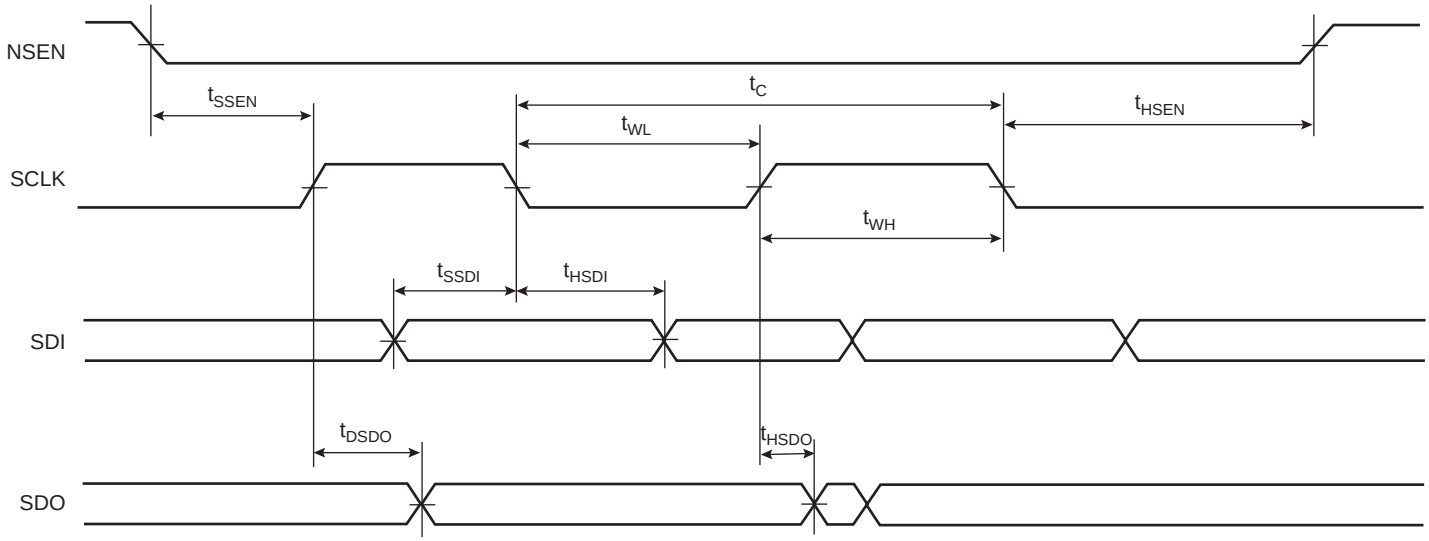


Table 5. SPI Timing Parameters

Timing Parameter	Description	Min	Max
t_C	SCLK min period	(1)$t_{SYSCLK}/2$	
t_{WL}	SCLK min pulse width low	50 ns	-
t_{WH}	SCLK min pulse width high	50 ns	-
t_{SSEN}	Setup time SEN falling to SCLK rising	50 ns	-
t_{HSEN}	Hold time SCLK falling to SEN rising	t_{SYSCLK}	-
t_{SSDI}	Setup time SDI valid to SCLK falling	20 ns	-
t_{HSDI}	Hold time SCLK falling to SDI not valid	20 ns	-
t_{DSDO}	Delay time SCLK rising to SDO valid	-	20 ns
t_{HSDO}	Hold time SCLK rising to SDO not valid	0 ns	-

Note: 1. t_{SYSCLK} = system clock period.

The frequency of SYS_CLK must be at least two times superior to that of SCLK.

After the end of reset (nPROC_RESET = 1), SYS_CLK must run at least during 500 µs before the first SPI access.

The minimum time for the USIM is one system clock period (t_{SYSCLK}).

As the clock domain is 900 kHz, to monitor function registers, two consecutive accesses at the same register must be superior to the 900 kHz period. Otherwise, only the second access will be taken into account.

The same approach is used for the charger registers but with 10 kHz.

RAIL1 DC/DC Converter 1.20 V, 1.2 A

Rail1 is a programmable buck DC/DC converter dedicated to the application processor core supply. The default voltage is 1.20 V. Three other values can be programmed: 1.3 V, 1.1 V and 1.5 V.

An external pin can select 1.75 V (SELDC175) output voltage with tuning: 1.80V, 1.70V and 1.65V. The entire cell is optimized for 1.20V.

When the cell is off, the output is pulled to ground.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 17. Rail1 Schematic

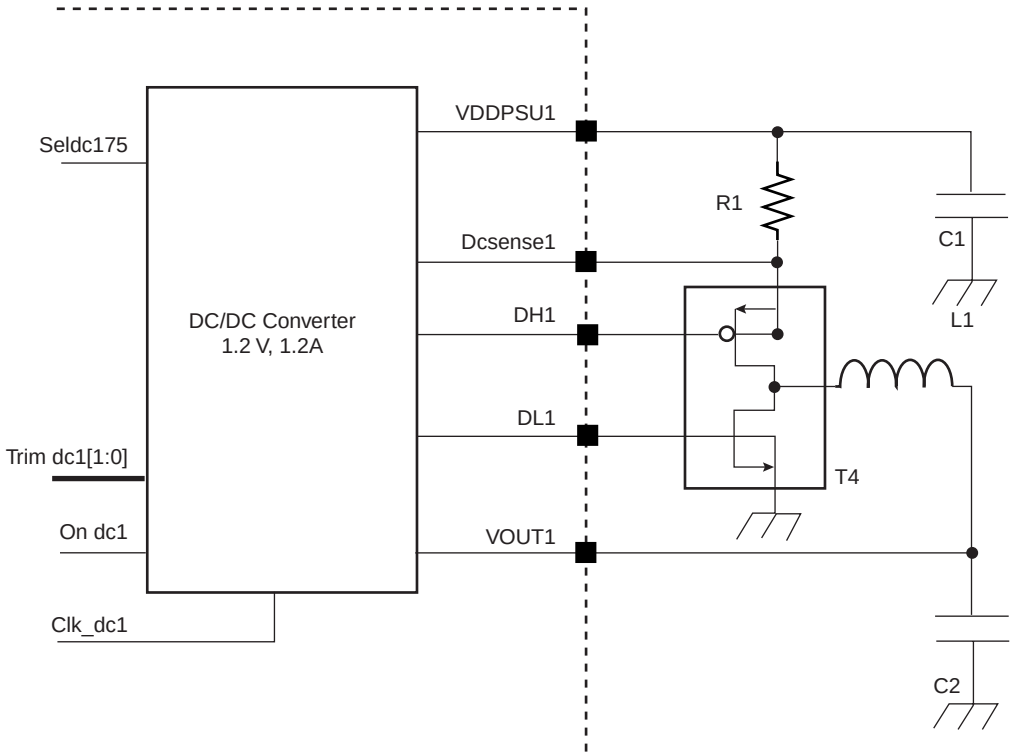


Table 6. Rail1 External Components

Schematic Reference	Reference
C1	22 µF Ceramic capacitor
C2	2 x 22 µF tantalum capacitors low ESR
L1	4.7 µH: SMT3106-471M ‘(Gowanda)
R1	100 mΩ ± 2% 250 mW
T4	Si5513DC

Rail1 Electrical Specifications

Rail1 can operate up to a load of 1.5 A if the R1 resistor is replaced by 80 mΩ ± 2%. Rail 1 can also operate at V_{IN} = 2.85 V.

Table 7. Rail1 Electrical Specifications

Symbol	Parameter	Condition (1.2V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 1200$ mA, $3\ V < V_{IN} < 5.5$ V		1.2		V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage			40		mV
Eff36	Efficiency	V_{IN} = 3.6 V, I_{LOAD} = 600 mA		83		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		85		%
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3 V to 5.5 V I_{LOAD} = 1200 mA		25		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} =5.5 V I_{LOAD} from 0 to 1200 mA		10		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5 V I_{LOAD} = 1200 mA		35		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3 V and V_{IN} = 5.5 V I_{LOAD} from 0 to 1200 mA		80		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5 V			1	µA
t_R	Rise Time	I_{LOAD} = 400 mA	0.01		10	ms
t_{R1200}	Rise Time	I_{LOAD} = 1200 mA	0.01		15	ms
t_{SETTLE}	Settling time for programmed voltage switching	Full load, 0.85 V to 1.3 V condition		70		µs
I_{SC}	Limitation current	$3V < V_{IN} < 5.5$ V	1.2			A

Rail2 DC/DC Converter 1.8V, 1.2 A

Rail2 is a programmable buck DC/DC converter dedicated to digital supply. The default voltage is 1.8 V. Three other values can be programmed: 1.85 V, 1.75 V and 1.70 V. An external pin can select 2.5 V output voltage (SELDC25) tuning: 2.6 V, 2.4 V and 2.3 V. The entire cell is optimized for 1.8 V

When the cell is off, the output is in high impedance state.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 18. Rail2 Schematic

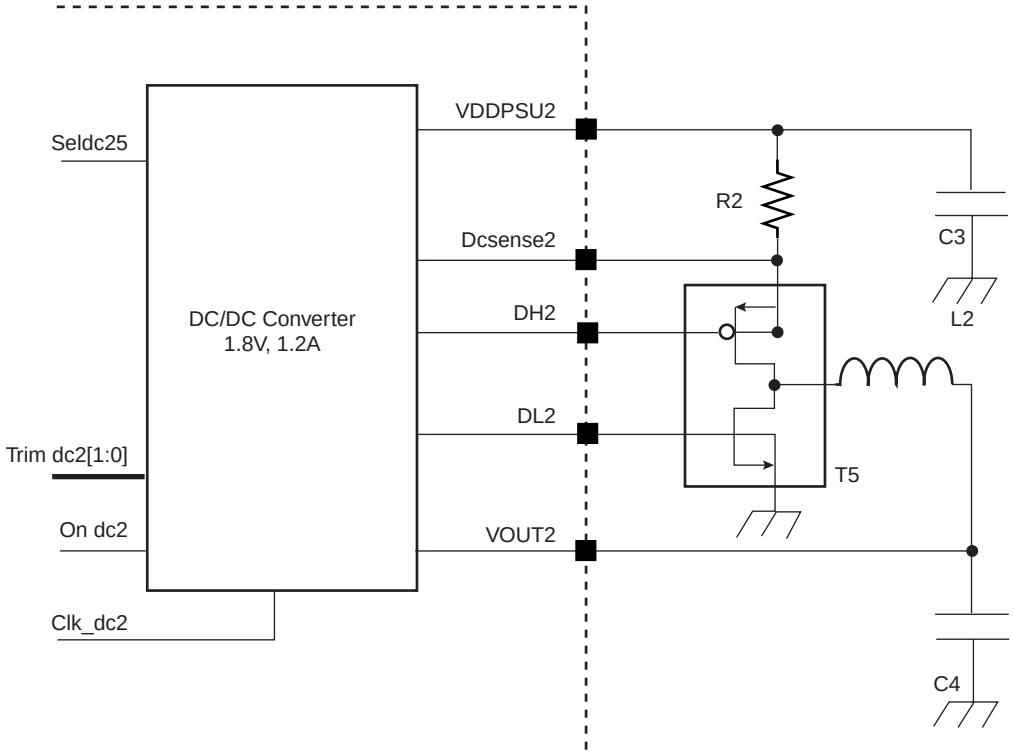


Table 8. Rail2 Preliminary External Components

Schematic Reference	Reference
C3	22 µF Ceramic capacitor
C4	2 x 22 µF tantalum capacitors low ESR
L2	10 µH: SMT3106-102M (Gowanda)
R2	100 mΩ ± 2% 250 mW
T5	Si5513DC

Rail2 Electrical Specifications

Rail 2 can also operate at V_{IN} = 2.85 V.

Table 9. Rail2 Electrical Specifications

Symbol	Parameter	Condition (1.2 V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 1200$ mA, $3\ V < V_{IN} < 5.5\ V$		1.8		V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage	I_{LOAD} = 1.2 A, V_{IN} = 3.6 V		200		mV
Eff36	Efficiency	V_{IN} = 3.6 V, I_{LOAD} = 600 mA		85		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		87		%

Table 9. Rail2 Electrical Specifications (Continued)

Symbol	Parameter	Condition (1.2 V Selected)	Min	Typ	Max	Unit
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3 V to 5.5 V, I_{LOAD} = 1200 mA		25		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5 V, I_{LOAD} from 0 to 1200 mA		10		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5 V, I_{LOAD} = 1200 mA		35		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3 V and V_{IN} = 5.5 V, I_{LOAD} from 0 to 1200 mA		80		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5 V			1	µA
t_R	Rise Time	I_{LOAD} = 1200 mA			1000	ms
t_{SETTLE}	Settling time for programmed voltage switching	Full load, 0.85 V to 1.3 V condition		50		µs
I_{SC}	Limitation current	3V < V_{IN} < 5.5 V	1.2	2		A

Rail3 DC/DC Converter 3.3V, 520 mA

Rail3 is a programmable buck DC/DC converter followed by a linear drop out regulator. The default value of the LDO is 3.3 V. Three other values can be programmed: 3.1 V, 3.2 V and 3.4 V. The entire cell is optimized for 3.3 V.

When the cell is off, the output is pulled to ground.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 19. Rail3 Schematic

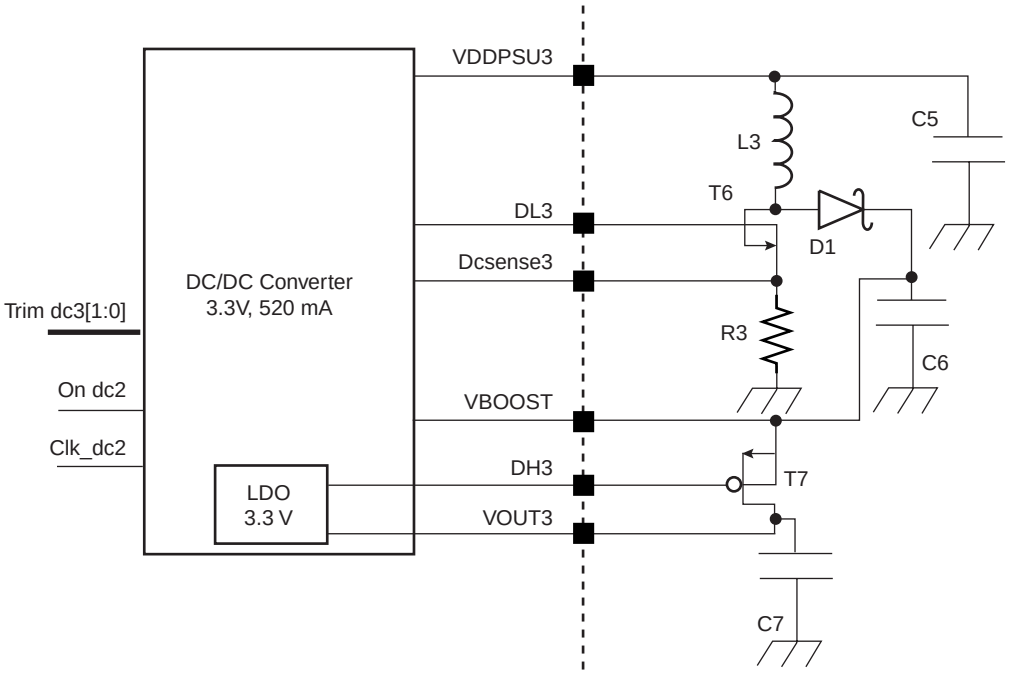


Table 10. Rail3 Preliminary External Components

Schematic Reference	Reference
C5,	22 µF ceramic capacitor
C6, C7	22 µF tantalum capacitor low ESR
D1	Schottky diode: MBRA120LT3 (ON Semiconductor)
L3	10 µH: SMT3106-102M (Gowanda)
R3	100 mΩ ± 2% 250 mW
T6	Si1400DL
T7	Si8401DL

Rail3 Electrical Specifications

Rail 3 can also operate at V_{IN} = 2.85 V.

Table 11. Rail3 Electrical Specifications

Symbol	Parameter	Condition (3.3 V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 520$ mA, $3 V < V_{IN} < 5.5 V$			520	V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage			70		mV
Eff36	Efficiency	V_{IN} = 3.6 V, I_{LOAD} = 430 mA		73		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 430 mA		65		%
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3 V to 5.5 V, I_{LOAD} = 430 mA		30		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3 V and V_{IN} = 5.5 V, I_{LOAD} from 52 to 468 mA		20		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5 V, I_{LOAD} = 300 mA		80		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3 V and V_{IN} = 5.5 V, I_{LOAD} from 0 to 300 mA		70		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5 V			1	µA
t_R	Rise Time	I_{LOAD} = 400 mA	0.01		100	ms
t_{SETTLE}	Settling time for programmed voltage switching	Full load, 3.1 V to 3.4 V condition		500		µs
I_{SC}	Limitation current	$3V < V_{IN} < 5.5 V$	520	850		mA

Rail 4 DC/DC Converter 0.9 V, 1.2A

Rail4 is a programmable buck DC/DC converter dedicated to the supply of advanced core processing units. The default voltage is 0.9 V. Three other values can be programmed: 1.2 V, 0.87 V and 1.1 V. The entire cell is optimized for 0.9 V.

When the cell is off, the output is in high impedance state.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 20. Rail4 schematic

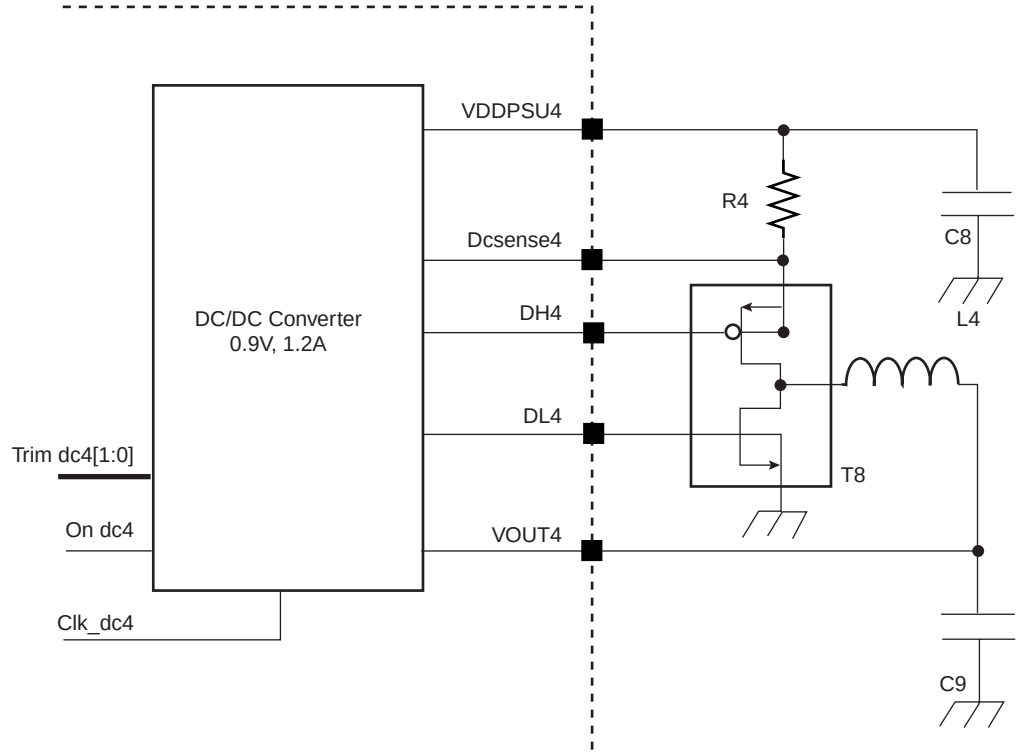


Table 12. Rail4 Preliminary External Components

Schematic Reference	Reference
C8,	22 µF ceramic capacitor
C9	2 x 22 µF tantalum capacitor low ESR
L4	4.7 µH: SMT3106-47M (Gowanda)
R4	100 mΩ ± 2% 250 mW
T8	Si5513DC

Rail4 Electrical Specifications

Rail 4 can also operate at V_{IN} = 2.85 V.

Table 13. Rail4 Electrical Specifications

Symbol	Parameter	Condition (0.9 V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 1200$ mA, $3\ V < V_{IN} < 5.5\ V$		0.9		V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage	I_{LOAD} = 1.2 A, V_{IN} = 3.6 V		35		mV
Eff36	Efficiency	V_{IN} = 3.6 V, I_{LOAD} = 600 mA		78		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		80		%

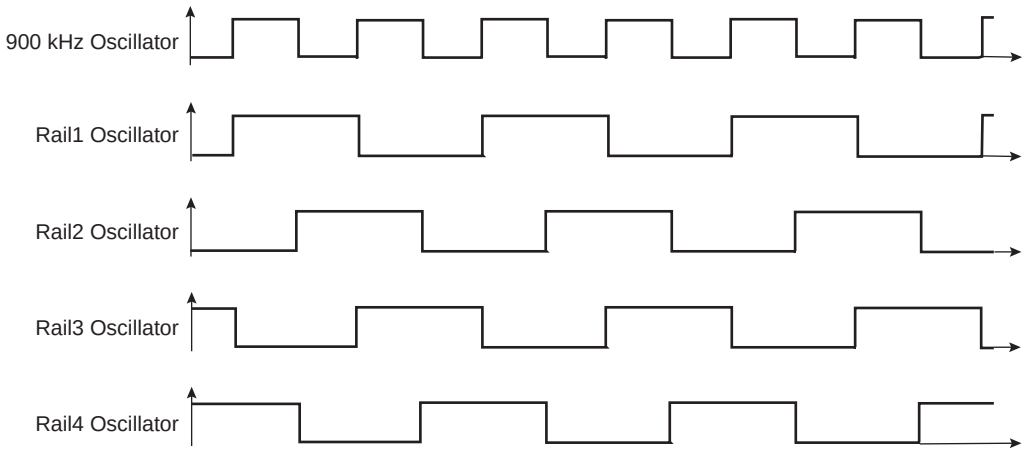
Table 13. Rail4 Electrical Specifications (Continued)

Symbol	Parameter	Condition (0.9 V Selected)	Min	Typ	Max	Unit
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3 V to 5.5 V, I_{LOAD} = 1200 mA		20		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3 V and V_{IN} = 5.5 V, I_{LOAD} from 120 to 1200 mA		10		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5 V, I_{LOAD} = 1200 mA		35		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3 V and V_{IN} = 5.5 V, I_{LOAD} from 120 to 1200 mA		85		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5 V			1	µA
t_R	Rise Time	I_{LOAD} = 1200 mA			3000	µs
tsettle	Settling time for programmed voltage switching	Full load, 0.84 V to 0.93 V condition		50		µs
I_{SC}	Limitation current	3V < V_{IN} < 5.5 V	1200	2		mA

900 kHz Oscillator and Clock Distribution

The 900 kHz oscillator provides the clock to all DC/DC converters. The clock distributor provides phased clocks to the DC/DC converters to avoid them switching at the same time.

Figure 21. 900 kHz Oscillator Distribution

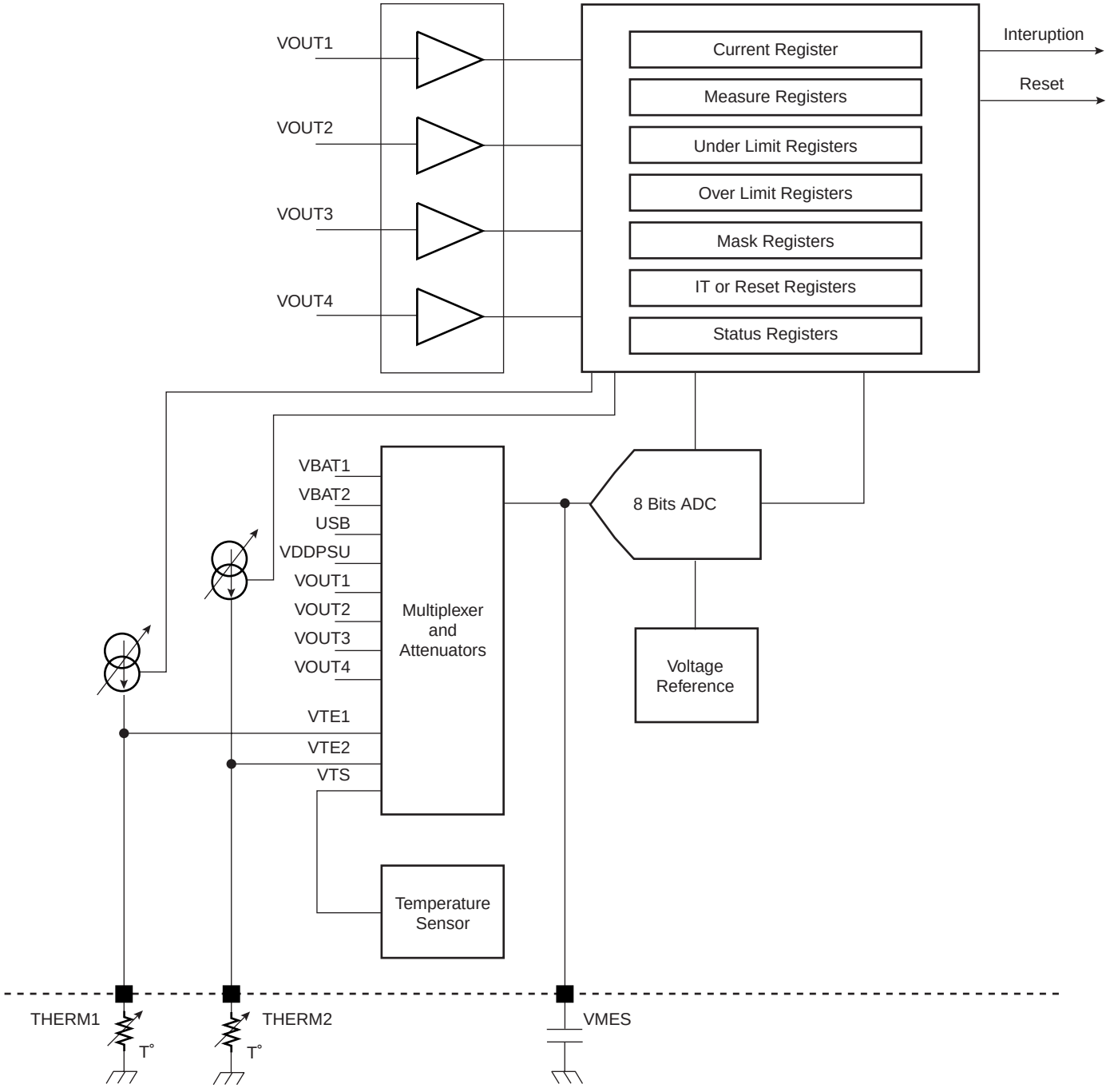


Monitoring Voltage and Temperature Function

The AT73C203 integrates voltage monitoring and temperature monitoring functionality, thus enabling the application processor to know when an under-voltage or over-temperature error condition occurs. The application processor can control this situation by changing the thresholds and programming an interrupt or a reset in the event and error condition occurs.

All the controls are performed via registers accessed via the SPI.

Figure 22. Voltage and Temperature Monitoring Architecture



Analog to Digital Converter and Multiplexer

An internal 8-bit analog to digital converter is used to measure the different voltages. The analog to digital converter has eleven internal inputs listed as follows:

- V_{BAT1} (internal battery)
- V_{BAT2} (external battery)
- USB (USB supply)
- V_{DDPSU} (output of the power switch)
- V_{OUT1} (output of Rail1)

- V_{OUT2} (output of Rail2)
- V_{OUT3} (output of Rail3)
- V_{OUT4} (output of Rail4)
- V_{TE1} (voltage on thermistor 1)
- V_{TE2} (voltage on thermistor 2)
- V_{TS} (output of the internal temperature sensor)

An external capacitor (C21) on V_{MES} pin enables filtering of the ADC input and provides immunity to high frequency noise.

These inputs are multiplexed into the analog to digital converter. This has a resolution of eight bits. The basic input range is 0.6 V to 2.25 V (typical) but the inputs have built-in attenuators to allow measurements without external components.

Take note that no attenuator is present for V_{OUT1}, V_{OUT4}, V_{TE1}, V_{TE2} and V_{TS}.

Monitoring Voltage and Temperature Electrical Characteristics

All bridge resistance values are given with ± 30% of global variations and mismatch values of less than 1%. All ratios will be confirmed during the design process.

Table 14. Monitoring Bridge (Attenuators) Electrical Specifications

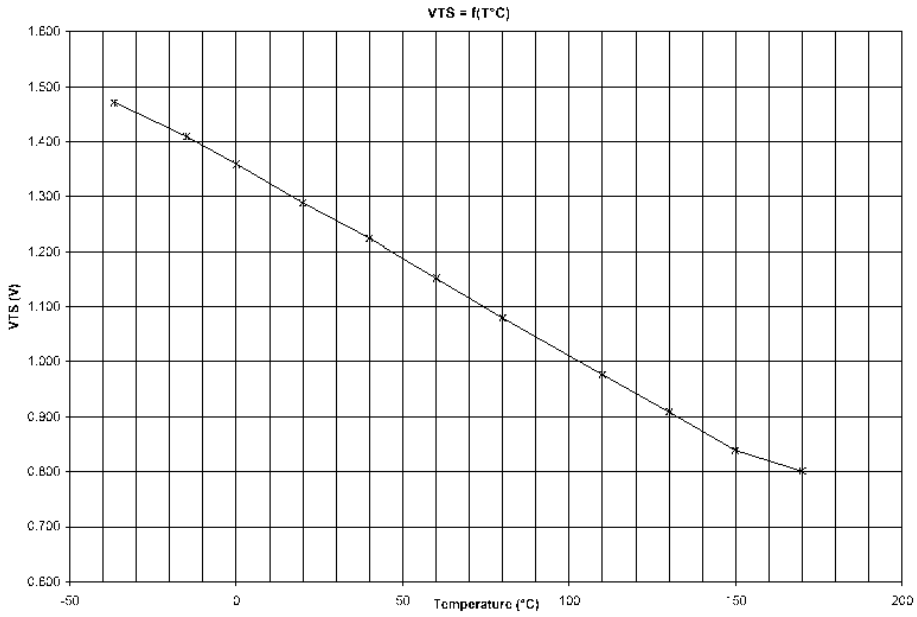
Symbol	Parameter	Condition	Min	Typ	Max
R_{ATBAT1}	Ratio V_{BAT1}	0V ÷ 5.5 V		2.5	
R_{ATBAT2}	Ratio V_{BAT2}	0V ÷ 5.5 V		2.5	
R_{ATUSB}	Ratio USB	0V ÷ 5.5 V		2.5	
R_{VDDPSU}	Ratio V_{DDPSU}	0V ÷ 2.5 V		2.5	
R_{OUT2}	Ratio V_{OUT2}	0V ÷ 3.4 V		2.0	
R_{OUT3}	Ratio V_{OUT3}	0V ÷ 5.5 V		2.0	

Typical sensor characteristic law: $V(T) = 1.31 - 3.6 \times 10^{-3} \times (T - 27)$

Table 15. Temperature Sensor Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.4	2.5	2.6	V
I_{CC}	Supply current	V_{CC} = 2.5 V			100	µA
DJ	Temperature sense dynamic		0		80	°C
εT	Absolute error	ϑ = 55°C			±10	°C
ΔT/Δϑ	Differential error	10% - 90%, Δϑ = [45°C, 55°C]			±5%	
V/ϑ	Voltage dynamic range	10% - 90%, Δϑ = [0°C, 80°C]			1	V
ΔV/Δϑ	Sensor voltage sensitivity		1		20	mV/°C
V_{TNOM}	Sensor output voltage @27°C	ϑ = 27°C	1.23		1.33	V

Figure 23. Typical Sensor Characteristics



Digital Core Function

By default, the digital core function is disabled. To enable it, the MON_ON bit in register MON_CR must be set to 1. A transition from 0 to 1 of MON_ON resets all the internal registers.

When the digital core function is on, the internal digital core automatically starts the monitoring sequence. It cycles sequentially through the measurement of the analog inputs. Eight measurements are taken, then the digital core computes the average of these eight values to reduce noise before moving to the next input.

Average values from these inputs are stored in value registers. These can be read out through the SPI bus. Measurements are updated every 2 ms (approximate).

Table 16. Value Registers

MON_VBAT1_MEAS	MON_VOUT3_MEAS
MON_VBAT2_MEAS	MON_VOUT4_MEAS
MON_USB_MEAS	MON_VTE1_MEAS
MON_VDDPSU_MEAS	MON_VTE2_MEAS
MON_VOUT1_MEAS	MON_VTS_MEAS
MON_VOUT2_MEAS	

To assure better accuracy, a calibration should be made during the printed circuit board test by injecting an accurate voltage into the analog inputs and checking the voltage read by the ADC. By comparing the voltage read by the ADC to the theoretical value stored in an external flash memory, the software can remove the internal offset.

An automatic comparison is launched when the monitoring function is enabled. The digital core compares the measurement with programmed limits stored in the limit registers.

Table 17. Limit Registers

MON_VBAT1_UNDL	MON_VBAT1_OVL
MON_VBAT2_UNDL	MON_VBAT2_OVL
MON_USB_UNDL	MON_USB_OVL
MON_VDDPSU_UNDL	MON_VDDPSU_OVL
MON_VOUT1_UNDL	MON_VOUT1_OVL
MON_VOUT2_UNDL	MON_VOUT2_OVL
MON_VOUT3_UNDL	MON_VOUT3_OVL
MON_VOUT4_UNDL	MON_VOUT4_OVL
MON_VTE1_UNDL	MON_VTE1_OVL
MON_VTE2_UNDL	MON_VTE2_OVL
MON_VTS_UNDL	MON_VTS_OVL

The results of out-of-limit comparisons are stored in the status registers, which can be read over the SPI to flag an out-of-limit condition.

Table 18. Status Registers

MON_SR1	MON_SR2

When an out-of-limit comparison occurs, an interrupt or a reset can be programmed via mask and interrupt/reset registers.

Table 19. Mask and Interrupt /Reset Registers

MON_MR1	MON_IR1
MON_MR2	MON_IR2

Thermistor Measurement

Two external NTC thermistors are used to measure the temperature of the battery. The resistance of the NTC is proportional to the temperature.

To measure the resistance and determine the temperature two 6-bit current DACs are integrated into the AT73C203.

The software can program the current flowing through thermistors 1 and 2 via MON_VTE1_CURR and MON_VTE2_CURR registers and can then read back the voltage through MON_VTE1_MEAS and MON_VTE2_MEAS registers. The temperature can then be estimated by the microprocessor.

Current DAC Electrical Specifications

The 6-bit DAC parameters are shown in Table 20 below.

Table 20. Current DAC Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{TEXCURR<0>}$	$V_{TEXCURR<0>}$		6	7.5	9	µA
$V_{TEXCURR<1>}$	$V_{TEXCURR<1>}$		12	15	18	µA
$V_{TEXCURR<2>}$	$V_{TEXCURR<2>}$		24	30	36	µA
$V_{TEXCURR<3>}$	$V_{TEXCURR<3>}$		48	60	72	µA
$V_{TEXCURR<4>}$	$V_{TEXCURR<4>}$		96	120	144	µA
$V_{TEXCURR<5>}$	$V_{TEXCURR<5>}$		192	240	288	µA
Lincurr	Linearity I_{OUT} = f(Rl)	Rl: resistive load to ground V_{OUT} = 0 to 2.35 V			2	%

Comparator Electrical Specifications

In parallel to the DAC, a comparator for each digital core supply rail (V_{OUT1}, V_{OUT2}, V_{OUT3} and V_{OUT4}) is used as a real time supply rail brownout detector for a drop.

The value of the comparator is not programmable but the threshold moves according to the voltage chosen. (Refer to the DC/DC converter specifications specific to each supply rail.)

Table 21. Comparator Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{TEXCURR<0>}$	$V_{TEXCURR<0>}$		6	7.5	9	µA
$V_{TEXCURR<1>}$	$V_{TEXCURR<1>}$		12	15	18	µA
$V_{TEXCURR<2>}$	$V_{TEXCURR<2>}$		24	30	36	µA
$V_{TEXCURR<3>}$	$V_{TEXCURR<3>}$		48	60	72	µA

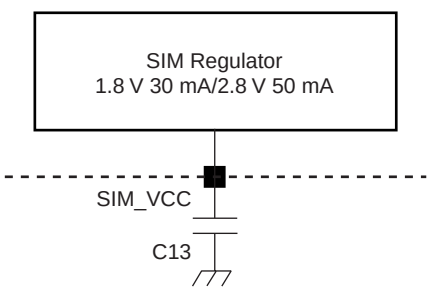
USIM Interface

A Low Drop Out (LDO) voltage regulator provides an accurate power supply to the SIM card. Two nominal values can be programmed: 1.8 V or 2.8 V. It is supplied by V_{DDPSU}.

When the cell is off, the output is pulled to ground.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 24. USIM Regulator



External components: 2.2 µFX5R ± 10% output capacitor

USIM 1.8 V Regulator Electrical Specifications

The USIM 1.8 V regulator complies with ETS TS 102 221, sections 5 and 6.

Table 22. USIM 1.8 V Regulator Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDSIM}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{SIM}	Output Voltage	$0 < I_{LOAD} < 30$ mA, $3\ V < V_{DDSIM} < 5.5\ V$	1.75	1.80	1.85	V
I_{OUT}	Output Current				30	mA
V_{DROP}	Min Supply for SIM_VCC > 1.75 V	I_{LOAD} = 50 mA	1.90			V
	Transient Line Regulation	$t_R = t_F$ = 5 µs, V_{DDSIM} from 3V to 5.5 V, I_{LOAD} = 30 mA			40	mV
	Transient Load Regulation	$t_R = t_F$ = 5 µs, V_{IN} = 2.97 V, I_{LOAD} from 3 to 27 mA			40	mV
I_{CC}	Quiescent Current	V_{DDSIM} = 5.5V			50	µA
I_{CC}	Powerdown Current	V_{DDSIM} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 30 mA 10% - 90% V_{OUT}			500	µs
I_{SC}	Limitation Current	$3V < V_{DDSIM} < 5.5\ V$	30			mA
V_N	Output Noise	BW: 10 Hz to 100 kHz Including bandgap noise			1	mVrms

USIM 2.8 V Regulator Electrical Specifications

The USIM 2.8 V regulator complies with ETS TS 102 221, sections 5 and 6.

Table 23. USIM 2.8 V Regulator Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDSIM}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{SIM}	Output Voltage	$0 < I_{LOAD} < 30$ mA, $3\ V < V_{DDSIM} < 5.5\ V$	2.77	2.8	2.83	V
I_{OUT}	Output Current				30	mA
V_{DROP}	Min Supply for SIM_VCC > 1.75 V	I_{LOAD} = 50 mA	2.85			V
	Transient Line Regulation	$t_R = t_F$ = 5 µs, V_{DDSIM} from 3V to 5.5 V, I_{LOAD} = 30 mA			30	mV
	Transient Load Regulation	$t_R = t_F$ = 5 µs, V_{IN} = 2.97 V, I_{LOAD} from 3 to 27 mA			30	mV
I_{CC}	Quiescent Current	V_{DDSIM} = 5.5V			50	µA
I_{CC}	Powerdown Current	V_{DDSIM} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 30 mA 10% - 90% V_{OUT}			500	µs
I_{SC}	Limitation Current	$3V < V_{DDSIM} < 5.5\ V$	50			mA
V_N	Output Noise	BW: 10 Hz to 100 kHz Including bandgap noise			1	mVrms

Charger Control

The AT73C203 is able to control the charging of two Lithium Ion batteries from either a PSU or USB supply.

Charging can occur in two different modes as follows:

- Stand-alone mode. The AT73C203 preconditions the battery independently of the application processor (the application processor is not powered up).
- Controlled mode. The application processor controls the charging phases via registers accessed via the SPI.

Figure 25. Charger Control Schematic

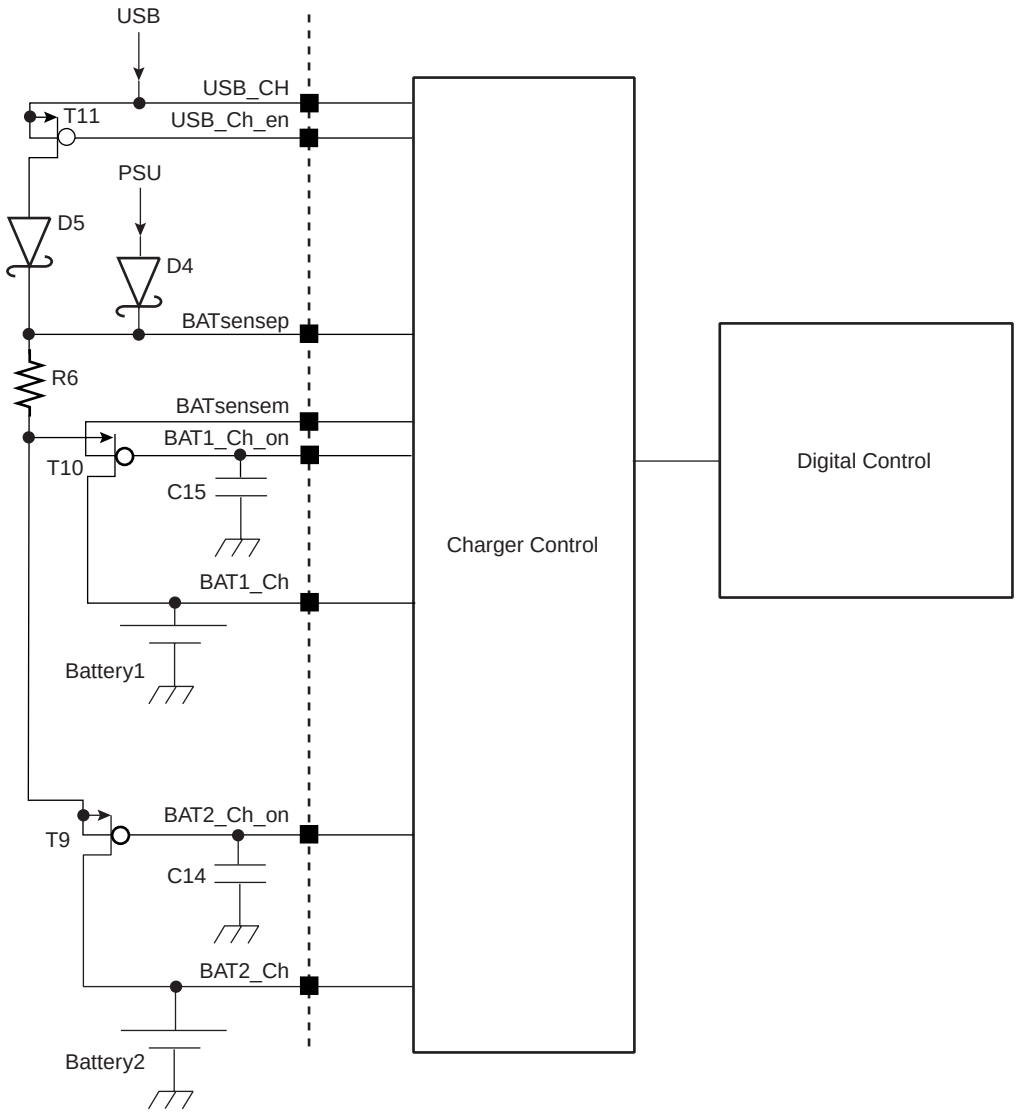


Table 24. Charger Preliminary Components

Schematic Reference	Reference
BAT1	Li-ion battery 4.2 V-3.0 V. Permanently connected to module
BAT2	Li-ion battery 4.2 V-3.0 V. Optional battery
C14, C15	10 nFX56 ± 10% ceramic capacitor
D4, D5	MBRA120LT3 (ON Semiconductor)
R6	200 mΩ +/- 2% 50 mW
T7	Si8401DL
T11	Si1405DL

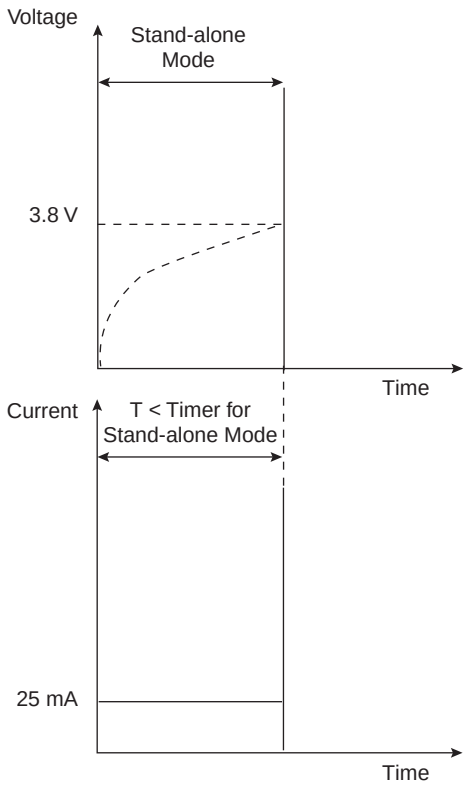
Charge Principles

Stand-alone Mode

The stand-alone mode occurs only when the USB is plugged in and there is no battery 2 (or it is flat) and battery 1 is flat and the PSU unplugged. (See"State Machine Description" on page 15 and Figure 28 on page 44).The AT73C203 can then choose to precharge battery 1 if the temperature range is within limits. The stand-alone mode is terminated if the charge timer expires or if the voltage of battery 1 goes above 3.8 V.

The digital core (via the USB_SCR register) can put the AT73C203 into a mode in which the digital core is off and battery 1 is charged (25 mA) through the USB until 4.1 V.

Figure 26. Stand-alone Mode

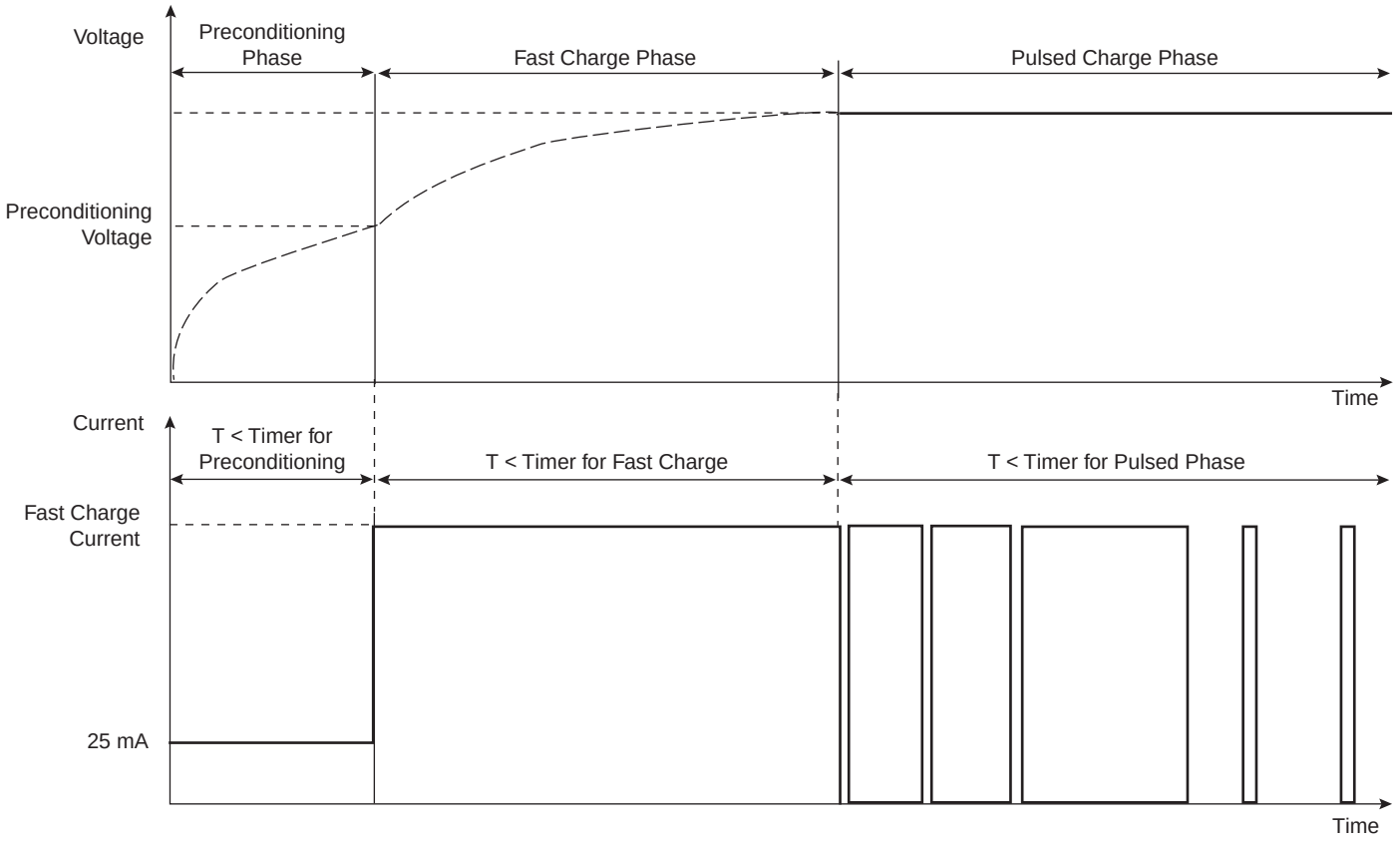


Controlled Mode

After the digital reset phase, the application processor can launch a charge phase. By default the charge phase is stopped when the application processor wakes up.

The charge control includes three charging phases (preconditioning, fast charge and pulsed charge) during which the application processor must check via the monitoring function that the operating temperature is within allowable limits for battery charging.

Figure 27. Controlled Mode



Preconditioning Phase

Battery 1 and Battery 2 can be preconditioned to a predetermined voltage from either the PSU or USB source. Precondition current is set to 25 mA.

To enable the precondition phase, the application processor must use the charger control register.

To program the preconditioning voltage threshold, the application processor must use an interrupt, which can be programmed for battery 1 and battery 2 with the over limit registers included in the monitoring function.

A safety timer (CHA_STR_CR) can be launched during this phase. If the safety timer expires, an interrupt is launched and the pre-conditioning phase is automatically stopped. If the pre-conditioning voltage threshold has been reached, the application processor should put the charger into the fast charge phase.

Fast Charge Phase

To enable the fast charge phase, the application processor must use the charger control register. The battery is charged at a constant current that can be adjusted (CHA_CURR in the CHA_MR in register). Note that battery 1 and battery 2 can not be in the fast charge phase at the same time.

The fast charge is automatically stopped when the battery voltage reaches the regulation voltage. The regulation voltage can be trimmed. By default, the voltage is 4.2 V. When this voltage is reached an interrupt is sent to warn the microprocessor.

A safety timer (CHA_STR_CR) can be launched during this phase.

Pulsed Charge Phase

To enable the pulsed charge phase, the application processor must use the charger control register. Note that battery 1 and battery 2 can not be in pulsed charge phase at the same time.

The charger control uses a hysteretic algorithm with minimum on-times and minimum off-times of the external PMOS. These minimum on-times and off-times can be programmed via registers CHA_TMINON and CHA_TMINOFF.

The battery voltage is sampled every 0.3 millisecond (typical). If the battery voltage is less than the battery regulation voltage, the external PMOS FET either turns on or, if already on, remains on. If the battery voltage is greater than, or equal to, the regulation voltage threshold, the FET either turns off or, if already off, remains off until the next sample.

At the beginning of the pulsed charge phase, the current stays on for many consecutive cycles between single off periods. As the battery continues to charge, the percentage of time spent in the "current-on" mode decreases. At the end of the pulsed phase, the current stays off for many cycles between single "on" pulses.

This phase is automatically stopped when the duty ratio of "on" cycles to "off" cycles falls below a threshold which must be programmed trough register CHA_TR. Additionally, an interrupt is sent to warn the microprocessor.

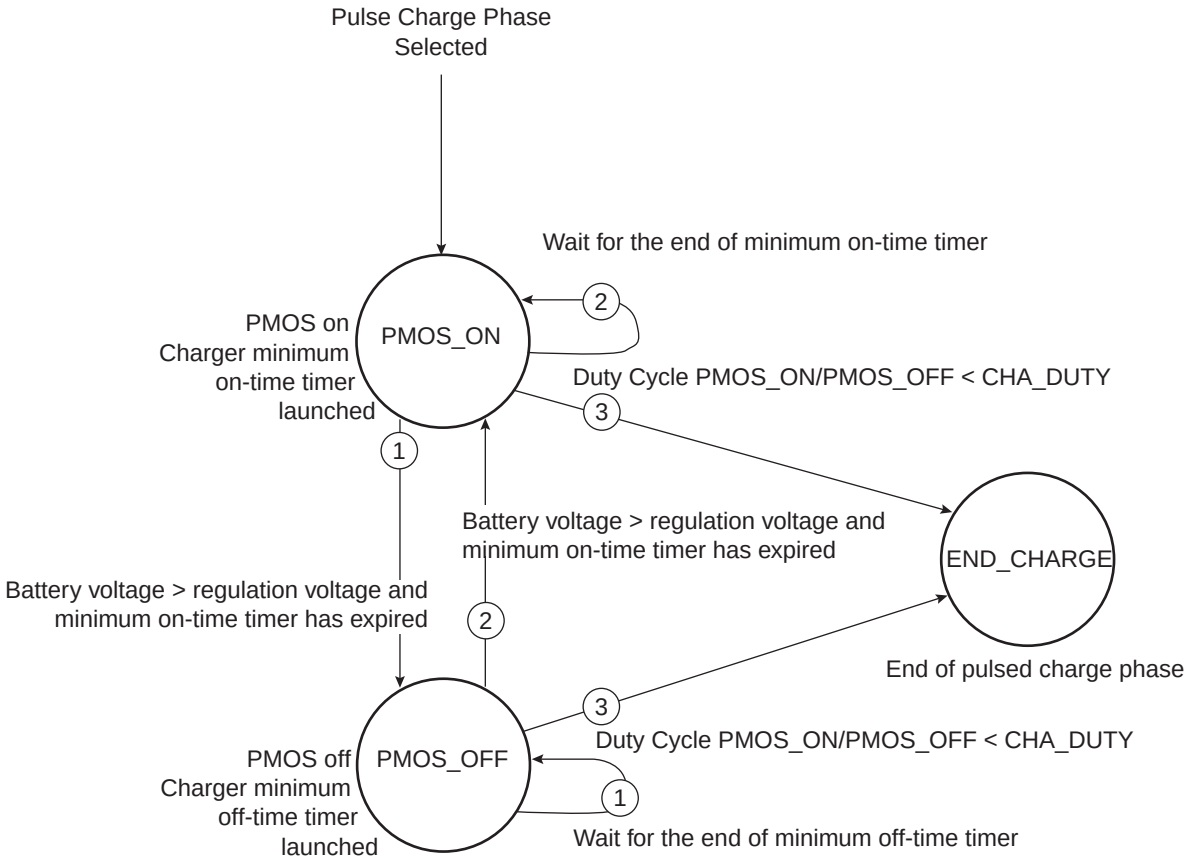
For safety, a timer (CHA_STR_CR) can be launched during this phase.

If this timer expires, an interrupt is launched and the pulsed charge phase is automatically stopped.

The “Start-up State Machine Pulsed Charge Phase” shown in Figure 28 on page 44 presents a summary of the pulsed charge phase. Refer also to the “State Machine Description” on page 15 for more information on the pulsed charge phase.

The parameters (CHA_TMINON, CHA_TMINOFF and CHA_TR) can be trimmed in order to be adapted to the battery. To properly choose the parameters, a test must been done with the real battery. At the end of top-off mode, it is preferable to use a small current (100 mA). A good default value seems to be 200 ms for CHA_TMINON and CHA_TMINOFF and a duty cycle threshold of 1/64.

Figure 28. Start-up State Machine Pulsed Charge Phase



Watchdog

For safety, during any phase of the controlled mode a watchdog is launched automatically. The application processor must rearm the watchdog via the charger control register, CHA_CR, at least every 13 s. If during 13 s (typical time), the watchdog has not been rearmed, the charge is stopped.

Charger Control Electrical Specifications

Table 25. Charger Control Electrical Specifications

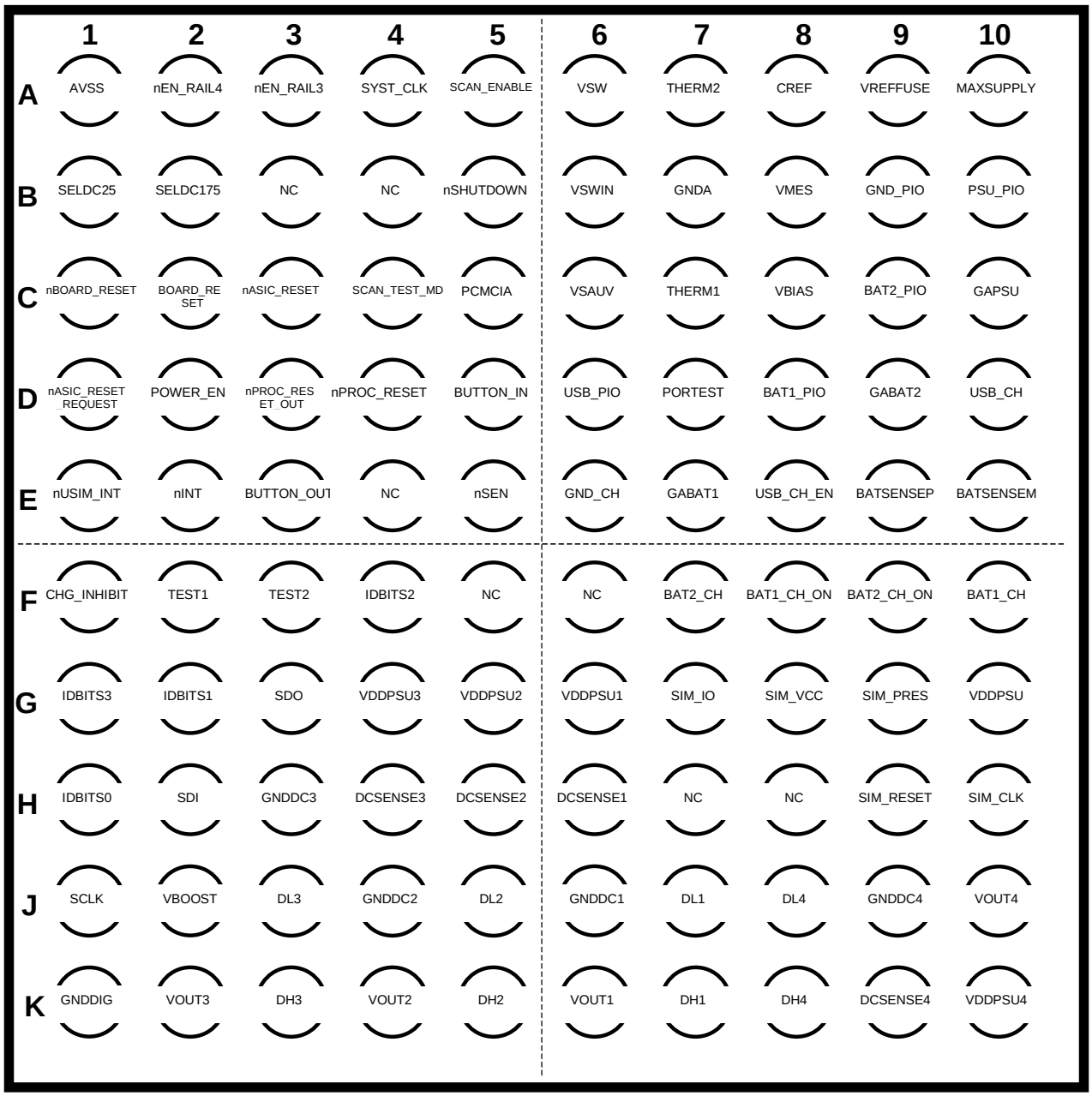
Symbol	Parameter	Condition	Min	Typ	Max	Units
PSU	Charger Voltage		4.90	5.0	5.10	V
USB	USB Voltage		4.62	5.0	5.25	V
$I_{PRECOND}$	Preconditioning Current	USB or PSU		25		mA
I_{CH}	Charge Current	CHA_CURR = 11		500		mA
		CHA_CURR = 10		300		mA
		CHA_CURR = 01		200		mA
		CHA_CURR = 00		100		mA
V_{REGTH}	Regulation Voltage Threshold	CHA_VOLT_TRIM =000		4.20		V
		CHA_VOLT_TRIM =001		4.170		V

Table 25. Charger Control Electrical Specifications (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
		CHA_VOLT_TRIM = 010		4.130		V
		CHA_VOLT_TRIM = 011		4.10		V
		CHA_VOLT_TRIM = 100		4.23		V
		CHA_VOLT_TRIM = 101		4.26		V
		CHA_VOLT_TRIM = 110		4.30		V
		CHA_VOLT_TRIM = 111		4.07		V
Hystbat1	Input hysteresis			2		mV
	Timer for stand alone mode			1		h
	Threshold voltage for stand alone mode			3.8		V
$t_{ACCURACY}$	Timing accuracy			±25		%
I_{CC}	Current consumption			1		mA

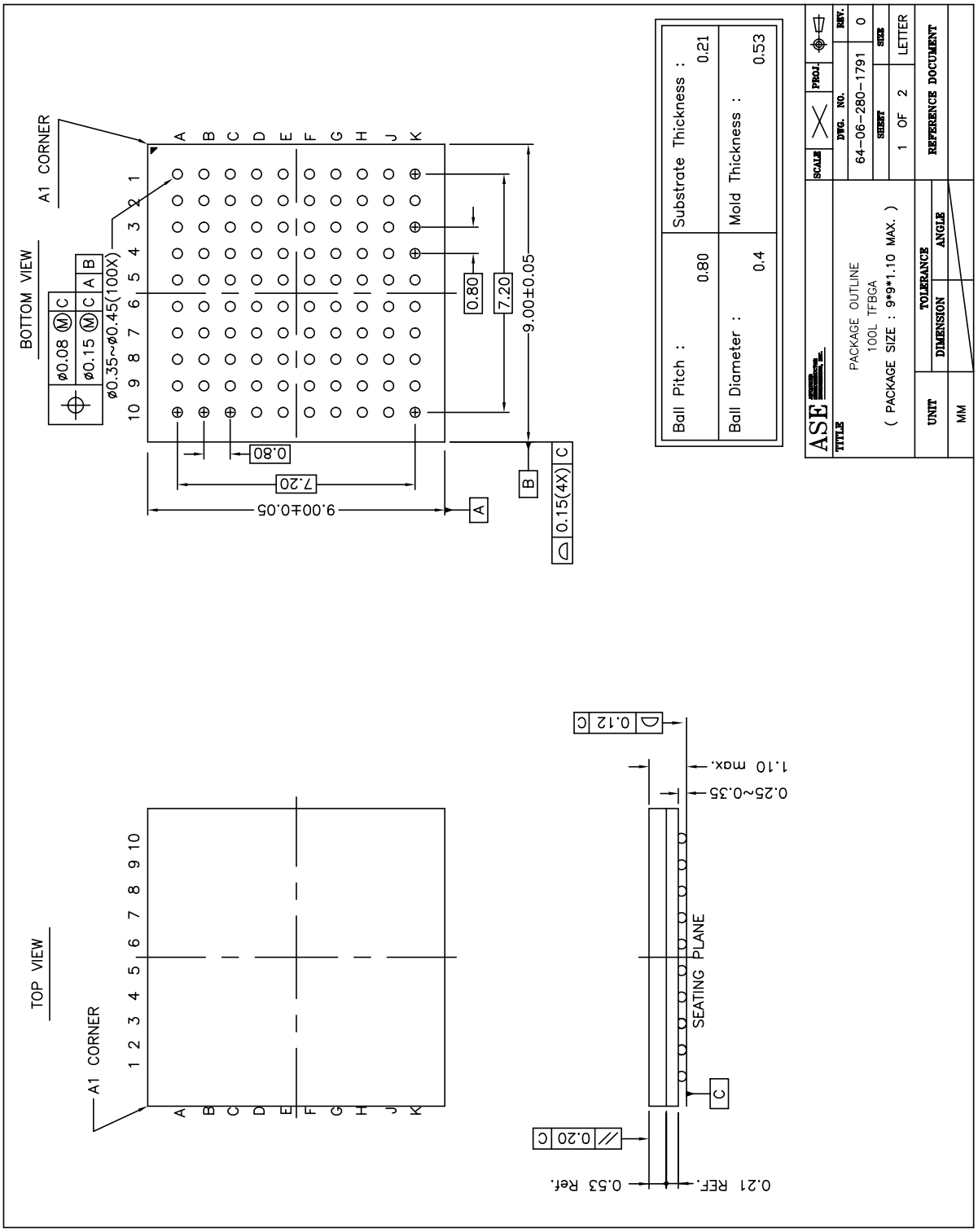
Package Outline (Top View)

Figure 29. 10 x 10 balls, 0.8mm Pitch BGA Package on 9 x 9mm Body Size for AT73C203



Package Specification

Figure 30. AT73C203 Package Specification



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