TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74AC166P, TC74AC166F, TC74AC166FN

8 – BIT SHIFT REGISTER (P – IN, S – OUT)

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74AC166 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

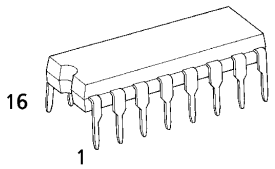
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8 - bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

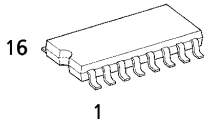
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

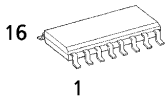
- High Speed ····· f_{MAX} = 170MHz(typ.)at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.)at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Pin and Function Compatible with 74HC166



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

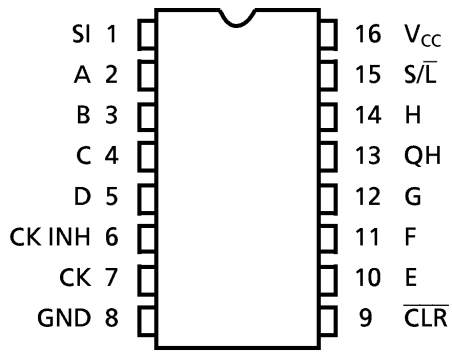


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



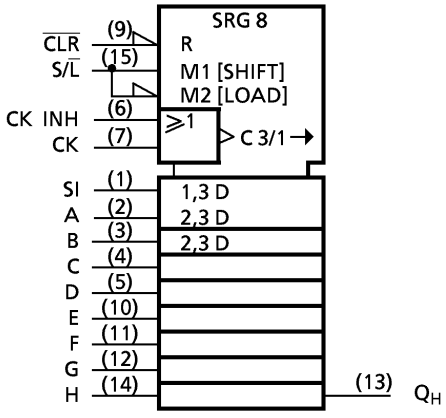
FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



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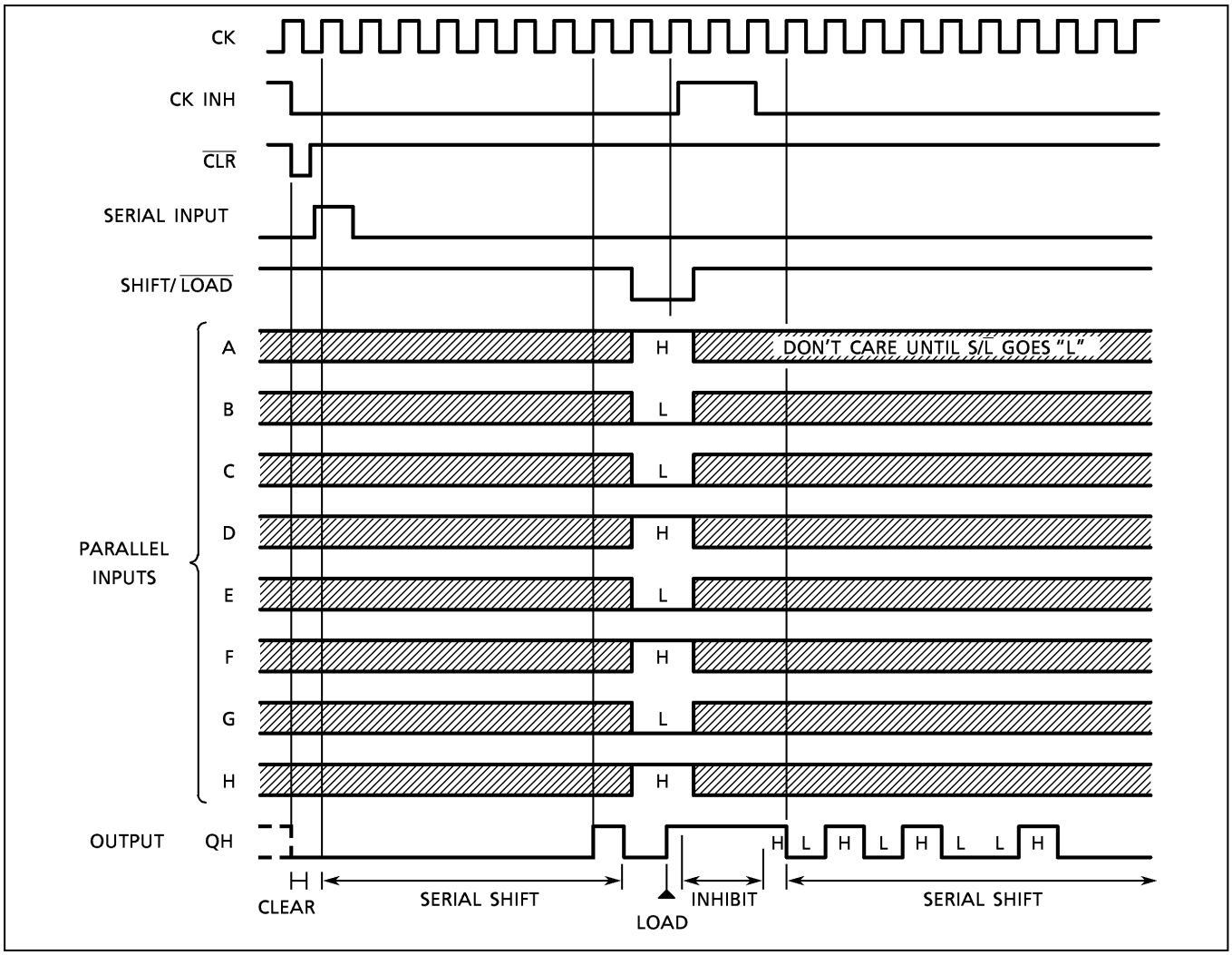
TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
$\overline{CLR}$	SHIFT/ $\overline{LOAD}$	CK INH.	CK	SERIAL IN	PARALLEL A ····· H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	↓	X	X	NO CHANGE	
H	L	L	↑	X	a ····· h	a b	h
H	H	L	↑	H	X	H QAn	QGn
H	H	L	↑	L	X	L QAn	QGn
H	X	H	X	X	X	NO CHANGE	

X : Don't Care

a ····· h : The level of steady state input voltage at inputs A through H respectively

TIMING CHART



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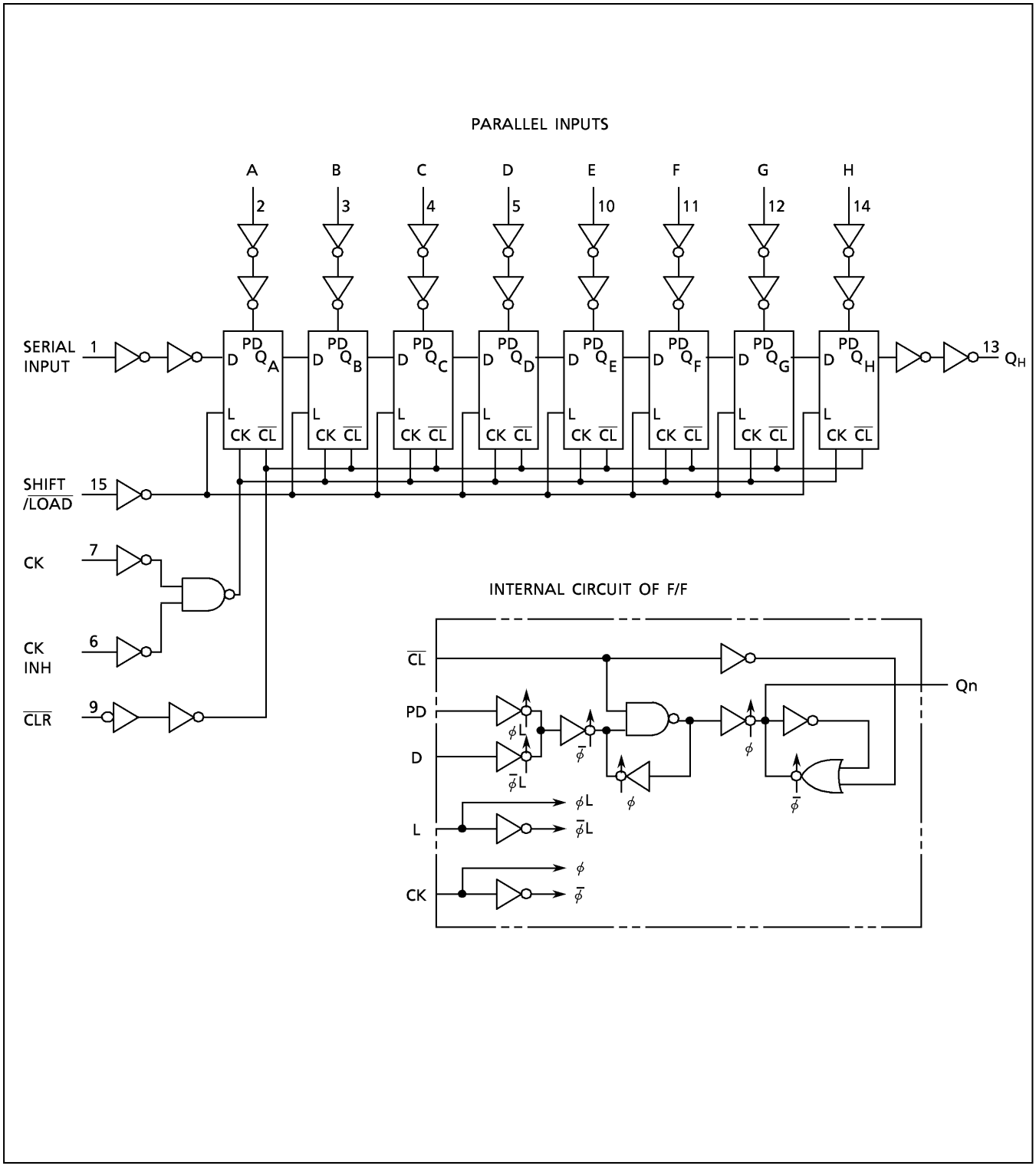
SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 (Vcc = 3.3 ± 0.3V) 0~ 20 (Vcc = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I_{OH} = −4mA I_{OH} = −24mA I_{OH} = −75mA*	3.0 4.5 5.5	2.58 3.94 —	— — —	— — —	2.48 3.80 3.85	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 12mA I_{OL} = 24mA I_{OL} = 75mA*	3.0 4.5 5.5	— — —	— — —	0.36 0.36 —	— — —	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = −40~85°C	UNIT
			V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	8.0 5.0	8.0 5.0	
Minimum Set-up Time (SI, PI)	t_s		3.3 ± 0.3 5.0 ± 0.5	8.0 4.0	8.0 4.0	
Minimum Set-up Time ($S/\overline{L}$)	t_s		3.3 ± 0.3 5.0 ± 0.5	7.0 4.0	7.0 4.0	
Minimum Hold Time (SI, PI)	t_h		3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	
Minimum Hold Time ($S/\overline{L}$)	t_h		3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	4.0 1.5	4.0 1.5	

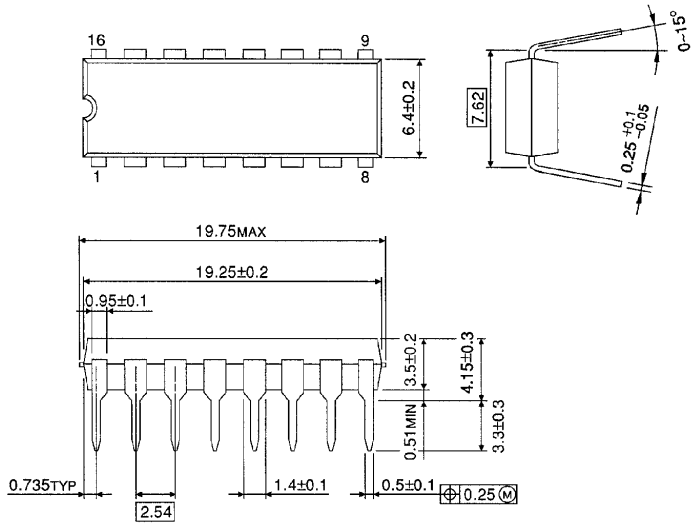
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, $R_L = 500\ \Omega$, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−QH)	t_{pLH} t_{pHL}		3.3 ± 0.3 5.0 ± 0.5	− −	9.4 6.6	16.1 10.0	1.0 1.0	18.3 11.4	ns
Propagation Delay Time ($\overline{CLR}$−QH)	t_{pHL}		3.3 ± 0.3 5.0 ± 0.5	− −	9.2 6.4	15.2 9.6	1.0 1.0	17.4 10.9	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3 5.0 ± 0.5	55 90	105 150	− −	55 90	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	67	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

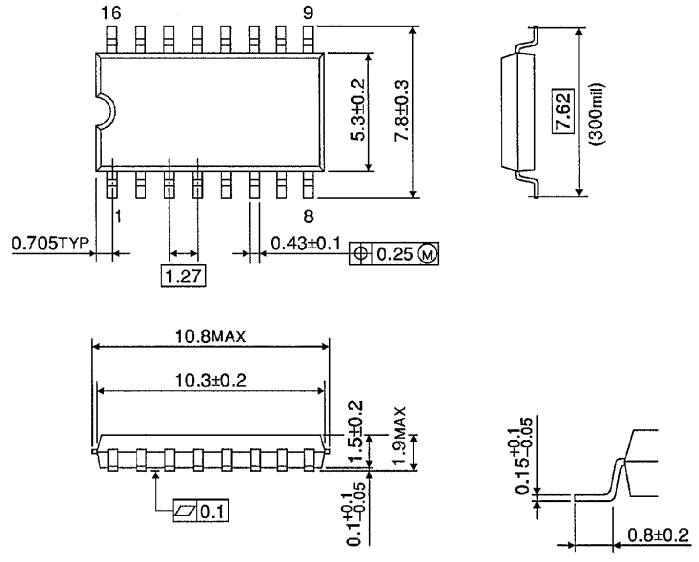
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

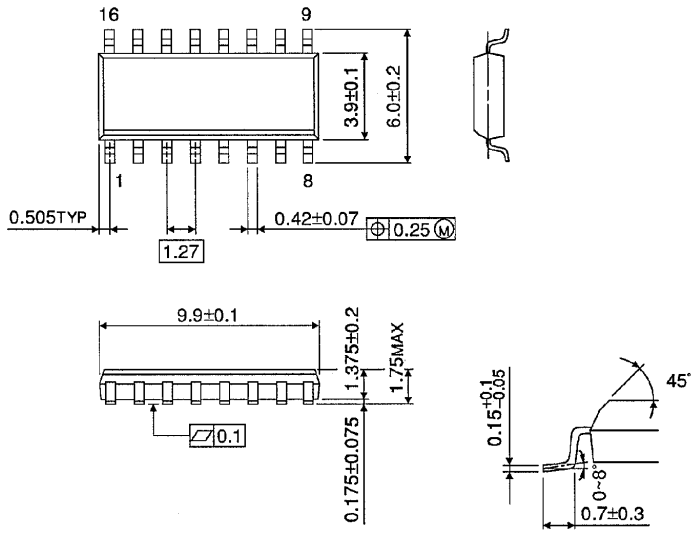
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)