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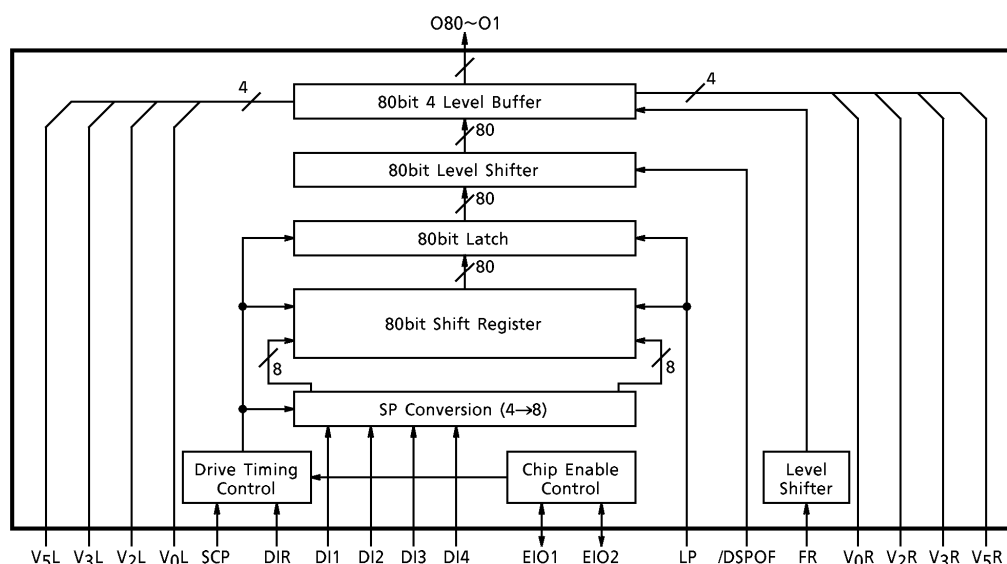
COLUMN DRIVER FOR A DOT MATRIX LCD

The T6B61A is a 80-channel output column driver for a STN dot matrix LCD. The T6B61A feature -30V LCD drive voltage and 10MHz maximum operating frequency. The T6B61A is able to drive LCD panels with a duty ratio up to 1/240. It is recommended to use with the T6B92.

FEATURES

- Display duty application : $\sim 1/240$
- LCD drive signal : 80
- Data transfer : 4bit bidirectional
- Operating frequency : 10MHz ($V_{DD} = 4.5V$)
- LCD drive voltage : $-11 \sim -30V$
- Power supply voltage : 2.7V~5.5V
- Operating temperature : $-20 \sim 65^{\circ}C$
- LCD drive output resistance : 800Ω MAX. (20V, 1/13 bias)
- Display off function : When /DSPOF is "L", All LCD drive outputs (O1~O80) stop on V_0 level
- Low power consumption : Cascade connection and auto enable transfer function are available

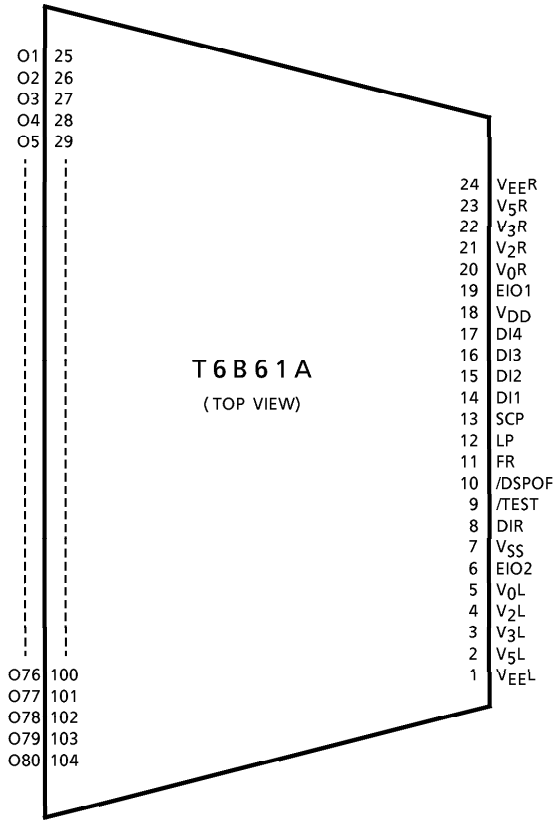
BLOCK DIAGRAM



980910EBE2

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- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.

PIN CONNECTION



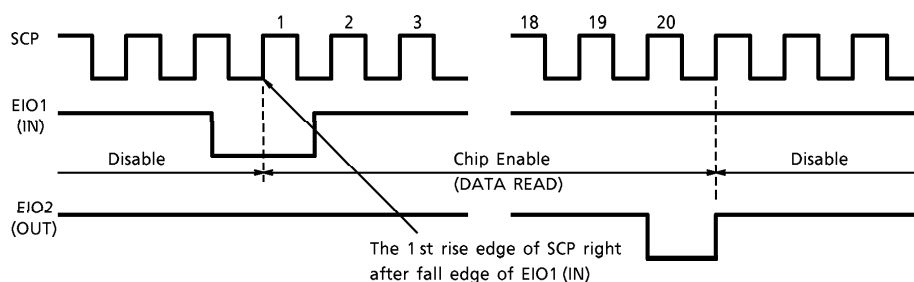
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- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction. This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1~O80	O	Output for LCD drive signal	V_0 ~ V_5
EIO1, EIO2	I/O	Input/Output for enable signal DIR selects input or output. Connect EIO (input) of 1st LSI to Low. For cascade connection of second or more LSIs, externally connect EIO (input) to EIO of next LSI. See example where DIR = H below. Chip enable follows SCP rising edge input after falling edge of EIO1 (input). All 80 bits of data are loaded in 20 SCP clocks. With chip disable, output signals from EIO2 are always High. Signals are Low from SCP rise after 20th SCP clock (during chip enable) to next SCP rise.	V_{DD} ~ V_{SS}
DI1~DI4	I	Input for data signal	
DIR	I	(Direction) Input for data flow direction select	
/DSPOF	I	(Display Off) /DSPOF = H, normal display /DSPOF = L, fixes LCD drive signal output to V_0 level Sets 80-bit data in internal shift register to L. Disables external data input.	
LP	I	(Latch Pulse) Input for latch pulse Display data is latched at the fall edge of LP. When EIO (IN) IS "L", $\overline{SCP} \cdot LP = "H"$ enables the 1st LSI.	
FR	I	(Frame) Input for frame signal	
SCP	I	(Shift Clock Pulse) Input for Shift Clock Pulse	
/TEST	I	(Test) /Test : "H" or OPEN	
V_{DD}	—	Power supply for internal logic (+5V)	—
V_{SS}	—	Ditto (0V)	
V_5 L-R	—	Bias supply for LCD drive circuit	
V_3 L-R	—	Ditto	
V_2 L-R	—	Ditto	
V_0 L-R	—	Ditto	

Fig.1 Ex.) DIR = "H"



FORMAT FOR /DSPOF, FR, DATA INPUT AND OUTPUT LEVEL

FR	DATA INPUT (DI1~DI4)	/DSPOF	OUTPUT LEVEL
L	L	H	V ₂
L	H	H	V ₀
H	L	H	V ₃
H	H	H	V ₅
*	*	L	V ₀

* Don't care

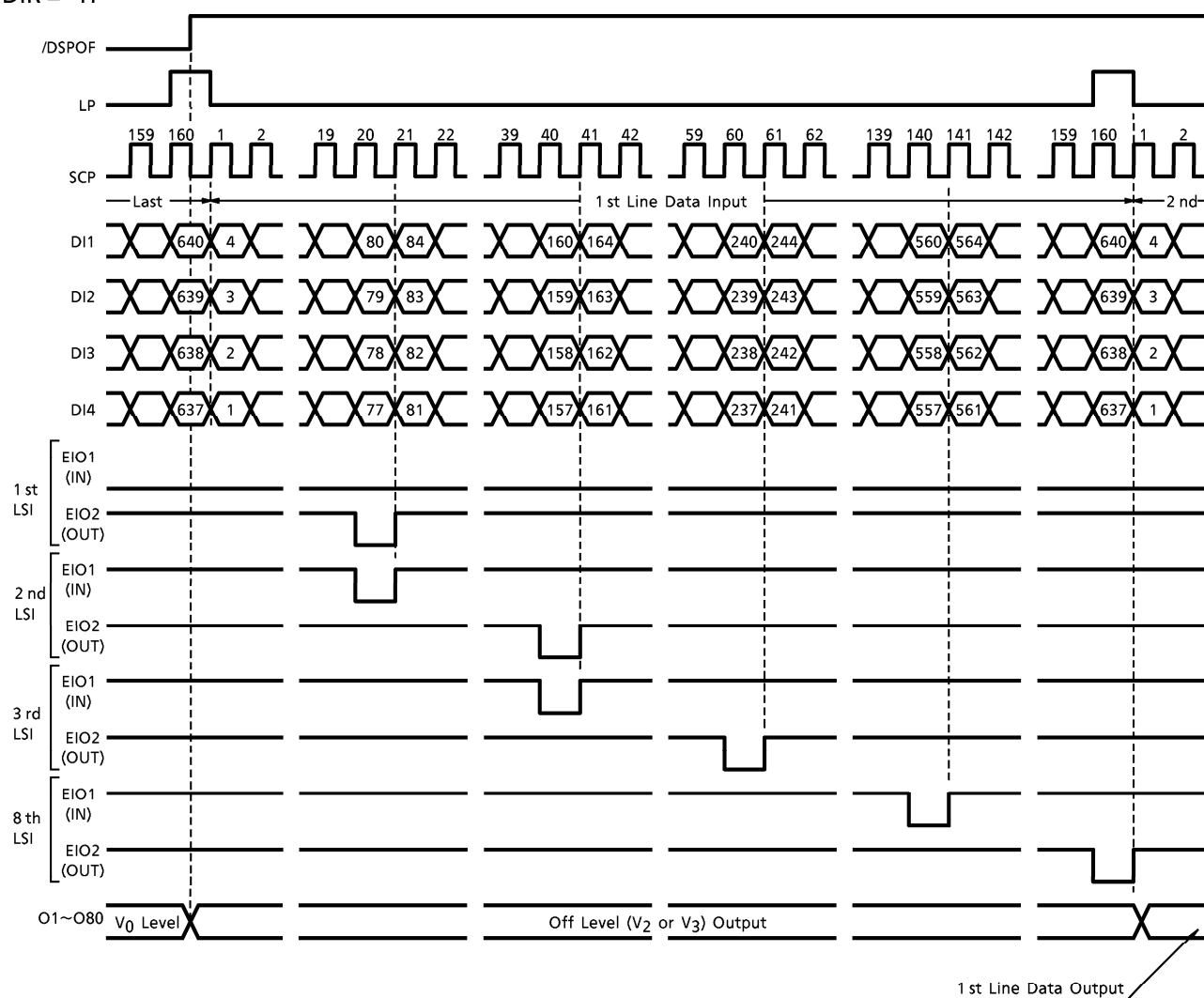
FORMAT FOR DATA INPUT

DIR	ENABLE PIN		(*1)	INPUT DATA LINE AND OUTPUT BUFFERS			
	(EIO1)	(EIO2)		DI1	DI2	DI3	DI4
H	IN	OUT	L	O80	O79	O78	O77
			F	O4	O3	O2	O1
L	OUT	IN	L	O1	O2	O3	O4
			F	O77	O78	O79	O80

 (*1) L : LAST DATA
 F : FIRST DATA

TIMING CHART

DIR = "H"



MAXIMUM RATINGS(Keep the following conditions, $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$, Values measured at $V_{SS} = 0V$)

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	V_{DD}	V_{DD}	$-0.3 \sim 7.0$	V
Supply Voltage 2	V_0	$V_{0L/R}$	$V_{DD} - 32 \sim V_{DD} + 0.3$	V
	V_2	$V_{2L/R}$		
	V_3	$V_{3L/R}$		
	V_5	$V_{5L/R}$		
Input Voltage	V_{in}	(*2)	$-0.3 \sim V_{DD} + 0.3$	V
Operating Temperature	T_{opr}	—	$-20 \sim 65$	°C
Storage Temperature	T_{stg}	—	$-40 \sim 125$	°C

(*2) SCP, FR, LP, DIR, EIO1, EIO2, DI1~DI4, /DSPOF, /TEST

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, $V_{SS} = 0V$, $V_{DD} = 2.7 \sim 5.5V$, $V_0 = V_{DD}$,
 $V_5 = (V_{DD} - 30) \sim (V_{DD} - 11)V$, $T_a = -20 \sim 65^\circ C$)

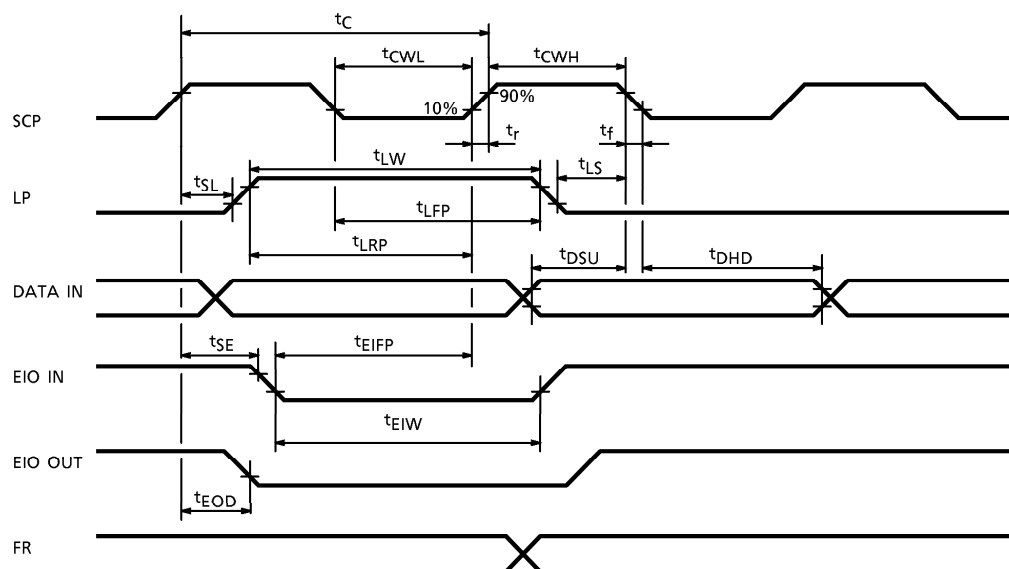
ITEM		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	PIN NAME	
Supply Voltage 1		V _{DD}	—		2.7	5.0	5.5	V	V _{DD}	
Supply Voltage 2		V ₅	—		V _{DD} − 30.0	—	V _{DD} − 11.0	V	V ₅ L / R	
Input Voltage	“H” Level	V _{IH}	—		V _{DD} × 0.8	—	V _{DD}	V	SCP, FR, LP, DIR, EIO1, EIO2, DI1~DI4, /DSPOF, /TEST	
	“L” Level	V _{IL}			0	—	V _{DD} × 0.2			
Output Voltage	“H” Level	V _{OH}	—	I _{OH} = − 0.5mA	V _{DD} − 0.5	—	—	V	EIO1~EIO2	
	“L” Level	V _{OL}		I _{OL} = 0.5mA	—	—	0.5			
Output Resistance	“H” Level	R _{OH}	—	V _{OUT} = V ₀ − 0.5V (*3)	—	—	800	Ω	O1~O80	
	“M” Level	R _{OM}		V _{OUT} = V ₂ ± 0.5V (*3)	—	—	800			
		R _{OM}		V _{OUT} = V ₃ ± 0.5V (*3)	—	—	800			
	“L” Level	R _{OL}		V _{OUT} = V ₅ + 0.5V (*3)	—	—	800			
Current Consumption (*4)		I _{SS}	—	V _{DD} = 5.5V V ₅ = − 24.5V f _{FR} = 80Hz f _{SCP} = 6.15MHz O1~O80 : No Load	Input Data: Bit Binary	—	—	− 2.0	mA	V _{SS}
Current Consumption (*5)		I _{SS}	—	As mentioned above	Input Data: Bit Binary	—	—	− 800	μA	V _{SS}

(*3) $V_{DD} = 5.0V$, $V_5 = -15V$, $V_2 = V_{DD} - 2/13(V_{DD} - V_5)$, $V_3 = V_{DD} - 11/13(V_{DD} - V_5)$

(*4) Current consumption during the internal data receiver operating.

(*5) Current consumption during the internal data receiver sleeping.

AC CHARACTERISTICS



TSET CONDITIONS 1 ($V_{SS} = 0V$, $V_{DD} = 5V \pm 10\%$, $V_0 = V_{DD}$, $V_5 = (V_{DD} - 30) \sim (V_{DD} - 11)V$, $T_a = -20 \sim 65^\circ C$)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Clock Cycle	t_C	—	100	—	ns
SCP Pulse Width	t_{CWL}, t_{CWH}	—	40	—	ns
Data Set Up Time	t_{DSU}	—	20	—	ns
Data Hold Time	t_{DHD}	—	15	—	ns
SCP Rise / Fall Time	t_r, t_f	—	—	(*6)	ns
LP Rise Time	t_{LRP}	—	40	—	ns
LP Fall Time	t_{LFP}	—	15	—	ns
LP Pulse Width	t_{LW}	—	40	—	ns
SCP to LP Delay Time	t_{SL}	—	0	—	ns
LP to SCP Delay Time	t_{LS}	—	20	—	ns
EIO IN Fall Time	t_{EIFP}	—	40	—	ns
EIO IN Pulse Width	t_{EIW}	—	40	—	ns
SCP to EIO Delay Time	t_{SE}	—	10	—	ns
EIO OUT Delay Time	t_{EOD}	(*7)	—	60	ns

(*6) $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and $t_r, t_f \leq 50ns$

(*7) $C_L = 10pF$

TEST CONDITIONS 2 ($V_{SS}=0V$, $V_{DD}=2.7\sim5.5V$, $V_0=V_{DD}$, $V_5=(V_{DD}-30)\sim(V_{DD}-11)V$, $T_a=-20\sim65^\circ C$)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Clock Cycle	t_C	—	200	—	ns
SCP Pulse Width	t_{CWH}, t_{CWL}	—	60	—	ns
Data Set Up Time	t_{DSU}	—	45	—	ns
Data Hold Time	t_{DHD}	—	15	—	ns
SCP Rise / Fall Time	t_r, t_f	—	—	(*8)	ns
LP Rise Time	t_{LRP}	—	60	—	ns
LP Fall Time	t_{LFP}	—	15	—	ns
LP Pulse Width	t_{LW}	—	60	—	ns
SCP to LP Delay Time	t_{SL}	—	0	—	ns
LP to SCP Delay Time	t_{LS}	—	30	—	ns
EIO IN Fall Time	t_{EIFP}	—	60	—	ns
EIO IN Pulse Width	t_{EIW}	—	60	—	ns
SCP to EIO Delay Time	t_{SE}	—	10	—	ns
EIO OUT Delay Time	t_{EOD}	(*9)	—	140	ns

(*8) $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and $t_r, t_f \leq 50ns$

(*9) $C_L = 10pF$

TEST CONDITIONS 3 ($V_{SS}=0V$, $V_{DD}=3.0\sim5.5V$, $V_0=V_{DD}$, $V_5=(V_{DD}-30)\sim(V_{DD}-11)V$, $T_a=-20\sim65^\circ C$)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Clock Cycle	t_C	—	153	—	ns
SCP Pulse Width	t_{CWH}, t_{CWL}	—	50	—	ns
Data Set Up Time	t_{DSU}	—	35	—	ns
Data Hold Time	t_{DHD}	—	15	—	ns
SCP Rise / Fall Time	t_r, t_f	—	—	(*10)	ns
LP Rise Time	t_{LRP}	—	50	—	ns
LP Fall Time	t_{LFP}	—	15	—	ns
LP Pulse Width	t_{LW}	—	50	—	ns
SCP to LP Delay Time	t_{SL}	—	0	—	ns
LP to SCP Delay Time	t_{LS}	—	25	—	ns
EIO IN Fall Time	t_{EIFP}	—	50	—	ns
EIO IN Pulse Width	t_{EIW}	—	50	—	ns
SCP to EIO Delay Time	t_{SE}	—	10	—	ns
EIO OUT Delay Time	t_{EOD}	(*11)	—	100	ns

(*10) $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and $t_r, t_f \leq 50ns$

(*11) $C_L = 10pF$