

# T 6 C 6 1

## COLUMN DRIVER FOR A DOT MATRIX LCD

The T6C61 is a 160-channel-output column driver for an STN dot matrix LCD. The T6C61 features a 42-V LCD drive voltage and a 25-MHz maximum operating frequency. The T6C61 is able to drive LCD panels with a duty ratio of up to 1/480. It is recommended for use with the T6C14.

Unit: mm

T6C61	LEAD PITCH	
	IN	OUT
(UAN, 3NS)	0.48	0.08

Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

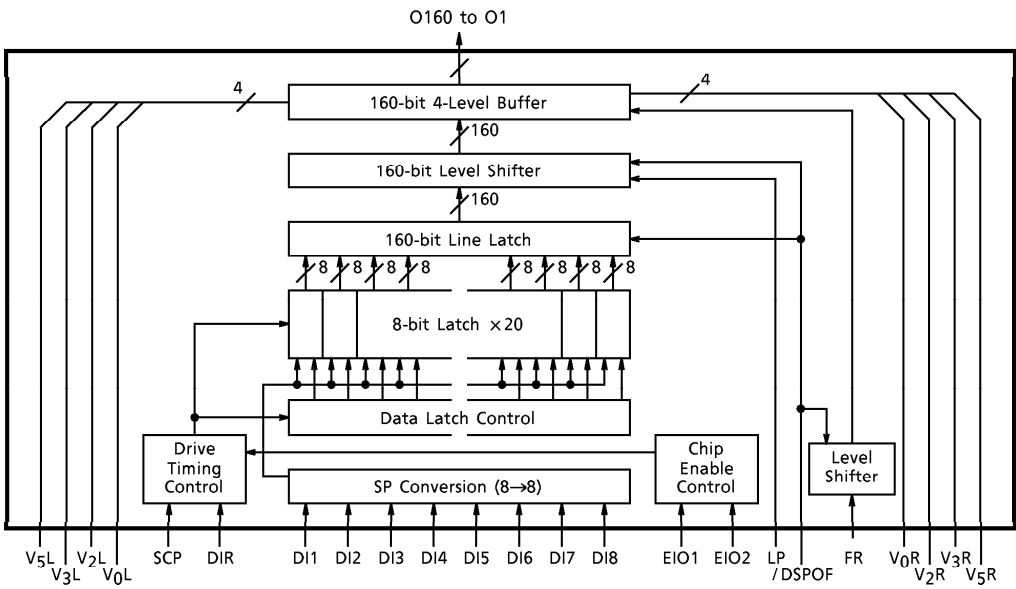
### FEATURES

- Display duty application : to 1/480
- LCD drive signal : 160
- Data transfer : 8-bit bidirectional
- Operating frequency : 25MHz ( $V_{DD} = 4.5V$ )  
13MHz ( $V_{DD} = 2.7V$ )
- LCD drive voltage : 14 to 42V (max 45V)
- Power supply voltage : 2.7 to 5.5V
- Operating temperature : -20 to 75°C
- LCD drive output resistance : 700 $\Omega$  (typ.), 1200 $\Omega$  (max) (20V, 1/13 bias)
- Display-off function : When /DSPOF is L, all LCD drive outputs (O1 to O160) remain at the  $V_5$  level.
- Low power consumption : Cascade connection and auto enable transfer functions are available.

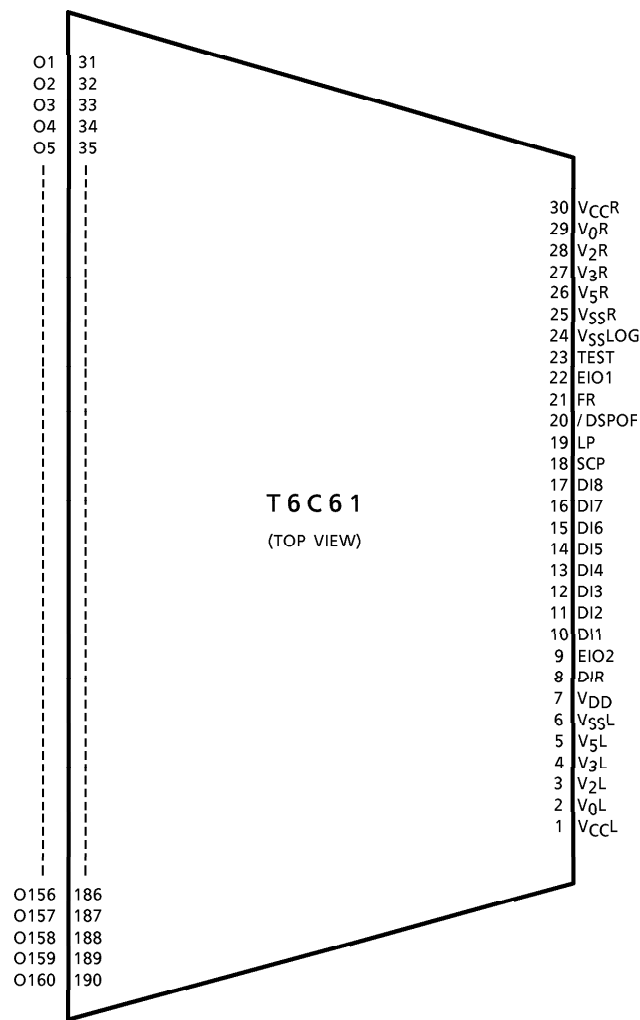
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- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction. This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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BLOCK DIAGRAM



PIN ASSIGNMENT



The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package.

## PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1 to O160	Output	Output for LCD drive signal	$V_0$ to $V_5$
EIO1, EIO2	I/O	Input/output for enable signal DIR selects In or Out. Connect EIO (IN) of 1st LSI to L For a cascade connection, connect EIO (OUT) to EIO (IN) of next LSI.	$V_{DD}$ to $V_{SS}$
DI1 to DI8	Input	Input for data signal	
DIR	Input	(Direction) Input for data flow direction select	
/DSPOF	Input	(Display Off) /DSPOF = L : Display-off mode, (O1 to O160) remain at the $V_5$ level. /DSPOF = H : Function mode, (O1 to O160) are operational.	
LP	Input	(Latch Pulse) Input for latch pulse Display data is latched on the falling edge of LP. When EIO (IN) = L, setting $SCP \cdot LP = H$ enables the 1st LSI.	
FR	Input	(Frame) Input for frame signal	
SCP	Input	(Shift Clock Pulse) Input for shift clock pulse	
TEST	Input	(Test) Test : L or open	—
$V_{DD}$	—	Power supply for internal logic (5V)	
$V_{SSLOG}$	—	Power supply for internal logic (0V)	
$V_{SSL \cdot R}$	—	Power supply for LCD drive circuit	
$V_5L \cdot R$	—	Power supply for LCD drive circuit	
$V_3L \cdot R$	—	Power supply for LCD drive circuit	
$V_2L \cdot R$	—	Power supply for LCD drive circuit	
$V_0L \cdot R$	—	Power supply for LCD drive circuit	
$V_{CCL \cdot R}$	—	Power supply for LCD drive circuit	

RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

FR	DATA INPUT (DI1~DI8)	/DSPOF	OUTPUT LEVEL
H	L	H	V <sub>2</sub>
H	H	H	V <sub>0</sub>
L	L	H	V <sub>3</sub>
L	H	H	V <sub>5</sub>
*	*	L	V <sub>5</sub>

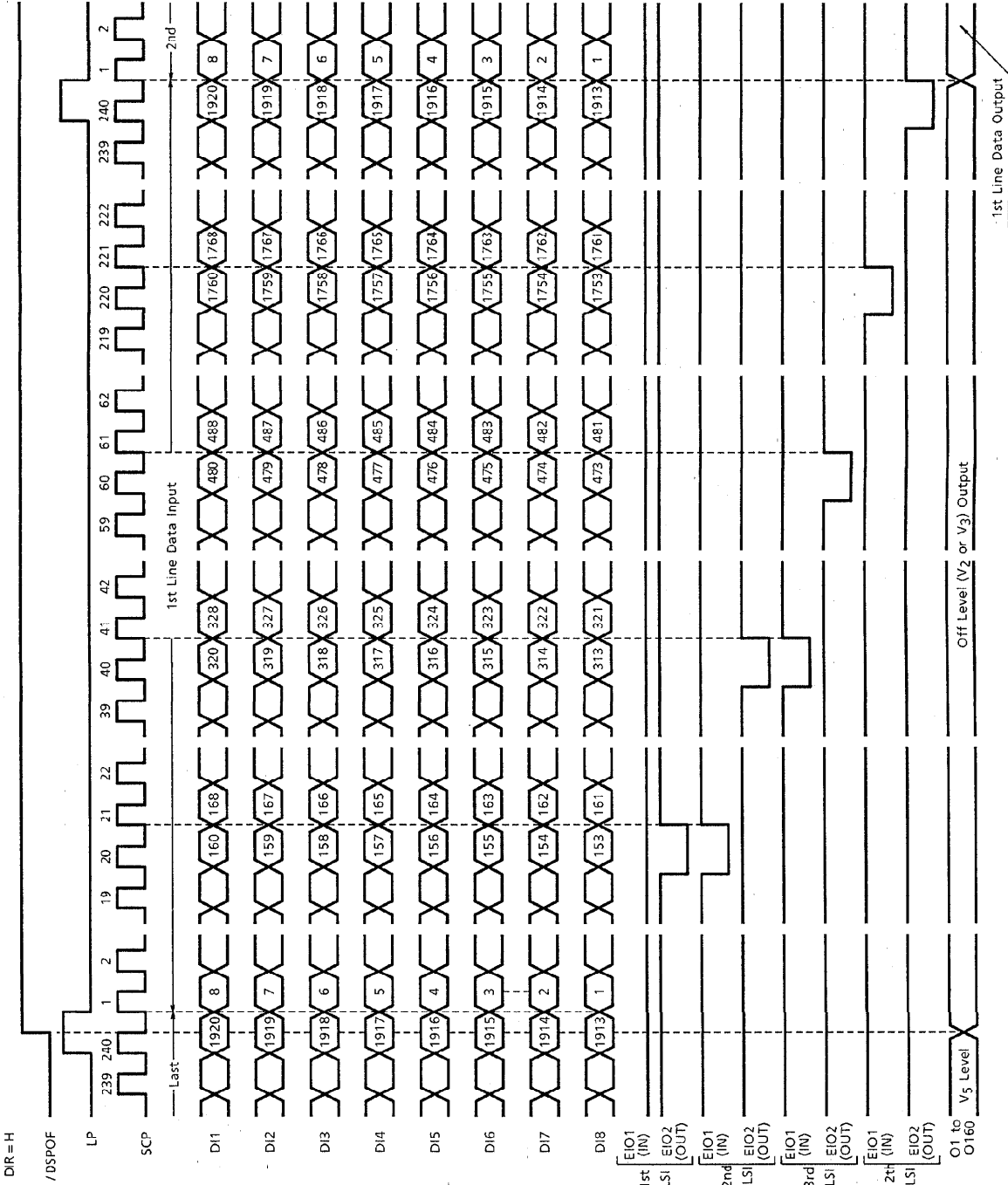
\* Don't Care

DATA INPUT FORMAT

DIR	ENABLE PIN		(*1)	INPUT DATA LINE AND OUTPUT BUFFERS							
	EIO1	EIO2		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	IN	OUT	L	O160	O159	O158	O157	O156	O155	O154	O153
			F	O8	O7	O6	O5	O4	O3	O2	O1
L	OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
			F	O153	O154	O155	O156	O157	O158	O159	O160

(\*1) L : LAST DATA F : FIRST DATA

TIMING DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS**(Ensure that the following conditions are maintained,  $V_{CC} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{SS}$ )

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	$V_{DD}$	$V_{DD}$	- 0.3 to 6.5	V
Supply Voltage 2	$V_{CC}$	$V_{CCL/R}$	- 0.3 to 45.0	V
Supply Voltage 3	$V_0, V_2$	$V_{0L/R}, V_{2L/R}$	- 0.3 to $V_{CC} + 0.3$	V
Supply Voltage 4	$V_3, V_5$	$V_{3L/R}, V_{5L/R}$	- 0.3 to $V_{CC} + 0.3$	V
Input Voltage	$V_{IN}$	(*2)	- 0.3 to $V_{DD} + 0.3$	V
Operating Temperature	$T_{opr}$	—	- 20 to 75	°C
Storage Temperature	$T_{stg}$	—	- 40 to 125	°C

(\*2) SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, /DSPOF, TEST

## ELECTRICAL CHARACTERISTICS

## DC CHARACTERISTICS

(Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 2.7$  to  $5.5V$ ,  $V_{CC} = 14$  to  $42V$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM		SYMBOL	TEST CIR- CUIT	TEST CONDITIONS			MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1		V <sub>DD</sub>	—	—			2.7	5.0	5.5	V	V <sub>DD</sub>
Supply Voltage 2		V <sub>CC</sub>	—	—			14	—	42		V <sub>CC</sub> L/R
Input Voltage	H Level	V <sub>IH</sub>	—	—			0.8 V <sub>DD</sub>	—	V <sub>DD</sub>		SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, /DSPOF, TEST
	L Level	V <sub>IL</sub>		—			0	—	0.2 V <sub>DD</sub>		
Output Voltage	H Level	V <sub>OH</sub>	—	I <sub>OH</sub> = -0.5mA			V <sub>DD</sub> - 0.5	—	V <sub>DD</sub>	EIO1, EIO2	
	L Level	V <sub>OL</sub>		I <sub>OL</sub> = 0.5mA			0	—	0.5		
Output Resistance	H Level	R <sub>OH</sub>	—	V <sub>OUT</sub> = V <sub>0</sub> - 0.5V (*3)			—	700	1200	Ω	O1 to O160
	M Level	R <sub>OM</sub>		V <sub>OUT</sub> = V <sub>2</sub> ± 0.5V (*3)			—	700	1200		
				V <sub>OUT</sub> = V <sub>3</sub> ± 0.5V (*3)			—	700	1200		
	L Level	R <sub>OL</sub>		V <sub>OUT</sub> = V <sub>5</sub> + 0.5V (*3)			—	700	1200		
Input Current		I <sub>IL</sub>	—	V <sub>DD</sub>	V <sub>CC</sub>	CONDITION	- 10	—	10	μA	V <sub>0</sub> L/R V <sub>2</sub> L/R V <sub>3</sub> L/R V <sub>5</sub> L/R
				5.0	42	Standby					
Current Consumption		I <sub>DD</sub> Ope	—	5.0	20	Function (*4)	—	—	5.0	mA	V <sub>DD</sub>
				2.7	20		—	—	2.5		
		I <sub>DD</sub> St/by		5.0	20	Function (*5)	—	—	2.0		
				2.7	20		—	—	1.0		
		I <sub>CC</sub> Leak			5.0	42	Standby	- 10	—	10	μA

(\*3)  $V_{CC} = 20V$ , 1/13 bias(\*4)  $f_{SCP} = 13MHz$ ,  $f_{LP} = 54kHz$ ,  $f_{FR} = 13.5kHz$ ,  $f_{EIO} = 650kHz$ 

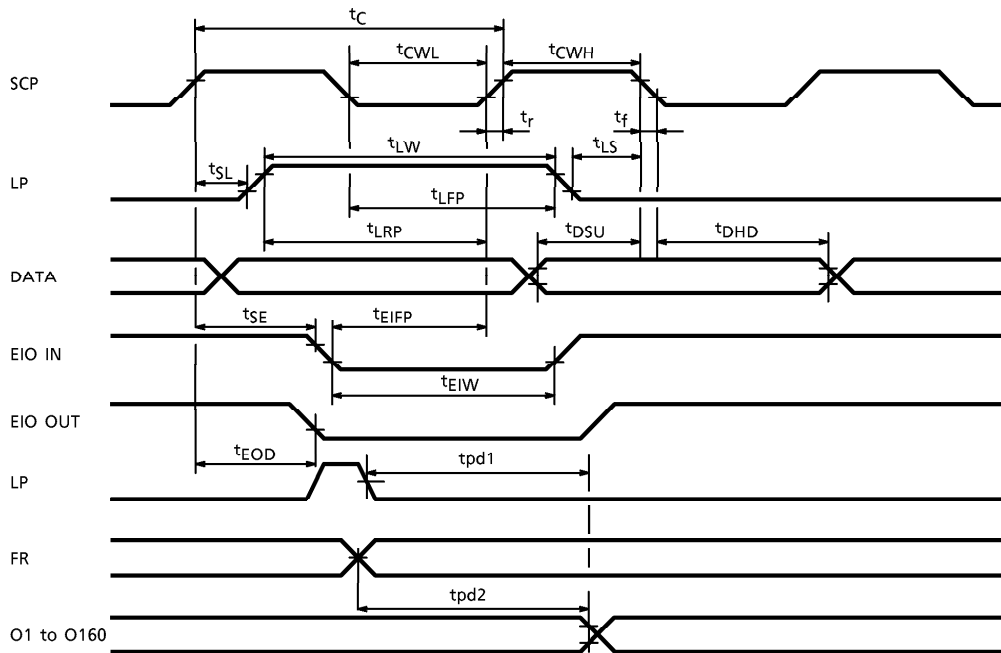
Data Format : every bit inverted, while internal data receiver is operating

(\*5)  $f_{SCP} = 13MHz$ ,  $f_{LP} = 54kHz$ ,  $f_{FR} = 13.5kHz$ 

Data Format : every bit inverted, while internal data receiver is sleeping



## AC CHARACTERISTICS



TEST CONDITIONS (1) ( $V_{SS} = 0V$ ,  $V_{DD} = 4.5$  to  $5.5V$ ,  $V_{CC} = 14$  to  $42V$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	$t_C$	—	40	—	—	ns
SCP Pulse Width	$t_{CWH}$	—	15	—	—	
	$t_{CWL}$	—	15	—	—	
Data Set-Up Time	$t_{DSU}$	—	10	—	—	
Data Hold Time	$t_{DHD}$	—	10	—	—	
SCP Rise / Fall Time	$t_r, t_f$	—	—	—	(*6)	
LP Rise Time	$t_{LRP}$	—	15	—	—	
LP Fall Time	$t_{LFP}$	—	10	—	—	
LP Pulse Width	$t_{LW}$	—	10	—	—	
SCP-to-LP Delay Time	$t_{SL}$	—	5	—	—	
LP-to-SCP Delay Time	$t_{LS}$	—	10	—	—	
EIO-IN Rise Time	$t_{EIPF}$	—	20	—	—	
EIO-IN Pulse Width	$t_{EIW}$	—	10	—	—	
SCP-to-EIO Delay Time	$t_{SE}$	—	5	—	—	
EIO-OUT Delay Time	$t_{EOD}$	(*7)	—	—	20	
Output Delay Time 1 (LP→OUT)	$t_{pd1}$	—	—	—	400	
Output Delay Time 2 (FR→OUT)	$t_{pd2}$	—	—	—	400	
Output Delay Time Variation	(*8)	—	—	0	30	

(\*6)  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r, t_f \leq 50ns$

(\*7)  $C_L = 10pF$

(\*8) Variation in  $t_{pd1}$  and  $t_{pd2}$

TEST CONDITIONS (2) ( $V_{SS}=0V$ ,  $V_{DD}=2.7$  to  $4.5V$ ,  $V_{CC}=14$  to  $42V$ ,  $T_a=-20$  to  $75^{\circ}C$ )

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	$t_C$	—	76	—	—	ns
SCP Pulse Width	$t_{CWH}$	—	30	—	—	
	$t_{CWL}$	—	30	—	—	
Data Set-up Time	$t_{DSU}$	—	28	—	—	
Data Hold Time	$t_{DHD}$	—	28	—	—	
SCP Rise/Fall Time	$t_r, t_f$	—	—	—	(*9)	
LP Rise Time	$t_{LRP}$	—	28	—	—	
LP Fall Time	$t_{LFP}$	—	28	—	—	
LP Pulse Width	$t_{LW}$	—	28	—	—	
SCP-to-LP Delay Time	$t_{SL}$	—	5	—	—	
LP-to-SCP Delay Time	$t_{LS}$	—	10	—	—	
EIO-IN Rise Time	$t_{EIFP}$	—	40	—	—	
EIO-IN Pulse Width	$t_{EIW}$	—	28	—	—	
SCP-to-EIO Delay Time	$t_{SE}$	—	5	—	—	
EIO-OUT Delay Time	$t_{EOD}$	(*10)	—	—	35	
Output Delay Time 1 (LP→OUT)	$t_{pd1}$	—	—	—	500	
Output Delay Time 2 (FR→OUT)	$t_{pd2}$	—	—	—	500	
Output Delay Time Variation	(*11)	—	—	0	50	

(\*9)  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r, t_f \leq 50ns$

(\*10)  $C_L = 10pF$

(\*11) Variation in  $t_{pd1}$  and  $t_{pd2}$

#### NOTE

Insert the bypass capacitor ( $0.1\mu F$ ) between  $V_{DD}$  and  $V_{SS}$ , and between  $V_{CC}$  and  $V_{SS}$  to decrease power supply noise.

Place the bypass capacitor as close to the LSI as possible.