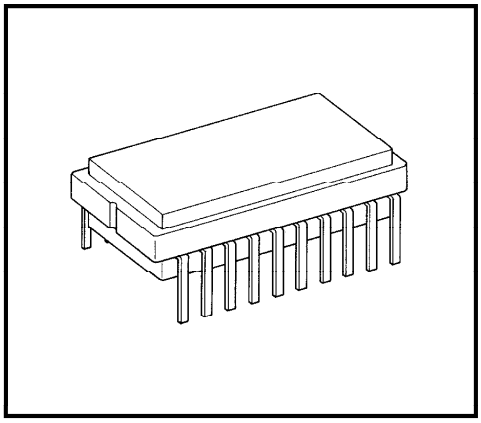
TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD2000P

The TCD2000P is a high sensitive and low dark current 480-elements color linear image sensor which includes CCD drive circuit, clamp circuit and sample & hold circuit. The CCD drive circuit consists of the pulse generator. therefore it is possible to easy drive by applying simple pulses. The sensor is designed for scanner.



Weight : 1.0g (Typ.)

FEATURES

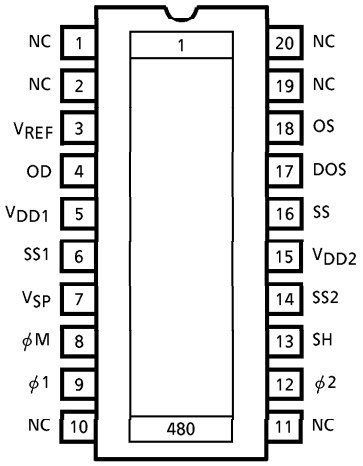
- Number of Image Sensing Elements
  : 480 elements (160 × 3 color sequential)
- Image Sensing Element Size : 11μm × 33μm on 33μm centers
- Photo Sensing Region : High sensitive pn photodiode
- Clock : 3 Input pulses 5V
- Internal Circuit : Sample & Hold circuit, Clamp circuit
- Package : 20 pin
- Color Filter : Red, Green, Blue

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Master Clock Voltage	$V_{\phi M}$	−0.3~8	V
Clock Pulse Voltage	V_{ϕ}		
Shift Pulse Voltage	V_{SH}		
Reference Voltage	V_{REF}	−0.3~15	V
Power Supply Voltage (Analog)	V_{AD}		
Power Supply Voltage (Digital)	V_{DD1}		
	V_{DD2}		
Sample & Hold Switch Voltage	V_{SP}	−0.3~8	V
Operating Temperature	T_{opr}	0~60	°C
Storage Temperature	T_{stg}	−25~85	°C

(Note 1) All voltage are with respect to SS terminals (Ground).

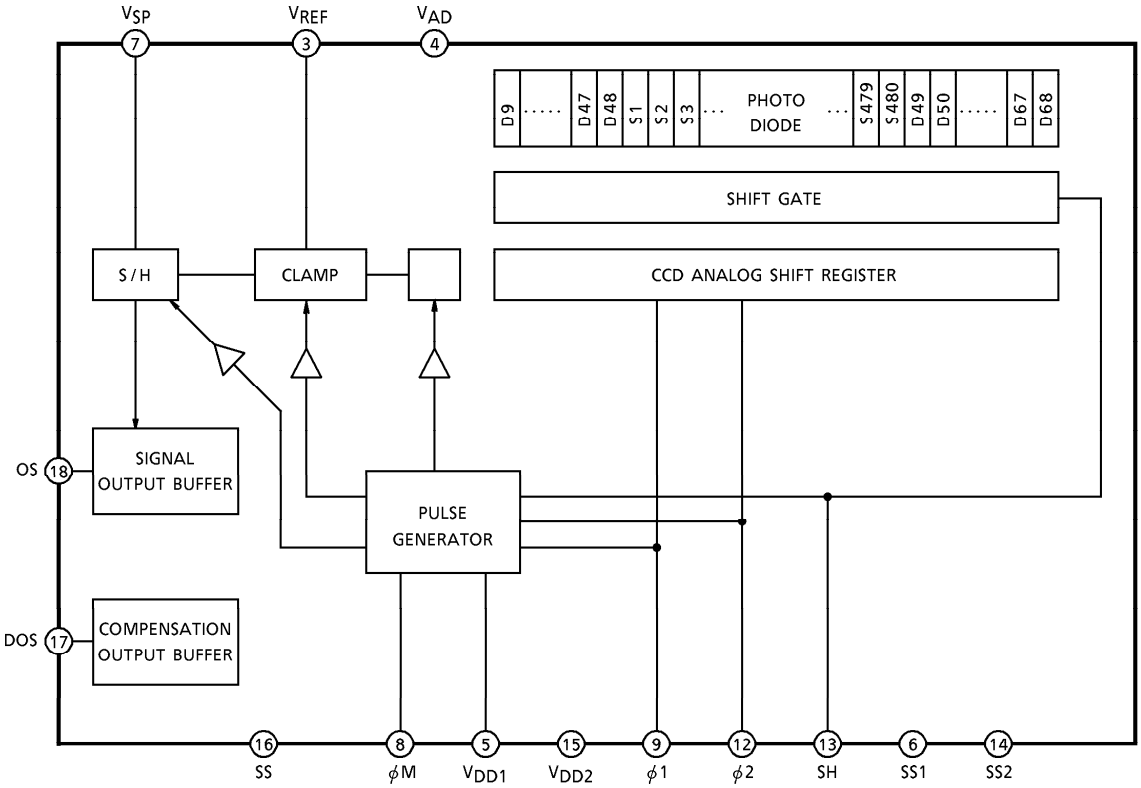
PIN CONNECTIONS



(TOP VIEW)

961001EBA2

CIRCUIT DIAGRAM



PIN NAMES

ϕM	Master Clock	V_{AD}	Power (Analog)
ϕ1	Clock (Phase 1)	V_{DD1}	Power (Digital, 12V)
ϕ2	Clock (Phase 2)	V_{DD2}	Power (Digital, 12V)
SH	Shift Gate	SS	Ground (Analog)
OS	Signal Output	SS1	Ground (Digital, 12V)
DOS	Compensation Output	SS2	Ground (Digital, 12V)
V_{REF}	Reference Voltage Input	V_{SP}	Sample and Hold Switch
NC	Non Connection		

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, $V_{REF} = V_{AD} = V_{DD1} = V_{DD2} = 12V$, $V_{\phi M} = V_{\phi} = V_{SH} = 5V$ (PULSE), $f_{\phi} = 1.0MHz$, t_{INT} (INTEGRATION TIME) = 10ms, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER, LOAD RESISTANCE = 100Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	RB	3.7	5.3	6.9	V / lx·s	
	RG	8.4	12.0	15.6		
	RR	4.6	6.6	8.7		
Photo Response Non Uniformity	PRNU (1)	—	10	20	%	(Note 2)
	PRNU (3)	—	3	12	mV	(Note 3)
Saturation Output Voltage	V_{SAT}	1.2	2.0	—	V	(Note 4)
Saturation Exposure	SE	—	0.17	—	lx·s	(Note 5)
Dark Signal Voltage	V_{DRK}	—	12	25	mV	(Note 6)
Dark Signal Non Uniformity	DSNU	—	5	10	mV	(Note 6)
Analog Current Dissipation	I_{AD}	—	12	18	mA	
Digital Current Dissipation	I_{DD1}	—	—	1	mA	
	I_{DD2}	—	13.5	20	mA	
Input Current of V_{REF}	I_{REF}	—	—	1	mA	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	Z_O	—	0.5	1.0	kΩ	
DC Signal Output Voltage	V_{OS}	4.5	6.0	7.5	V	(Note 7)
DC Compensation Output Voltage	V_{DOS}	4.5	6.0	7.5	V	(Note 7)
DC Differential Error Voltage	$\lvert V_{OS}-V_{DOS} \rvert$	0	—	100	mV	

(Note 2) PRNU (1) is measured at 50% of SE (Typ.)

Definition of PRNU : $PRNU = \frac{\Delta\chi}{\overline{\chi}} \times 100\,(\%)$

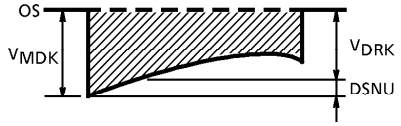
Where $\overline{\chi}$ is average of total signal outputs and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$ under uniform illumination.

(Note 3) PRNU (3) is defined as maximum voltage with next pixel where measured 5% of SE (Typ.)

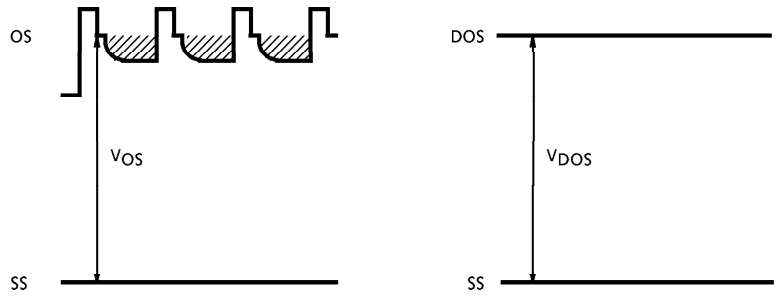
(Note 4) V_{SAT} is defined as minimum Saturation Output Voltage of all effective pixels.

(Note 5) Definition of SE : $SE = \frac{V_{SAT}}{R}$ (lx·s)

(Note 6) V_{DRK} is defined as average dark signal voltage of all effective pixels.
DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



(Note 7) DC signal output voltage and DC compensation output voltage are defined as follows:



OPERATING CONDITION

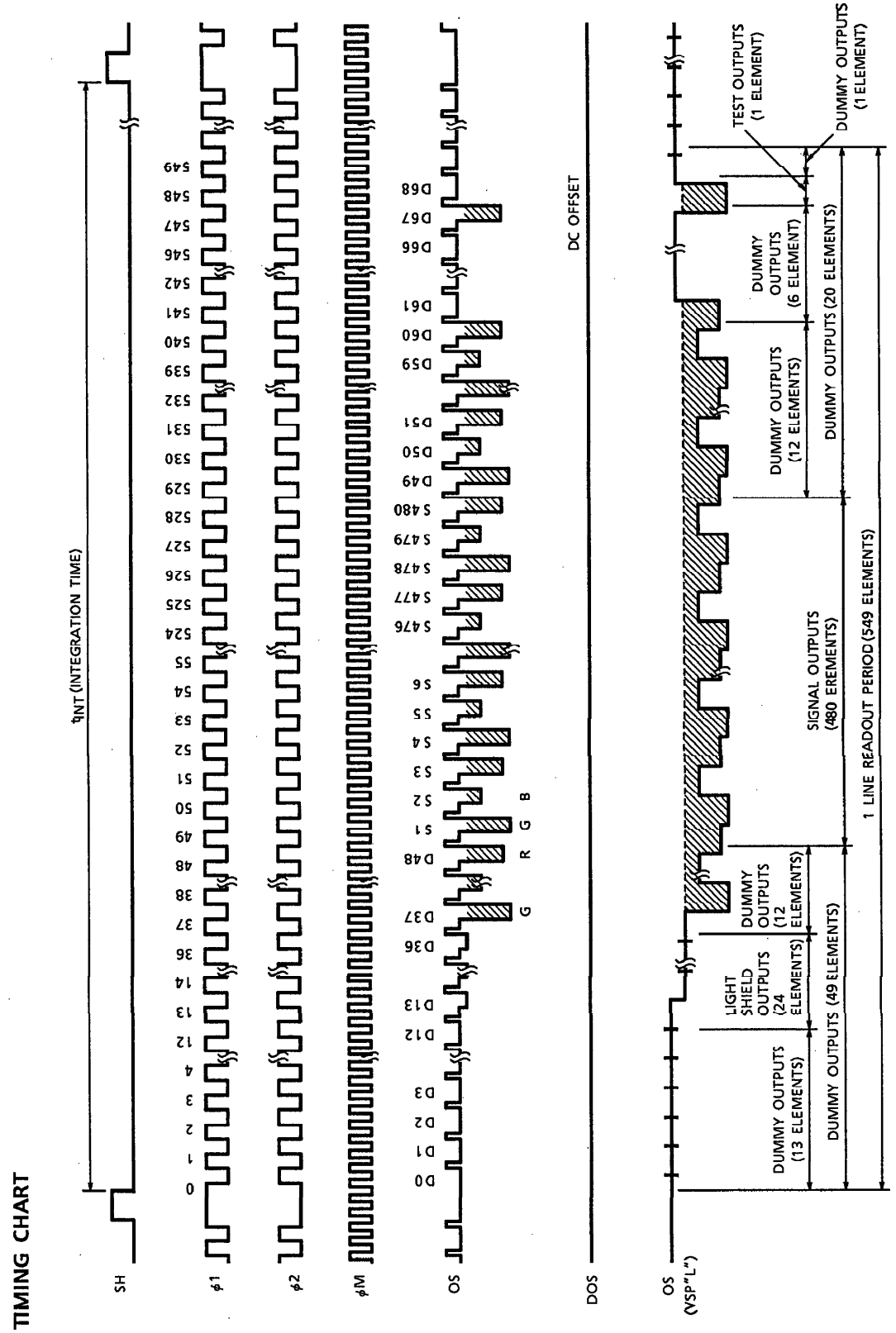
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Master Clock Pulse Voltage	"H" Level	$V_{\phi M}$	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Clock Pulse Voltage	"H" Level	$V_{\phi 1}$ $V_{\phi 2}$	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Shift Pulse Voltage	"H" Level	V_{SH}	$V_{\phi} - 0.5$	V_{ϕ}	V_{ϕ}	V
	"L" Level		0	—	0.5	
Sample and Hold Switch Voltage*	"H" Level	V_{SP}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Reference Voltage		V_{REF}	11.4	12.0	13.0	V
Power Supply Voltage (Analog)		V_{AD}	11.4	12.0	13.0	V
Power Supply Voltage (Digital)		V_{DD1}	11.4	12.0	13.0	V
		V_{DD2}	11.4	12.0	13.0	

(*) Supply "H" Level to V_{SP} terminal when sample-and-hold circuit is used, when sample-and-hold circuit is not used supply "L" Level to V_{SP} terminal.

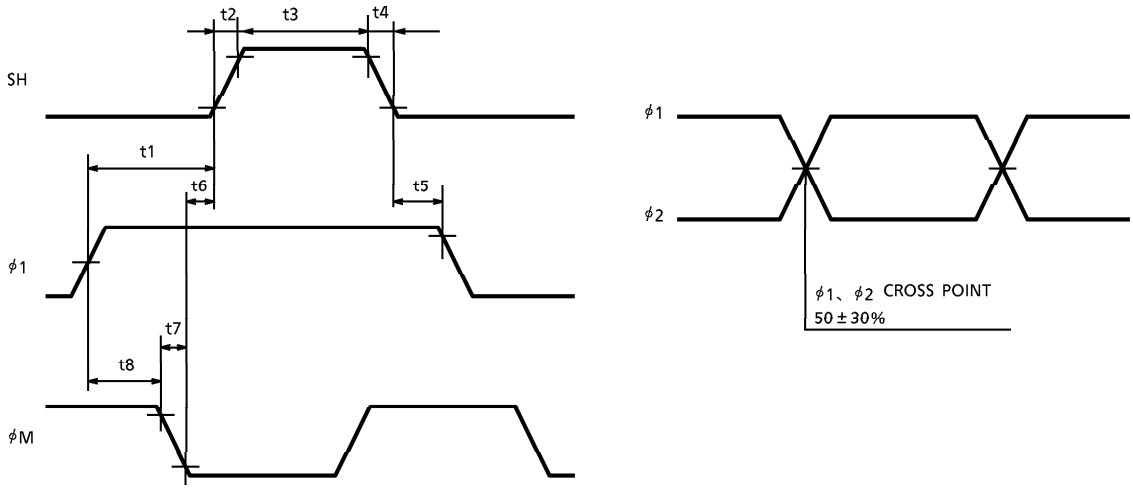
CLOCK CHARACTERISTICS (Ta = 25°C)

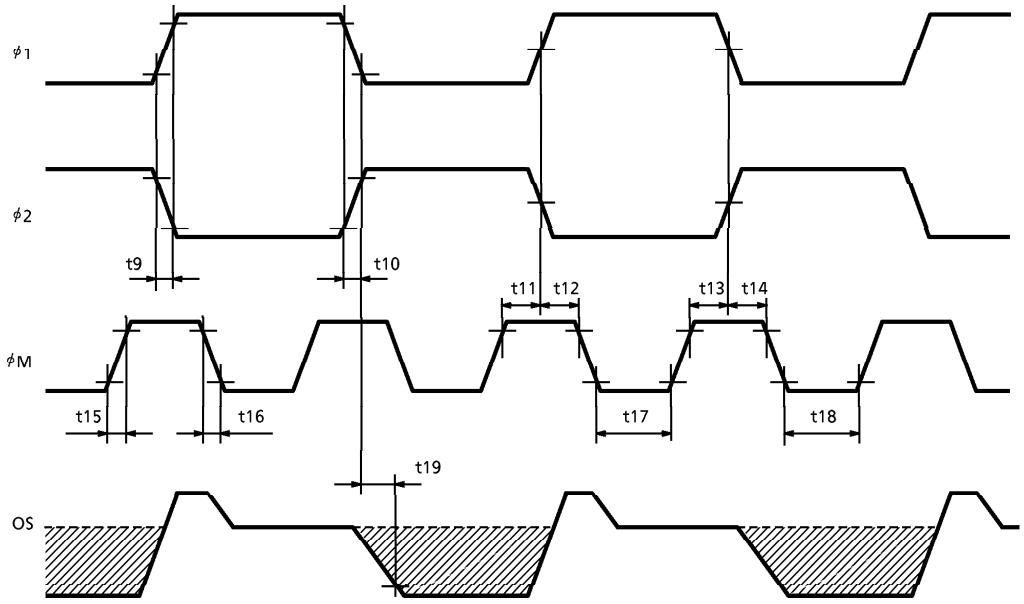
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Master Clock Pulse Frequency	$f_{\phi M}$	—	2.0	6.0	MHz
Clock Pulse Frequency	f_{ϕ}	—	1.0	3.0	MHz
Master Clock Pulse Capacitance	$C_{\phi M}$	—	10	20	pF
Clock Capacitance	C_{ϕ}	—	100	200	pF
Shift Gate Capacitance	C_{SH}	—	50	100	pF

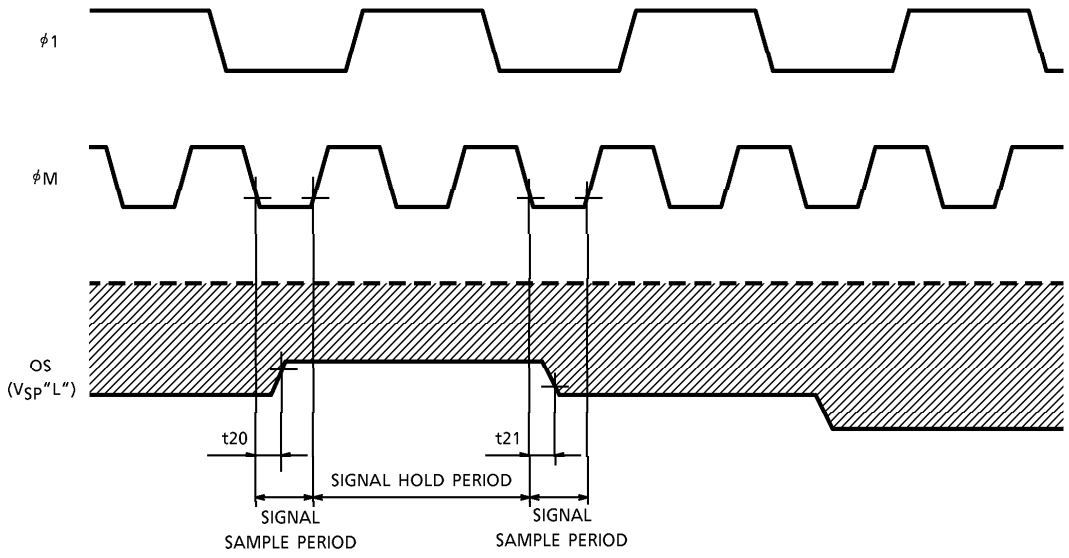
TIMING CHART



TIMING REQUIREMENS





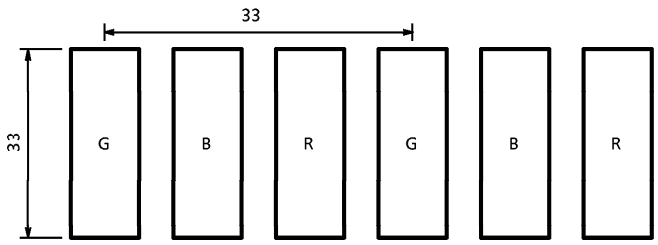


CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 2)	MAX.	UNIT
Pulse Timing of SH and φ1, φ2	t1	60	300	—	ns
	t5	0	300	—	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	300	1000	—	ns
Pulse Timing of SH and φM	t6	20	50	—	ns
φ1, φ2 Pulse Rise Time, Fall Time	t9, t10	0	20	—	ns
Pulse Timing of φ1, φ2 and φM	t11, t13	20	100	—	ns
	t8, t12, t14	40	100	—	ns
φM Pulse Rise Time, Fall Time	t7, t15, t16	0	20	—	ns
φM Pulse Width	t17, t18	80	250	—	ns
Video Data Delay Time (Note 3)	t19	—	45	—	ns
S/H Video Data Delay Time	t20, t21	—	70	—	ns

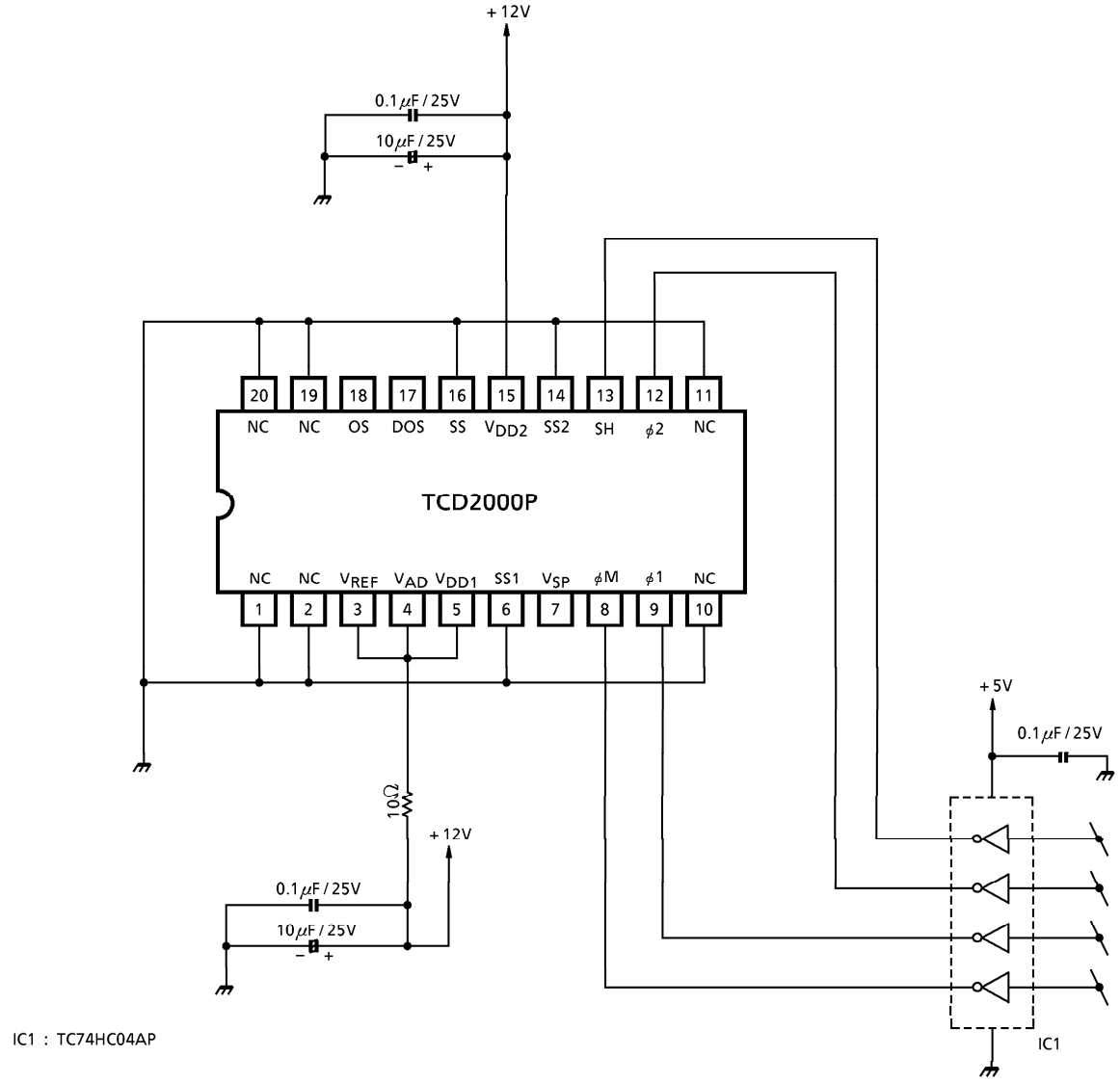
(Note 2) TYP. is the case of f_ϕ = 1MHz.
(Note 3) Load Resistance is 100kΩ.

ELEMENT SHAPE

Unit : μm



TYPICAL DRIVE CIRCUIT



IC1 : TC74HC04AP

CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

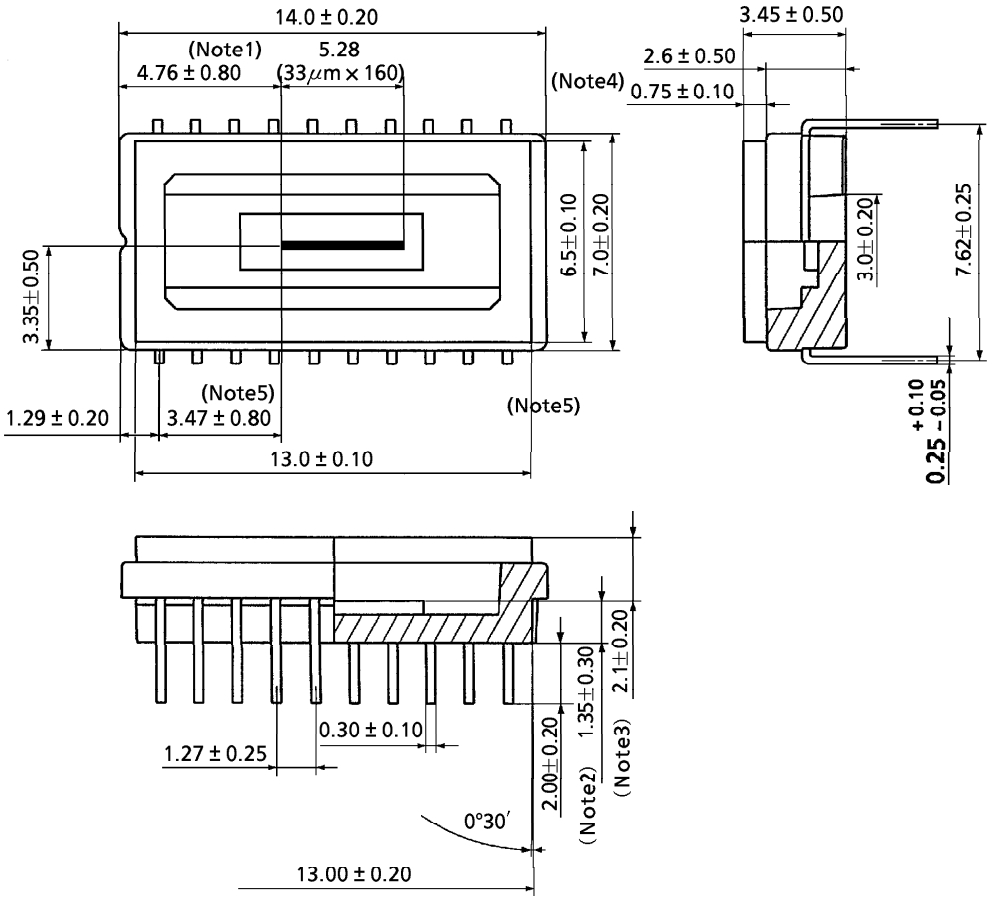
   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming

   Since this package is not shoutagainst mechanical stress, you should not reform the lead frame.
   We recommend to use a IC-inserter when you assemble to PCB.

OUTLINE DRAWING

Unit : mm



(Note1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note3) TOP OF CHIP TO OF PACKAGE.
(Note4) GLASS THICKNESS (n = 1.5)
(Note5) No. 1 SENSOR ELEMENT (S1) TO CENTER OF No. 1 PIN.

Weight : 1.0g (Typ.)