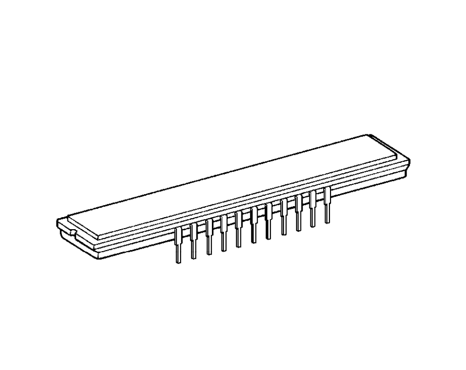
TENTATIVE TOSHIBA CCD LINEAR IMAGE SENSOR CCD (Charge Coupled Device)

TCD2558D

The TCD2558D is a high sensitive and low dark current 5340 elements × 3 line CCD color image sensor which includes CCD drive circuit, clamp circuit.
The sensor can be used for image scanner. The device contains a row of 5340 × 3 photodioeds, which provide a 24 lines / mm (600DPI) across a A4 size paper. The divice is operated by 5 V (Pulse), and 12 V power supply.



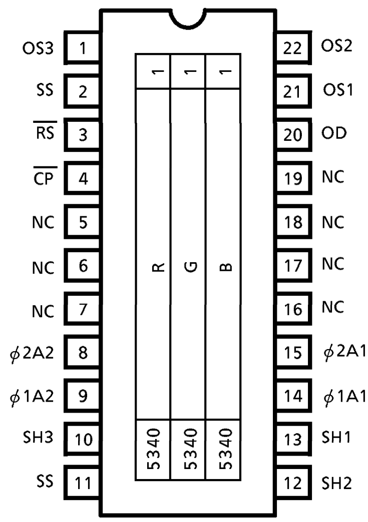
WDIP22-G-400-2.54D (A)

Weight : 5.2 g (Typ.)

FEATURES

- Number of Image Sensing Elements : 5340 elements × 3 line
- Image Sensing Element Size : 7 μm by 7 μm on 7 μm centers
- Photo Sensing Region : High sensitive and low dark current PN photodiode
- Distance Between Photodiode Array : 28 μm, 4 line
- Clock : 2 phase (5 V)
- Power Supply : 12 V Power supply voltage
- Internal Circuit : Clamp Circuit
- Package : 22 pin CERDIP package
- Color Filter : Red, Green, Blue

PIN CONNECTIONS



(TOP VIEW)

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_ϕ	−0.3~8	V
Shift Pulse Voltage	V_{SH}		
Reset Pulse Voltage	$V_{\overline{RS}}$		
Clamp Pulse Voltage	$V_{\overline{CP}}$		
Power Supply	V_{OD}	−0.3~15	V
Operating Temperature	T_{opr}	0~60	°C
Storage Temperature	T_{stg}	−25~85	°C

(Note 1) : All voltage are with respect to SS terminals (Ground).

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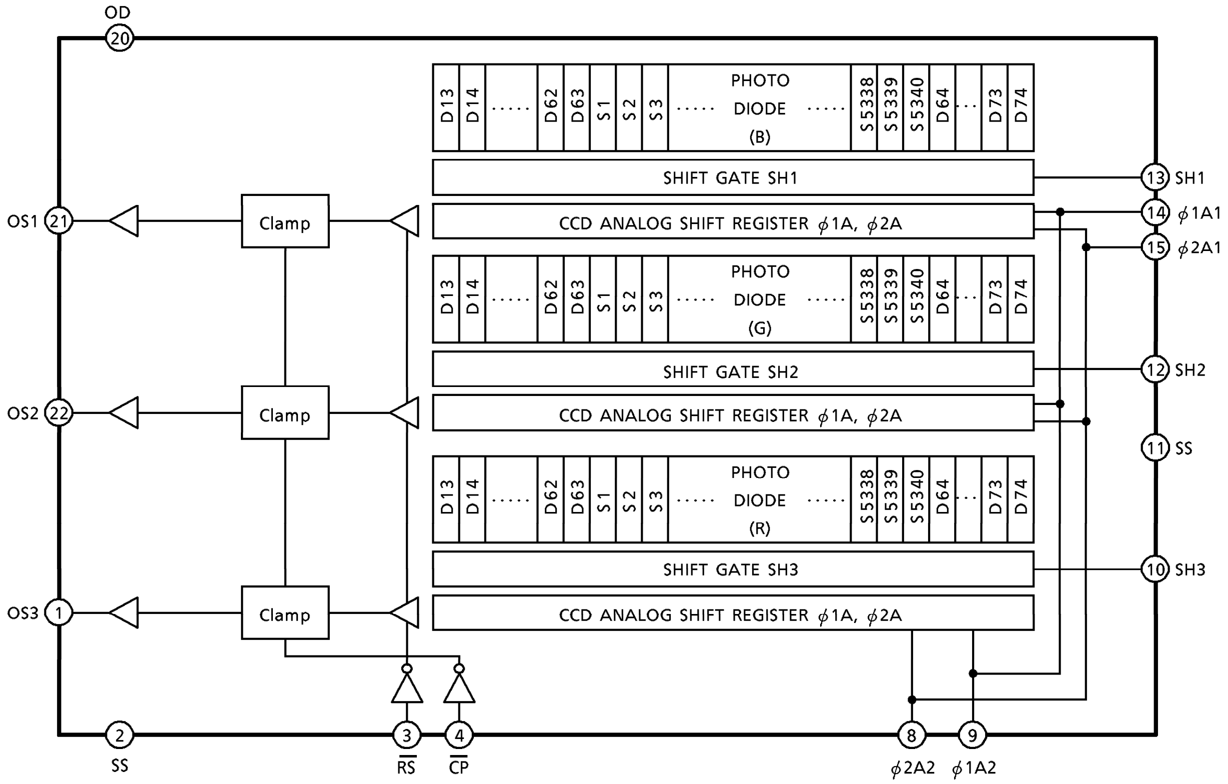
CIRCUIT DIAGRAM



PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS3	Signal Output 3 (Red)	12	SH2	Shift Gate 2
2	SS	Ground	13	SH1	Shift Gate 1
3	$\overline{RS}$	Reset Gate	14	φ1A1	Clock 1 (Phase 1)
4	$\overline{CP}$	Clamp Gate	15	φ2A1	Clock 1 (Phase 2)
5	NC	Non Connection	16	NC	Non Connection
6	NC	Non Connection	17	NC	Non Connection
7	NC	Non Connection	18	NC	Non Connection
8	φ2A2	Clock 2 (Phase 2)	19	NC	Non Connection
9	φ1A2	Clock 2 (Phase 1)	20	OD	Power
10	SH3	Shift Gate 3	21	OS1	Signal Output 1 (Blue)
11	SS	Ground	22	OS2	Signal Output 2 (Green)

OPTICAL / ELECTRICAL CHARACTERISTICS
(Ta = 25°C, V_{OD} = 12 V, $V\phi$ = $V_{\overline{SH}}$ = $V_{\overline{RS}}$ = $V_{\overline{CP}}$ = 5 V (PULSE), $f\phi$ = 1 MHz, $f_{\overline{RS}}$ = 1 MHz, t_{INT} = 10 ms, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1 mm), LOAD RESISTANCE = 100 kΩ)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R_R	6.5	9.3	12.1	V / (lx·s)	(Note 2)
	R_G	6.9	9.9	12.9		
	R_B	3.8	5.4	7.0		
Photo Response Non Uniformity	PRNU (1)	—	10	20	%	(Note 3)
	PRNU (3)	—	3	12	mV	(Note 4)
Image Lag	IL	—	1	—	%	(Note 5)
Saturation Output Voltage	V_{SAT}	3.2	3.5	—	V	(Note 6)
Saturation Exposure	SE	—	0.35	—	lx·s	(Note 7)
Dark Signal Voltage	V_{DRK}	—	0.5	2.0	mV	(Note 8)
Dark Signal Non Uniformity	DSNU	—	5.0	9.0	mV	(Note 8)
DC Power Dissipation	P_D	—	430	600	mW	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	Z_O	—	0.1	1.0	kΩ	
DC Signal Output Voltage	V_{OS}	5	6	7	V	(Note 9)
Random Noise	$N_{D\sigma}$	—	0.8	—	mV	(Note 10)
Reset Noise	V_{RSN}	—	0.5	1.0	V	(Note 9)

(Note 2) : Responsivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

(Note 3) : PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

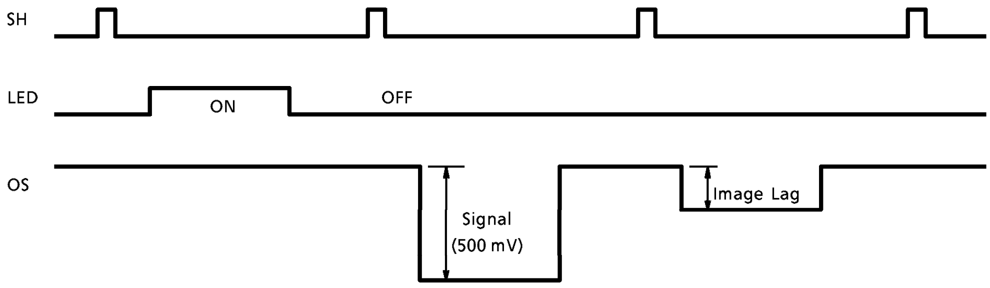
$$\mathrm{PRNU\ (1)} = \frac{\Delta \chi}{\overline{\chi}} \times 100\ (\%)$$

When $\overline{\chi}$ is average of total signal output and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$. The amount of incident light is shown below.

Red = 1 / 2 · SE
Green = 1 / 2 · SE
Bule = 1 / 4 · SE

(Note 4) : PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).

(Note 5) : Image Lag is defined as follows.

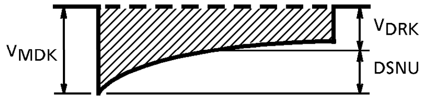


(Note 6) : V_{SAT} is defined as minimum saturation output of all effective pixels.

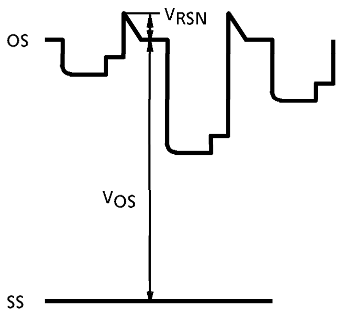
(Note 7) : Definition of SE

$$SE = \frac{V_{SAT}}{R_G} \ (lx \cdot s)$$

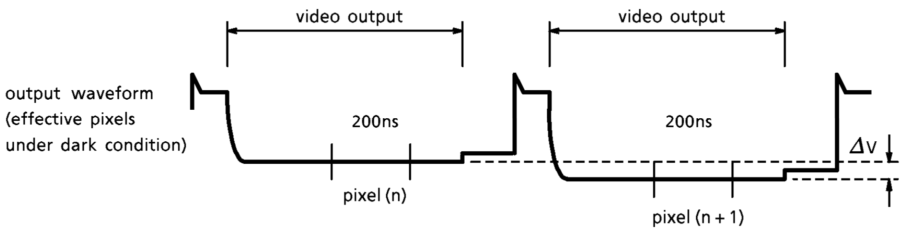
(Note 8) : V_{DRK} is defined as average dark signal voltage of all effective pixels.
DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



(Note 9) : DC signal output voltage is defined as follows.
Reset Noise Voltage is defined as follows.



(Note 10) : Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
2) Each of the output level at video output periods averaged over 200ns period to get V (n) and V (n + 1).
3) V (n + 1) is subtracted from V (n) to get ΔV.

$$\Delta V = V(n) - V(n+1)$$

4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i| \qquad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get sigma value.
6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

7) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$ND\ \sigma = \frac{1}{\sqrt{2}}\,\overline{\sigma}$$

OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Voltage	"H" Level	$V\phi A$	4.5	5.0	5.5	V	
	"L" Level		0.0	—	0.5		
Shift Pulse Voltage	"H" Level	V_{SH}	$V\phi A$"H" − 0.5	$V\phi A$"H"	$V\phi A$"H"	V	(Note 11)
	"L" Level		0.0	—	0.5		
Reset Pulse Voltage	"H" Level	$V_{\overline{RS}}$	4.5	5.0	5.5	V	
	"L" Level		0.0	—	0.5		
Clamp Pulse Voltage	"H" Level	$V_{\overline{CP}}$	4.5	5.0	5.5	V	
	"L" Level		0.0	—	0.5		
Power Supply Voltage		V_{OD}	11.4	12.0	13.0	V	

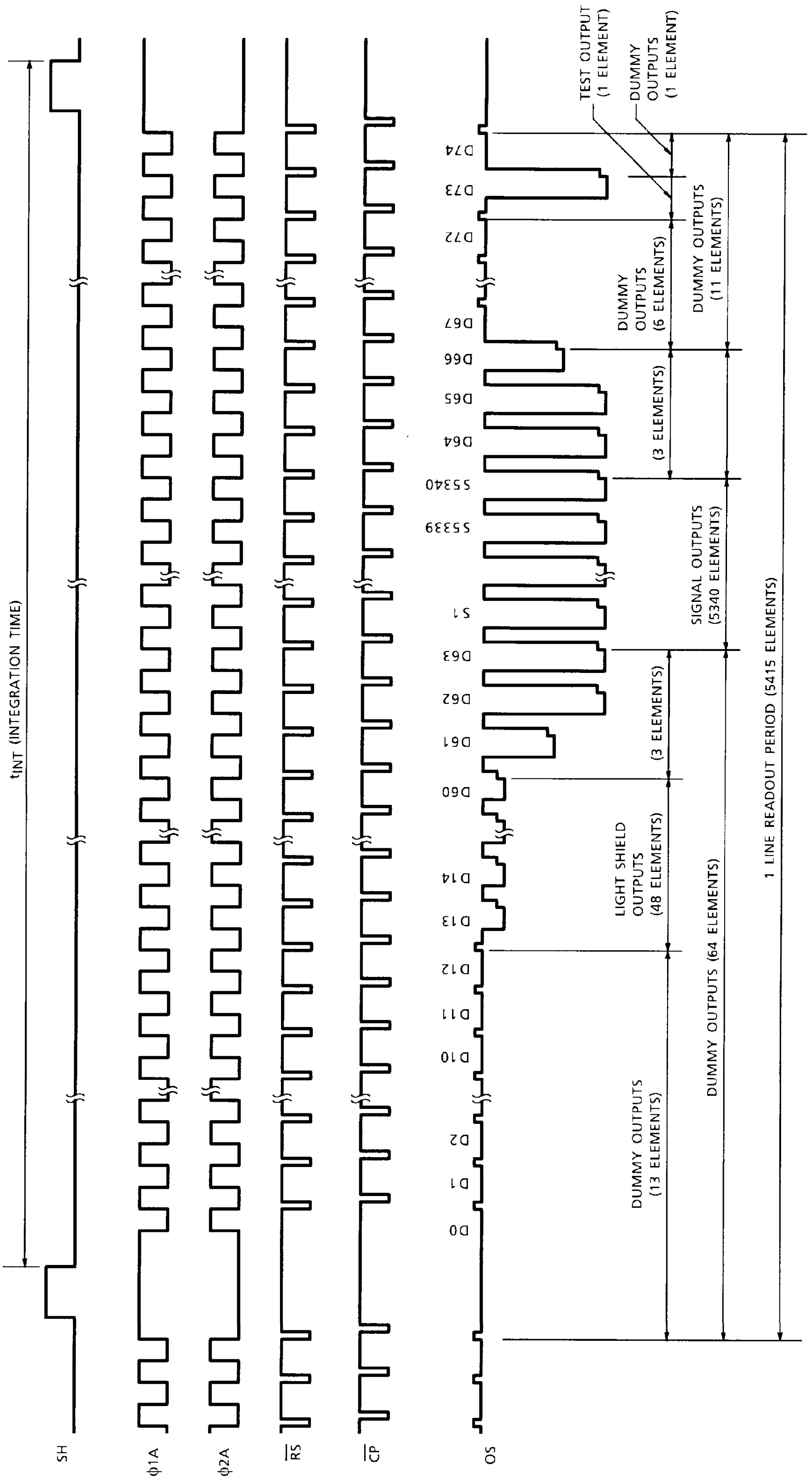
(Note 11) : $V\phi A$"H" means the high level voltage of $V\phi A$ when SH pulse is high level.

CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	$f\phi$	0.3	1.0	10	MHz
Reset Pulse Frequency	$f_{\overline{RS}}$	0.3	1.0	10	MHz
Clamp Pulse Frequency (Bit clamp mode)	$f_{\overline{CP}}$	0.3	1.0	10	MHz
Clock 1 Capacitance (Note 12)	$C\phi 1$	—	140	210	pF
Clock 2 Capacitance (Note 12)	$C\phi 2$	—	120	180	pF
Shift Gate Capacitance	C_{SH}	—	20	60	pF
Reset Gate Capacitance	$C_{\overline{RS}}$	—	10	30	pF
Clamp Gate Capacitance	$C_{\overline{CP}}$	—	10	30	pF

(Note 12) : V_{OD} = 12 V

TIMING CHART (BIT CLAMP MODE)



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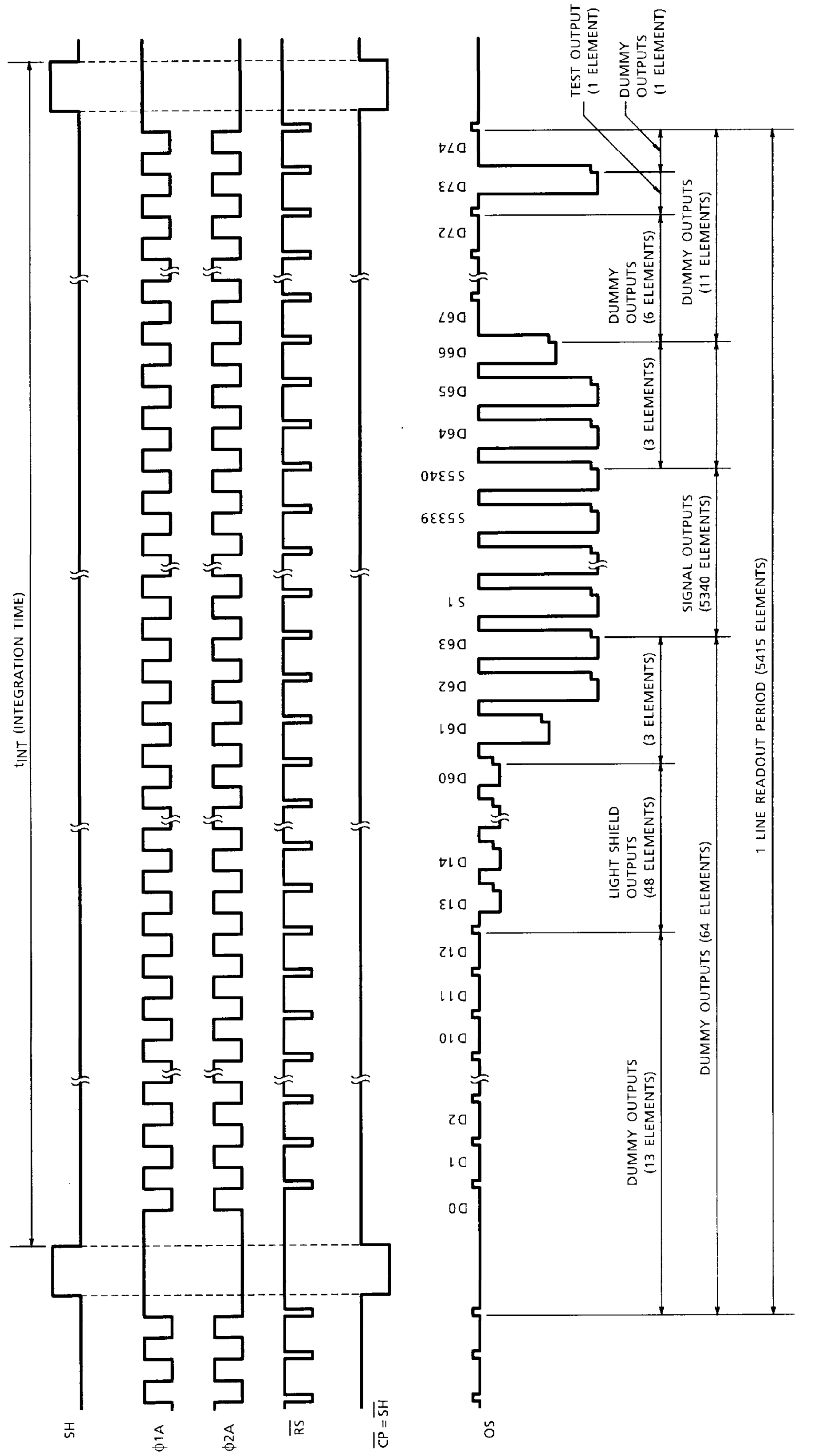
TIMING CHART (LINE CLAMP MODE)



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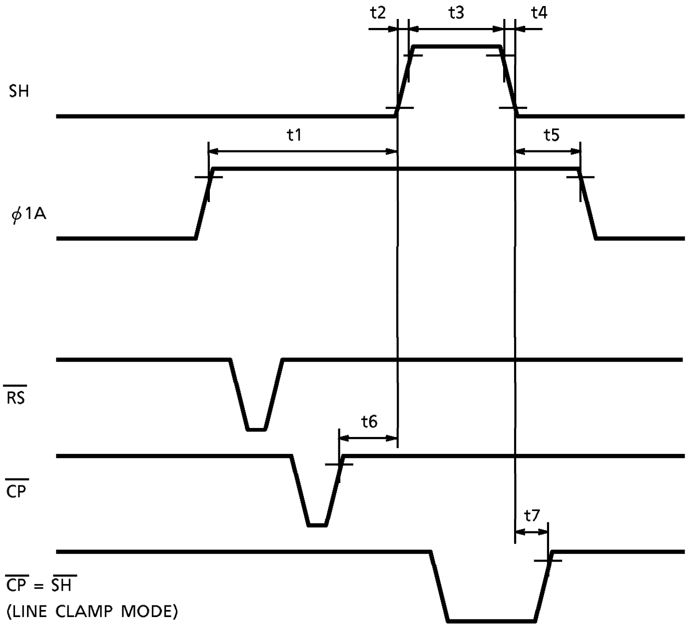
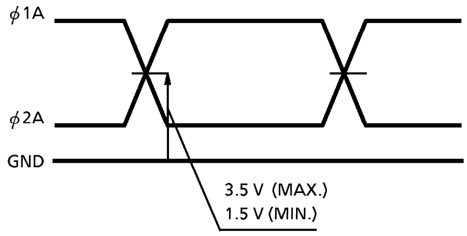
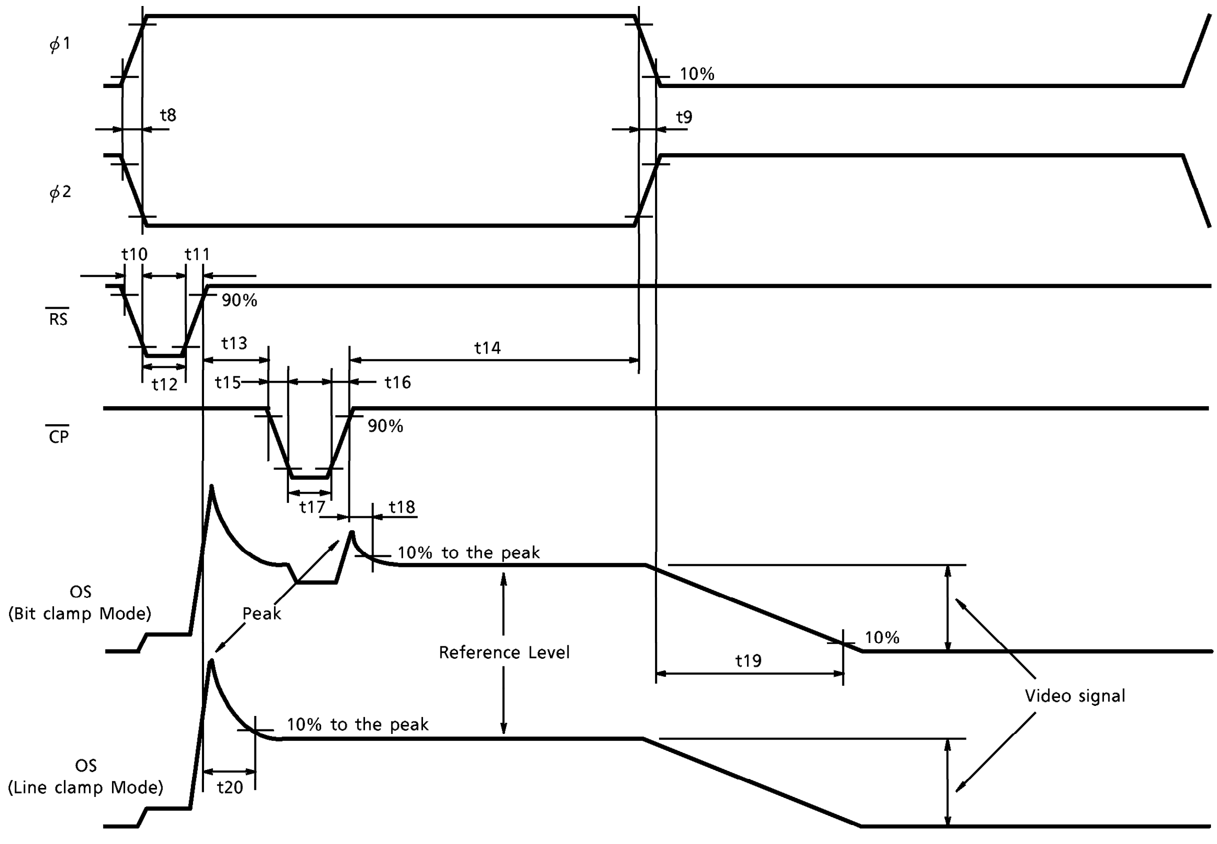
TIMING REQUIREMENTS







TIMING REQUIREMENTS

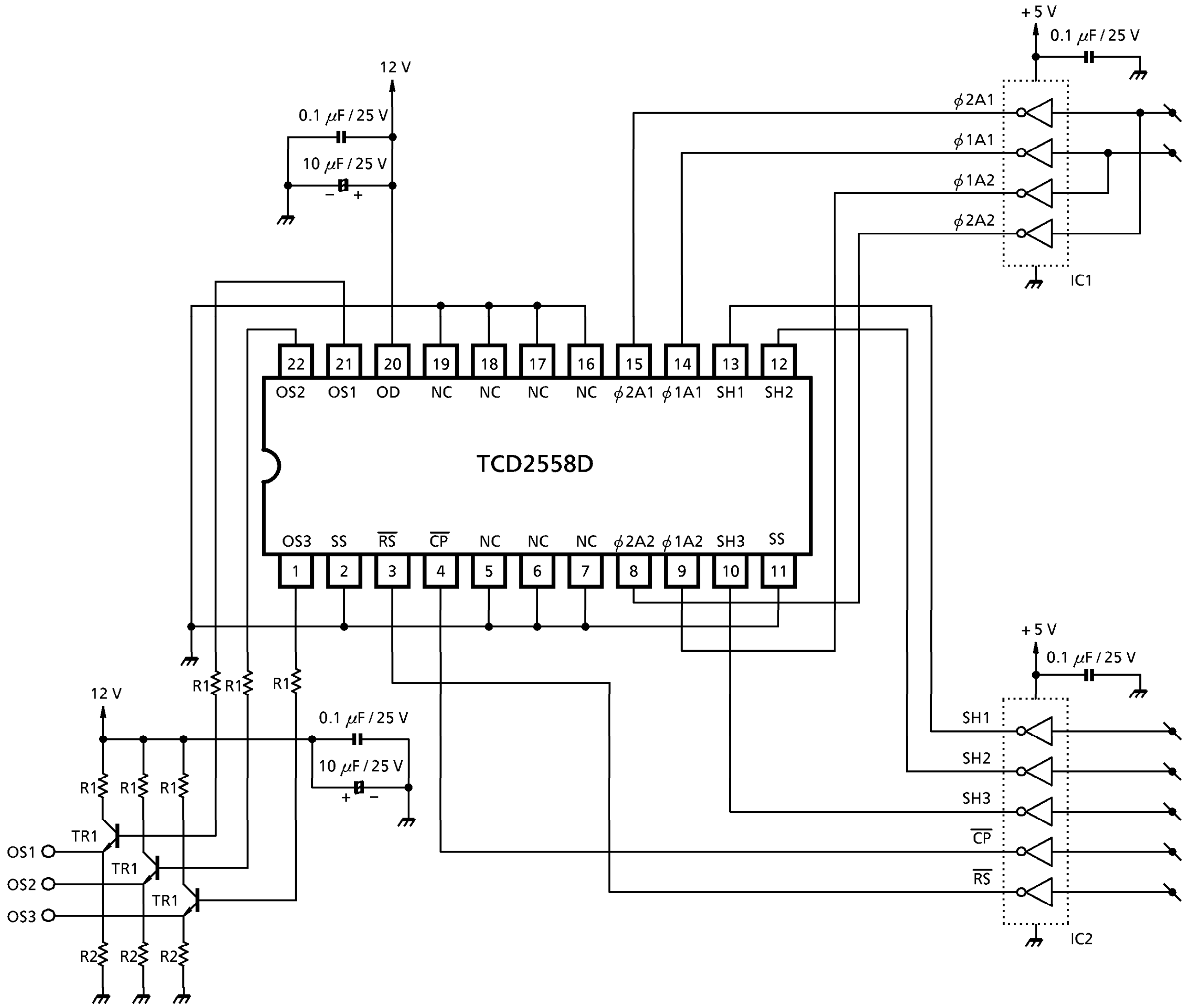
CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 13)	MAX.	UNIT
Pulse Timing of SH and ϕ1	t1	120	1000	—	ns
	t5	800	1000	—	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	3000	5000	—	ns
Pulse Timing of SH and $\overline{CP}$	t6	200	500	—	ns
Pulse Timing of SH and $\overline{CP}$ (Line clamp mode)	t7	10	100	—	ns
ϕ1, ϕ2 Pulse Rise Time, Fall Time	t8, t9	0	50	—	ns
$\overline{RS}$ Pulse Rise Time, Fall Time	t10, t11	0	20	—	ns
$\overline{RS}$ Pulse Width	t12	10 (25)	80	—	ns
Pulse Timing of $\overline{RS}$ and $\overline{CP}$	t13	10	20	—	ns
Pulse Timing of ϕ1A, ϕ2A and $\overline{CP}$	t14	0	20	—	ns
$\overline{CP}$ Pulse Rise Time, Fall Time	t15, t16	0	20	—	ns
$\overline{CP}$ Pulse Width (Note 14)	t17	25 (3000)	80 (5000)	—	ns
Reference Level Settle Time (Bit clamp mode)	t18	—	20	45 (Note 17)	ns
Video Data Delay Time (Note 15)	t19	—	20	45 (Note 16)	ns
Reference Level Settle Time (Line clamp mode)	t20	—	35	55 (Note 17)	ns

(Note 13) : TYP. is the case of $f_{\overline{RS}}$ = 1.0 MHz
(Note 14) : Line clamp Mode inside ( ).
(Note 15) : Load resistance is 100 kΩ
(Note 16) : Typical settle time to about 1% of final value
(Note 17) : Typical settle time to about 1% of the peak

CLAMP MODE

CLAMP MEANS	CP INPUT PULSE
Bit Clamp	$\overline{CP}$ Pulse
Line Clamp	$\overline{CP}$ = $\overline{SH}$ or $\overline{CP}$ = DC 5 V

TYPICAL DRIVE CIRCUIT



IC1 : TC74AC04AP
IC2 : TC74HC04AP
TR1 : 2SC1815-Y
R1 : 150 Ω
R2 : 1500 Ω

CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N_2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

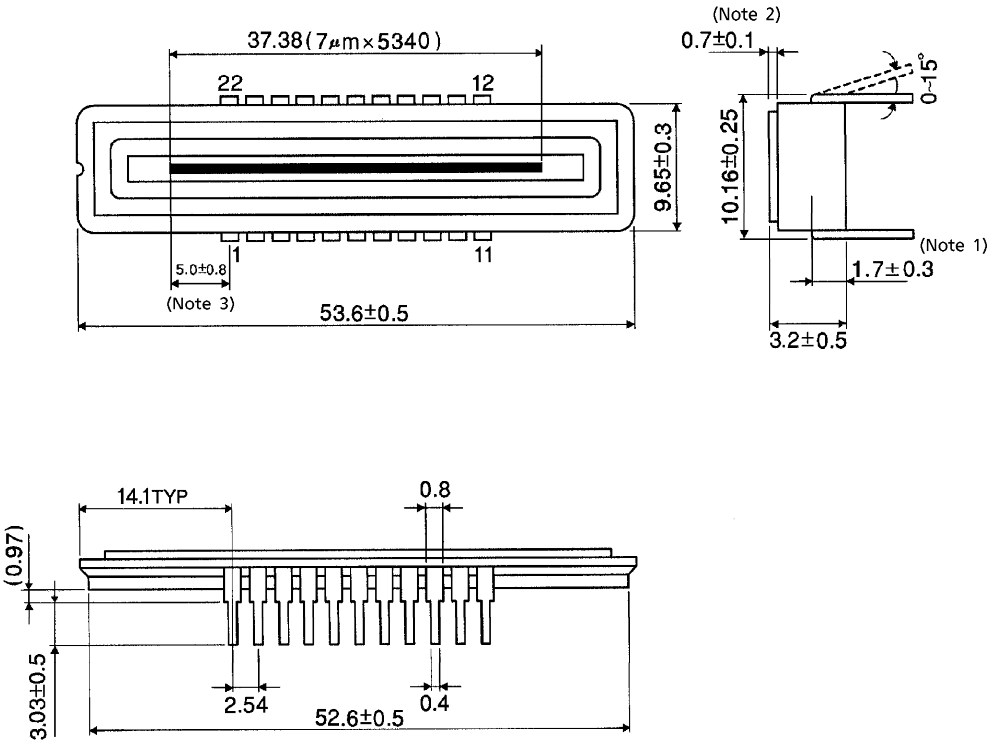
3. Incident Light

   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming
   Since this package is not strong against mechanical stress, you should not reform the lead frame.
   We recommend to use a IC-inserter when you assemble to PCB.

PACKAGE DIMENSIONS

WDIP22-G-400-2.54D (A) Unit : mm



(Note 1) : TOP OF CHIP TO BOTTOM OF PACKAGE.

(Note 2) : GLASS THICKNESS (n = 1.5)

(Note 3) : No.1 SENSOR ELEMENT (S1) TO EDGE OF No.1 PIN.

Weight : 5.2 g (Typ.)