TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

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Octal D-Type Flip-Flop with 3-State Output

The TC7MET374AFK is an advanced high speed CMOS octal flip-flop with 3-state output fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (*) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.
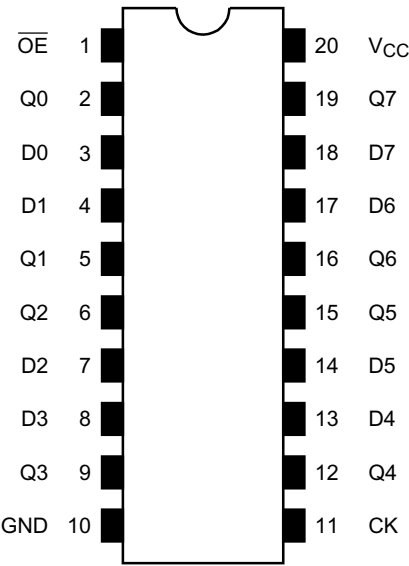
   *: output in off-state

VSSOP20-P-0030-0.50
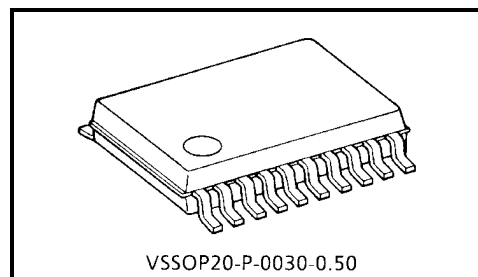
Weight: 0.03 g (typ.)

Features

- High speed: f_{max} = 140 MHz (typ.) (V_{CC} = 5 V)

- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)

- Compatible with TTL outputs: V_{IL} = 0.8 V (max)
                                 V_{IH} = 2.0 V (min)

- Power down protection is provided on all inputs and outputs.

- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$

- Low noise: V_{OLP} = 1.5 V (max)

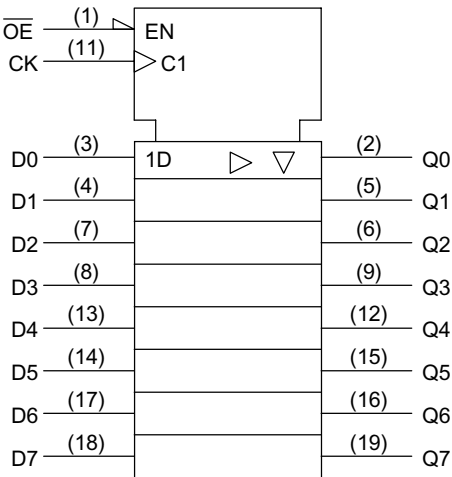- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 374 type.

000630EBA1

Pin Assignment (top view)

$\overline{OE}$	1		20	V_{CC}	
Q0	2		19	Q7	
D0	3		18	D7	
D1	4		17	D6	
Q1	5		16	Q6	
Q2	6		15	Q5	
D2	7		14	D5	
D3	8		13	D4	
Q3	9		12	Q4	
GND	10		11	CK	

IEC Logic Symbol

$\overline{OE}$ (1) — EN
CK (11) — >C1

D0 (3)	1D ▷ ▽	(2) Q0
D1 (4)		(5) Q1
D2 (7)		(6) Q2
D3 (8)		(9) Q3
D4 (13)		(12) Q4
D5 (14)		(15) Q5
D6 (17)		(16) Q6
D7 (18)		(19) Q7

Truth Table

Inputs			Outputs
$\overline{OE}$	CK	D	
H	X	X	Z
L	⌐↓	X	Q_n
L	↑	L	L
L	↑	H	H

X: Don't care

Z: High impedance

Q_n: No change

System Diagram

D0	D1	D2	D3	D4	D5	D6	D7
3	4	7	8	13	14	17	18

CK 11

$\overline{OE}$ 1

2	5	6	9	12	15	16	19
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
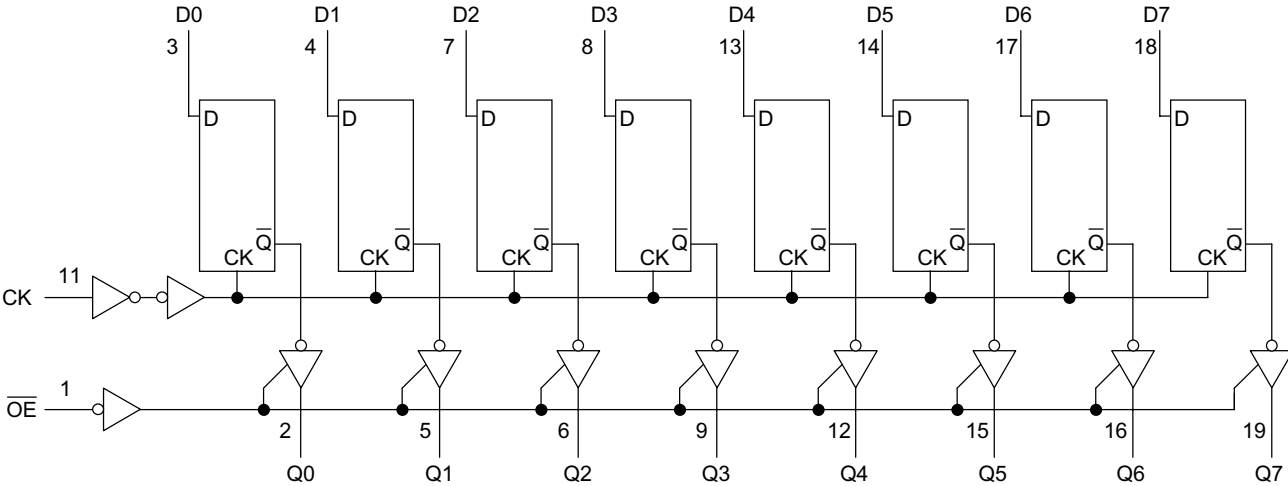
Maximum Ratings

Characteristics	Symbol	Rating		Unit
Supply voltage range	V_{CC}	$-0.5\sim7.0$		V
DC input voltage	V_{IN}	$-0.5\sim7.0$		V
DC output voltage	V_{OUT}	$-0.5\sim7.0$	(Note1)	V
		$-0.5\sim V_{CC}+0.5$	(Note2)	
Input diode current	I_{IK}	-20		mA
Output diode current	I_{OK}	±20	(Note3)	mA
DC output current	I_{OUT}	±25		mA
DC V_{CC}/ground current	I_{CC}	±75		mA
Power dissipation	P_D	180		mW
Storage temperature	T_{stg}	$-65\sim150$		°C

Note1: Output in off-state

Note2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note3: $V_{OUT} <$ GND, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

Characteristics	Symbol	Rating		Unit
Supply voltage	V_{CC}	$4.5\sim5.5$		V
Input voltage	V_{IN}	$0\sim5.5$		V
Output voltage	V_{OUT}	$0\sim5.5$	(Note4)	V
		$0\sim V_{CC}$	(Note5)	
Operating temperature	T_{opr}	$-40\sim85$		°C
Input rise and fall time	dt/dv	$0\sim20$		ns/V

Note4: Output in off-state

Note5: High or low state

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		Unit
						Min	Typ.	Max	Min	Max	
Input voltage	High level	V_{IH}	—		4.5~5.5	2.0	—	—	2.0	—	V
	Low level	V_{IL}	—		4.5~5.5	—	—	0.8	—	0.8	
Output voltage	High level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50$ μA	4.4	4.5	—	4.4	—	—	V
				$I_{OH} = -8$ mA	3.94	—	—	3.80	—	—	
	High level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μA	—	0	0.1	—	0.1	0.1	
				$I_{OL} = 8$ mA	—	—	0.36	—	0.44	0.44	
3-state output off-state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current		I_{IN}	$V_{IN} = 5.5$ V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	—	40.0	μA
		I_{CCT}	Per input: $V_{IN} = 3.4$ V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current		I_{OPD}	$V_{OUT} = 5.5$ V		0	—	—	0.5	—	5.0	μA

Timing Requirements (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C		Ta = −40~85°C	Unit
				Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_{w (H)}$ $t_{w (L)}$	—	5.0 ± 0.5	—	6.5	8.5	ns
Minimum set-up time	t_s	—	5.0 ± 0.5	—	2.5	2.5	ns
Minimum hold time	t_h	—	5.0 ± 0.5	—	2.5	2.5	ns

AC Electrical Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	4.1	9.4	1.0	10.5	ns
				50	—	5.6	10.4	1.0	11.5	
3-state output enable time	t_{pZL} t_{pZH}	$R_L = 1$ kΩ	5.0 ± 0.5	15	—	6.5	10.2	1.0	11.5	ns
				50	—	7.3	11.2	1.0	12.5	
3-state output disable time	t_{pLZ} t_{pHZ} f_{max}	$R_L = 1$ kΩ	5.0 ± 0.5	15	—	7.0	11.2	1.0	12.0	ns
				50	90	140	—	80	—	
Maximum clock frequency	f_{max}	—	5.0 ± 0.5	50	85	130	—	75	—	MHz
Output to output skew	t_{osLH} t_{osHL}	(Note6)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	9	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note7)			—	25	—	—	—	pF

Note6: Parameter guaranteed by design.

$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note7: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:
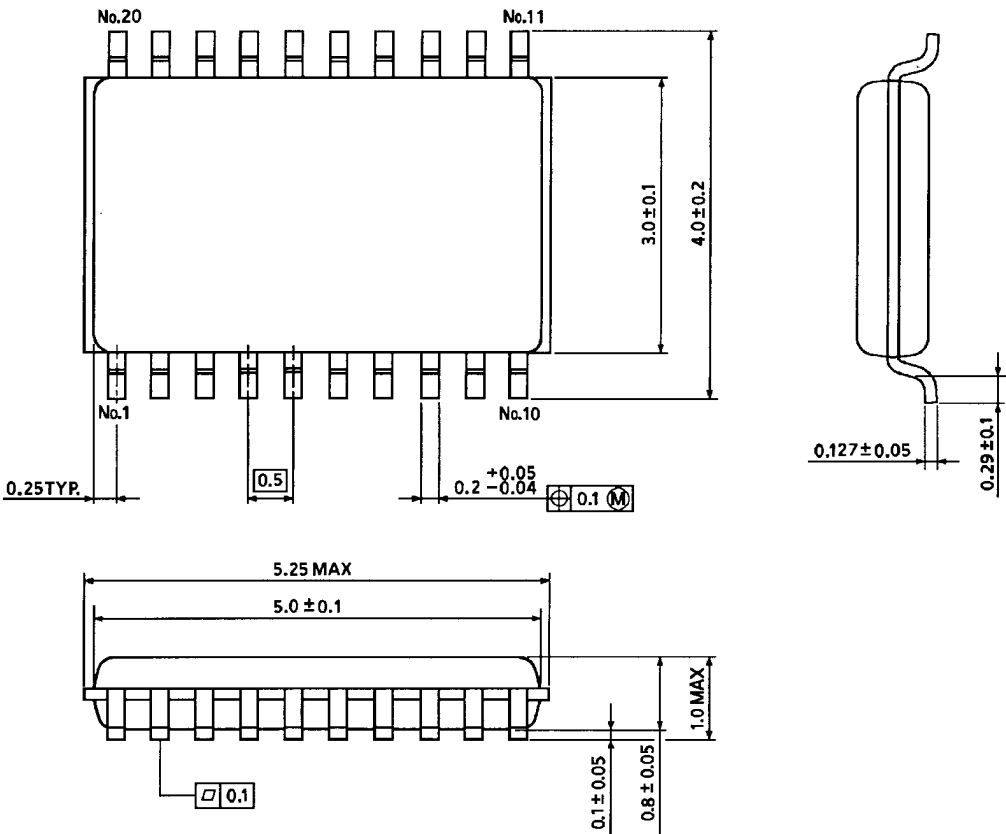
$C_{PD} (total) = 14 + 11 \cdot n$

Noise Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	5.0	1.1	1.5	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	5.0	−1.1	−1.5	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	$C_L = 50$ pF	5.0	—	2.0	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	$C_L = 50$ pF	5.0	—	0.8	V

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm

No.20 No.11

3.0±0.1
4.0±0.2

No.1 No.10

0.25 TYP.
0.5
0.2 +0.05 −0.04
⊕ 0.1 Ⓜ

0.127±0.05
0.29±0.1

5.25 MAX
5.0±0.1
1.0 MAX

□ 0.1

0.1±0.05
0.8±0.05

Weight: 0.03 g (typ.)