

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC7MET374AFK

Octal D-Type Flip-Flop with 3-State Output

The TC7MET374AFK is an advanced high speed CMOS octal flip-flop with 3-state output fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ( $\overline{OE}$ ).

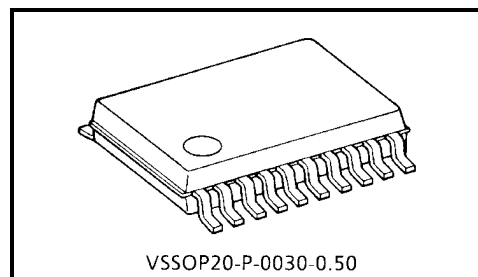
When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (\*) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

\*: output in off-state



Weight: 0.03 g (typ.)

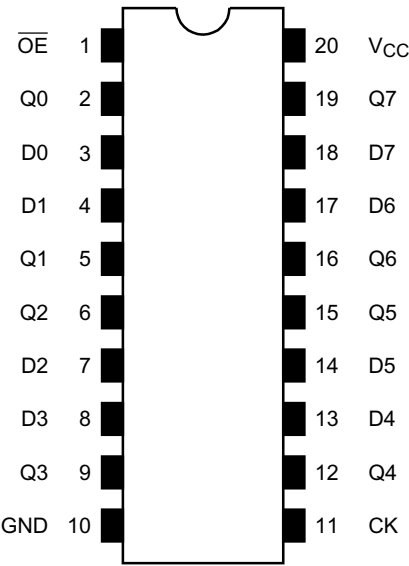
### Features

- High speed:  $f_{\max} = 140 \text{ MHz}$  (typ.) ( $V_{CC} = 5 \text{ V}$ )
- Low power dissipation:  $I_{CC} = 4 \mu\text{A}$  (max) ( $T_a = 25^\circ\text{C}$ )
- Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V}$  (max)  
 $V_{IH} = 2.0 \text{ V}$  (min)
- Power down protection is provided on all inputs and outputs.
- Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- Low noise:  $V_{OLP} = 1.5 \text{ V}$  (max)
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 374 type.

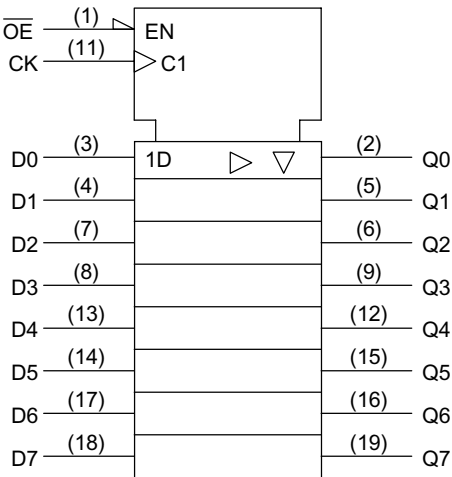
000630EBA1

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.  
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The Toshiba products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These Toshiba products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of Toshiba products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

Pin Assignment (top view)



IEC Logic Symbol

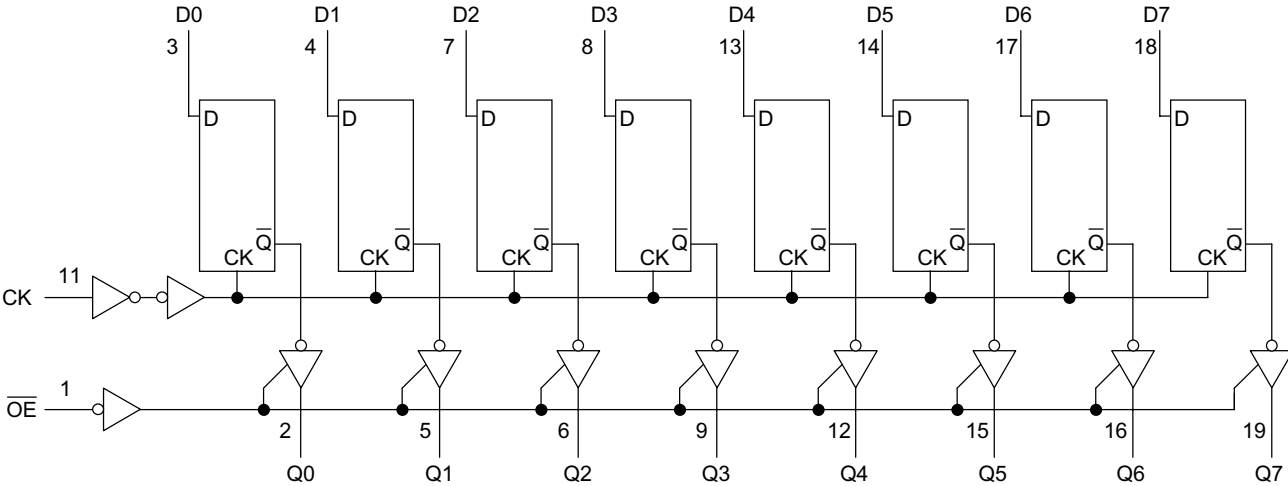


Truth Table

Inputs			Outputs
OE	CK	D	
H	X	X	Z
L		X	Q <sub>n</sub>
L		L	L
L		H	H

X: Don't care  
Z: High impedance  
Q<sub>n</sub>: No change

System Diagram



## Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~7.0	V
DC output voltage	$V_{OUT}$	-0.5~7.0 (Note1)	V
		-0.5~ $V_{CC} + 0.5$ (Note2)	
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	±20 (Note3)	mA
DC output current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /ground current	$I_{CC}$	±75	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65~150	°C

Note1: Output in off-state

Note2: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note3:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5~5.5	V
Input voltage	$V_{IN}$	0~5.5	V
Output voltage	$V_{OUT}$	0~5.5 (Note4)	V
		0~ $V_{CC}$ (Note5)	
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	$dt/dv$	0~20	ns/V

Note4: Output in off-state

Note5: High or low state

## Electrical Characteristics

## DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit	
					V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Input voltage	High level	V <sub>IH</sub>	—		4.5~5.5	2.0	—	—	2.0	—	V
	Low level	V <sub>IL</sub>	—		4.5~5.5	—	—	0.8	—	0.8	
Output voltage	High level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	4.4	4.5	—	4.4	—	—	V
				I <sub>OH</sub> = -8 mA	3.94	—	—	3.80	—	—	
	High level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	—	0	0.1	—	0.1	0.1	
				I <sub>OL</sub> = 8 mA	—	—	0.36	—	0.44	0.44	
3-state output off-state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA
		I <sub>CC</sub> T	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current		I <sub>OPD</sub>	V <sub>OUT</sub> = 5.5 V		0	—	—	0.5	—	5.0	μA

Timing Requirements (Input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	t <sub>w</sub> (H) t <sub>w</sub> (L)	—	5.0 ± 0.5	—	6.5	8.5	ns
Minimum set-up time	t <sub>s</sub>	—	5.0 ± 0.5	—	2.5	2.5	ns
Minimum hold time	t <sub>h</sub>	—	5.0 ± 0.5	—	2.5	2.5	ns

AC Electrical Characteristics (Input:  $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	—	$5.0 \pm 0.5$	15	—	4.1	9.4	1.0	10.5	ns
				50	—	5.6	10.4	1.0	11.5	
3-state output enable time	$t_{pZL}$ $t_{pZH}$	R <sub>L</sub> = 1 kΩ	$5.0 \pm 0.5$	15	—	6.5	10.2	1.0	11.5	ns
				50	—	7.3	11.2	1.0	12.5	
3-state output disable time	$t_{pLZ}$ $t_{pHZ}$ $f_{max}$	R <sub>L</sub> = 1 kΩ	$5.0 \pm 0.5$	15	—	7.0	11.2	1.0	12.0	ns
				50	90	140	—	80	—	
Maximum clock frequency	$f_{max}$	—	$5.0 \pm 0.5$	50	85	130	—	75	—	MHz
Output to output skew	$t_{osLH}$ $t_{osHL}$	(Note6)	$5.0 \pm 0.5$	50	—	—	1.0	—	1.0	ns
Input capacitance	C <sub>IN</sub>	—	—	—	—	4	10	—	10	pF
Output capacitance	C <sub>OUT</sub>	—	—	—	—	9	—	—	—	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note7)	—	—	—	25	—	—	—	pF

Note6: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note7: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C<sub>PD</sub> when n pcs. of latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 14 + 11 \cdot n$$

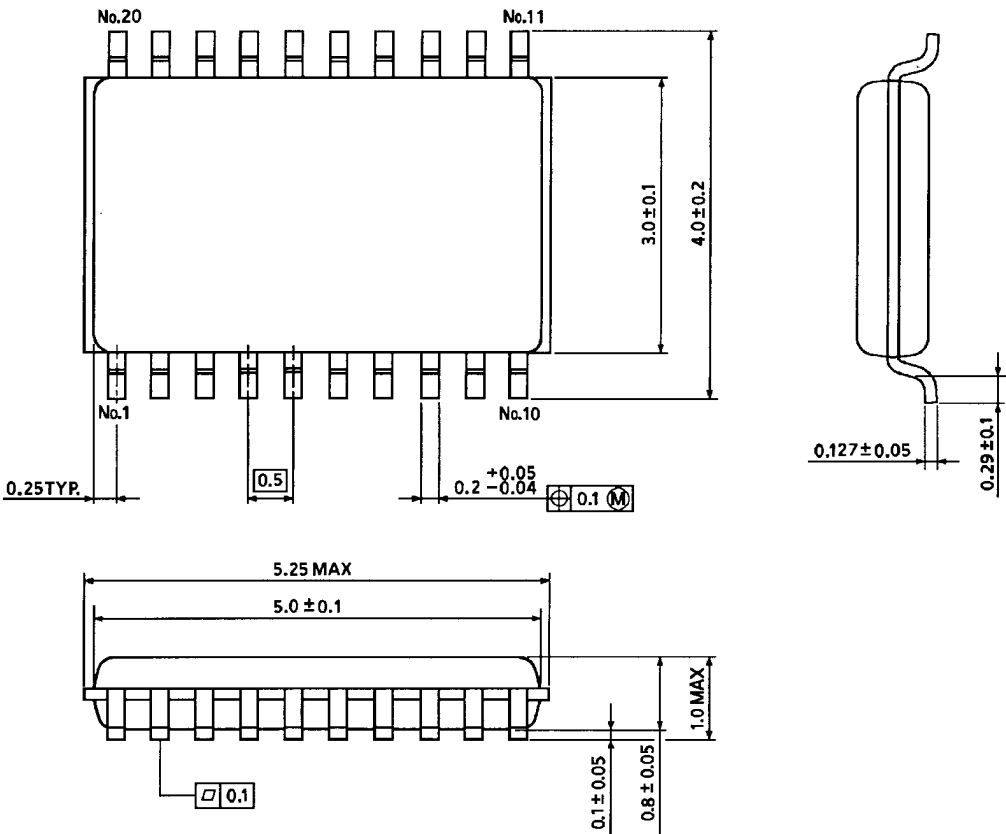
Noise Characteristics (Input:  $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	1.1	1.5	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-1.1	-1.5	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	2.0	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	0.8	V

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)